

# A Standalone Receiver With Multiple Access Interference Rejection, Clock and Data Recovery, and FEC for 2-D $\lambda - t$ OCDMA

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**Abstract**—We demonstrate a standalone (no global clock) receiver for two-dimensional wavelength-time optical code-division multiple-access. The receiver provides the following functions: quantization (to eliminate multiple access interference), clock and data recovery, return-to-zero to nonreturn-to-zero conversion (for optical code-division multiple-access compatibility with digital logic), framing (for byte synchronization), and forward-error correction (FEC) using a (255, 239) Reed–Solomon decoder. The receiver more than doubles the number of supported users at a bit-error rate  $< 10^{-10}$ . The receiver supports an information rate of 156.25 Mb/s. We performed the measurements at a bit rate of 167.4 Mb/s and a chip rate of 1.339 Gb/s (eight chips per bit) to account for FEC overhead.

**Index Terms**—Clock and data recovery (CDR), forward-error correction (FEC), optical code-division multiple-access (OCDMA), optical fiber communications, optical receiver, Reed–Solomon (RS) codes.

## I. INTRODUCTION

THE attractions of code-division multiplexing lie in the asynchronous, completely decentralized, and uncoordinated transmissions among users. Bit rates considered moderate by optical standards (155 and 622 Mb/s) are more than sufficient to meet the requirements for video and data delivery for the first generation of fiber-to-the-home. The soft capacity of a code-division multiple-access (CDMA) system permits growing the client base beyond the nominal maximum capacity (while accepting some quality of service degradation) without extensive upgrades to the infrastructure.

Practical considerations such as imperfect clock recovery and the efficiency of forward-error correction (FEC) are required to give system designers accurate estimates of the quality of service guarantees that can be delivered, while still providing margin for exploiting the soft capacity. Note that time-division

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multiple-access systems proposed for current passive optical networks standards have hard capacity, and they require infrastructure upgrades to expand the client base.

In [1], FEC was used in a coherent optical CDMA (OCDMA) system, whereas in [2] FEC was used in a spectral amplitude coding OCDMA system. In this letter, we present FEC for a two-dimensional (2-D) wavelength-time ( $\lambda - t$ ) OCDMA system. Moreover, we present for the first time a complete standalone OCDMA receiver that includes a quantizer to eliminate multiple access interference (MAI), a clock and data recovery (CDR) unit, and an FEC module. We address how soft capacity can be increased with the use of FEC while working with a recovered clock that provides practical nonideal sampling.

## II. OCDMA SYSTEM

The OCDMA test bed is presented in Fig. 1(a). The desired information rate was 156.25 Mb/s. Since we used eight chips per bit and a Reed–Solomon (RS) code introducing  $\sim 15/14$  of overhead [RS(255, 239)], we used a chip rate and a bit rate of 1.339 Gchip/s and 167.4 Mb/s, respectively. A broadband erbium-doped fiber source is modulated by a polarization-insensitive electroabsorption modulator. The extinction ratio is 11 dB and the modulating signal is a  $2^{15} - 1$  pseudorandom binary sequence. The data is FEC-encoded in a return-to-zero (RZ) format with 1/8 duty cycle. The modulated signal is amplified and sent to the OCDMA encoders through an optical coupler. The encoders are preceded by optical delay lines to decorrelate their data. The OCDMA encoded signals are combined, amplified, and sent to Decoder 1. The optical power before the photodetector is controlled with a variable optical attenuator. The output of the photodetector is low-pass filtered by a fourth-order Bessel–Thomson filter whose  $-3$ -dB cutoff frequency is  $0.7 \times$  chip rate, or 933 MHz. Such a filter reduces intensity noise from the incoherent broadband source [3]. Bit-error-rate (BER) measurements were performed on 1) the RZ data (OCDMA receiver bypassed) sampled with a global clock, and 2) the recovered nonreturn-to-zero (NRZ) data sampled with the recovered clock. In the second case, we measured the BER with and without RS decoding to determine the coding gain.

Fig. 1(b) presents the decoded optical spectrum before the photodetector. The solid line is for User 1 alone while the dashed line is for all six users active. Note that the sixth wavelength of Decoder 1 is used only by User 1. All other wavelengths are shared by at least one interferer. Each encoder in the system

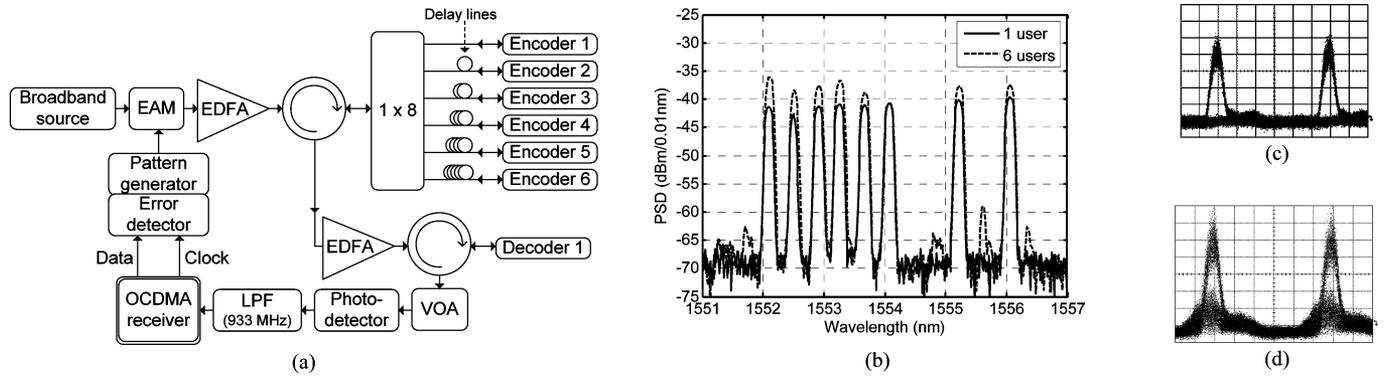


Fig. 1. (a) Block diagram of the experimental setup, (b) optical spectrum after Decoder 1 for one and six users, and oscilloscope traces after the LPF for (c) one user and (d) six users. EAM: electroabsorption modulator. EDFA: erbium-doped fiber amplifier. VOA: variable optical attenuator. LPF: low-pass filter.

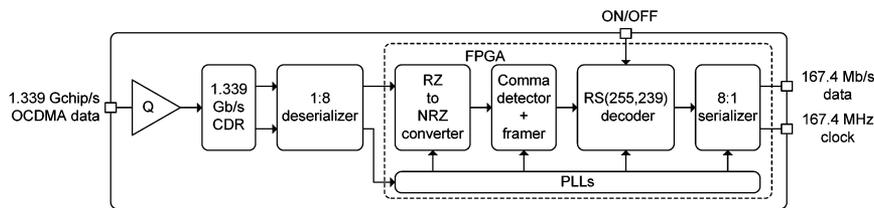


Fig. 2. Block diagram of the OCDMA receiver. The blocks within the dotted area were implemented on an FPGA.  $Q$ : quantizer. PLL: phase-locked loop.

consists of eight fiber Bragg gratings (FBGs) written in series, whose passbands and physical positions in the fiber determine the code. The FBG spectrums are 20 GHz wide and the channel spacing is 50 GHz. Code length and weight are 29 and 8, respectively. Encoder 2 has five common wavelengths with Encoder 1, whereas Encoders 3–5 have two and Encoder 6 has a single wavelength in common. The delays between decoded User 1 and the five interferers are adjusted such that interfering wavelengths appear within the autocorrelation peak of User 1 [Fig. 1(c)–(d)]. This corresponds to a worst-case scenario, thus allowing testing of the OCDMA receiver under severe conditions. The 2-D  $\lambda - t$  codes are given in [4], where they are called fast-frequency-hopping codes. Encoders 1 to 6 are labeled, respectively, as  $K$ ,  $O$ ,  $I$ ,  $G$ ,  $H$ , and  $C$  in [4].

### III. OCDMA RECEIVER

The OCDMA receiver that we designed is shown in Fig. 2. The blocks outside of the dotted area correspond to the receiver that was used in [5] and [6]. The quantizer ( $Q$ ) applies a threshold on the incoming data in order to filter out MAI. Any MAI above the threshold is not eliminated by the quantizer and can prevent the CDR from locking because of unexpected edges. The CDR recovers the clock at the chip rate for optimum sampling. In [5] and [6], the deserializer was used for RZ-to-NRZ conversion, whereas here it is used to reduce the frequency of the data for further processing by digital logic. The blocks inside the dotted area, which were implemented on a Virtex II Pro FPGA from Xilinx, enhance the OCDMA receiver described in [5] and [6] with automatic detection of the payload chips and RS(255, 239) decoding. The RZ-to-NRZ converter determines the index (zero to seven) of the payload chips using eight counters. This process happens quickly after reset. The first counter to reach a count of 20 determines the

payload index. The payload detection algorithm, therefore, requires 20 bits. If MAI is guaranteed never to go above the threshold, then the algorithm could use a single bit. Otherwise, the algorithm stands a better chance of returning the right payload index value if more bits are used.

Once the RZ-to-NRZ converter has identified the payload index, it remains locked on that index until the receiver is reset again. Only the payload chips make it through the RZ-to-NRZ converter, therefore dividing down the parallel data rate by eight. Hence, the operating frequency of the comma detector, the framer, and the decoder is around 21 MHz ( $1.339 \text{ GHz}/8/8$ ). This frequency is easily supported by most FPGAs. Upon reset, the comma detector looks for a preprogrammed comma—a unique 16-bit character. The framer uses the comma to realign the data. The realigned data is then sent to the RS decoder, which either outputs decoded or undecoded data as selected by the user. The RS decoder is an IP core from Xilinx LogiCORE portfolio. The 8:1 serializer finally performs a parallel-to-serial conversion to output NRZ data at 167.4 Mb/s.

### IV. RESULTS AND DISCUSSION

The performance of the OCDMA system with the global clock (solid curves) and the recovered clock (dashed curves) is shown in Fig. 3(a). The results were obtained with worst-case MAI and no FEC. Note that the abscissa is the useful power, i.e., the optical power contributed by the desired user at the photodiode. The BER floors for three to six users are due to the intensity noise from the incoherent source [3], [4]. When sampling with the recovered clock, we observe no appreciable power penalty compared to the global clock case. This result is an improvement over the result obtained in [6], where a power penalty of 3.3–3.5 dB was measured at a BER of  $10^{-9}$ . The improvement is due to a sampling optimization. In this work, the CDR operates at the chip

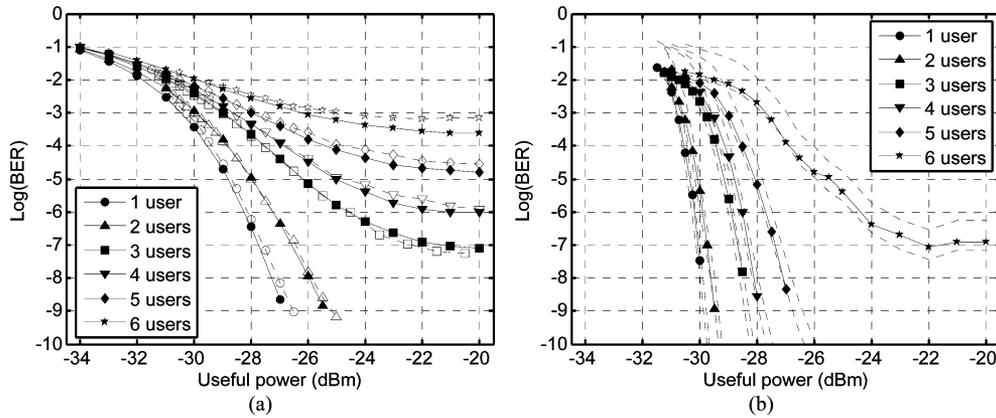


Fig. 3. BER performance of a six-user OCDMA system. (a) BER with the global clock (solid curves) and the recovered clock (dashed curves), no FEC. (b) Experimental (solid curves) and theoretical (dashed curves) BER with the recovered clock and FEC. For all cases with no BER floor, we obtained error-free operation for over 1 min at 156.25 Mb/s ( $\text{BER} < 10^{-10}$ ).

rate; in [6], the CDR was operating at twice the chip rate due to the unavailability of a 1 : 8 deserializer for RZ-to-NRZ conversion. The chips were, therefore, sampled on each side of the optimum sampling point, explaining the power penalty.

Fig. 3(b) shows the BER with FEC. The system can support five simultaneous users in the detection window (compared to two without FEC). The receiver with FEC eliminates the BER floor for the three-, four- and five-user cases. For the six-user case, the RS(255, 239) decoder is ineffective due to the high BER at the input ( $\sim 10^{-3}$ ). The input BER at which the decoder started to be effective was approximately  $10^{-4}$ . At a BER of  $10^{-9}$ , the coding gain for the one- and two-user cases is roughly 3 dB, as predicted by theory. The theoretical results were calculated with [7]

$$P_{S\_FEC} \approx \frac{1}{2^m - 1} \sum_{j=t+1}^{2^m - 1} j \binom{2^m - 1}{j} P_S^j (1 - P_S)^{2^m - 1 - j} \quad (1)$$

where  $P_{S\_FEC}$  and  $P_S$  are the symbol error probabilities after and before decoding, respectively,  $m$  is the number of bits per symbol (eight in this case), and  $t$  is the error correction capability of the RS(255, 239) code. Under the assumption of purely random bit errors

$$P_S = 1 - (1 - P_B)^m \quad (2)$$

where  $P_B$  is the channel BER without FEC as measured in Fig. 3(a) for the recovered clock case. Finally, the upper and lower bounds in Fig. 3(b) are calculated using (1) and

$$P_{B\_FEC} = P_{S\_FEC} \times \frac{n}{m} \quad (3)$$

where  $n$  takes a value of 8 or 1 errors/symbol for the upper and lower bounds, respectively. As we can see in Fig. 3(b), the experimental results lie within the upper and lower bounds. The agreement between experimental and theoretical results allows us to draw the conclusion that the errors are statistically independent in our 2-D  $\lambda - t$  OCDMA network, without having to introduce an interleaver.

## V. CONCLUSION

We demonstrated a standalone receiver for 2-D  $\lambda - t$  OCDMA. The receiver provides MAI rejection, CDR, automatic detection of the payload chips, RZ-to-NRZ conversion, framing, and FEC decoding. We showed that the BER penalty is low when using the recovered clock instead of the global clock. Moreover, the FEC functionality of the receiver eliminated a BER floor and increased from two to five the number of simultaneous users that can be tolerated in the detection window.

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