Digilent XC2-XL System Board Reference Manual

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Overview

The Digilent XC2-XL is self-contained circuit development platform that contains a Xilinx CoolRunner-II XC2C256 CPLD and a Xilinx XC9572XL CPLD. The XC2-XL is an ideal platform for CPLD-based circuit design using the latest Xilinx CAD tools. It provides a JTAG programming circuit, power supplies, a clock source, and basic I/O devices, so that circuits can be implemented immediately without the need for any other components. All CPLD signals are brought to expansion connectors, allowing accessory circuits to be constructed in the on-board prototype area, or attached via an expansion board. The XC2-XL is compatible with all versions of Xilinx CAD tools, including the free WebPack tools available at the Xilinx website. XC2-XL features include:

- A Xilinx CoolRunner-II XC2C256 CPLD in a TQ144 package;
- A Xilinx XC9572XL CPLD in a VQ44 package;
- JTAG ports to both CPLDs that can be independently enabled or disabled;
- Flexible power delivery using a wall-plug transformer, batteries, or external supplies;
- A socketed oscillator (1.8432MHz included; clocks up to 100+MHz can be used);
- Full routing of all I/O signals from both CPLDs to expansion connectors;
- A button and two LEDs for basic I/O;
- Non-volatility – as with all Xilinx CPLDs, designs remain after power is removed.

Several expansion boards containing a variety of I/O devices are available for the XC2-XL. These fully assembled and tested boards can be used to quickly and easily enhance the features of the XC2-XL. See the Digilent website at www.digilentinc.com/xc2xl for more information.

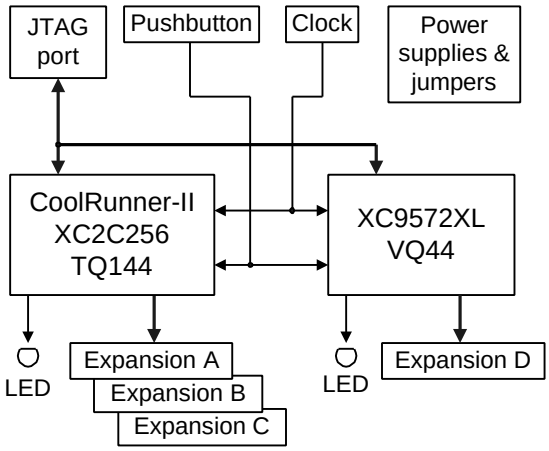

Figure 1. XC2-XL circuit board block diagram

Functional Description

The XC2-XL provides a minimal system that can be used to rapidly implement CPLD-based circuits, and to gain exposure to Xilinx CAD tools and CPLD-oriented design methods. The XC2-XL provides only the essential circuits needed to support the CPLDs, including power supplies, a clock source, and basic I/O (a pushbutton and two LEDs). All available I/O signals are routed to expansion connectors that mate with 40-pin, 100 mil spaced DIP headers available from several distributors.

The on-board power supplies and clock source can easily be disconnected from the CPLDs so that external power and clock signals can be used. Power supply design and decoupling follow recommended design practices, so the XC2-XL has stable, low noise supplies regardless of the power source used.

CPLD programming is accomplished via a 6-pin, 3.3V JTAG programming header that is

compatible with a variety of cables, including the JTAG3 cable from Digilent, the Parallel-3 or –4 cables from Xilinx, as well as cables from other vendors.

The XC2-XL measures 5.25" x 5.25", and it contains an 18-hole x 46-hole wire wrap area. The wire-wrap area can accommodate a self-adhesive solderless breadboard, allowing flexibility in accessory circuit construction.

Both CPLDs on the XC2-XL board are loaded with a sample configuration during board test. This basic configuration flashes the on-board LEDs at different rates that are selectable using the on-board button. This configuration, which can be downloaded from the Digilent or Xilinx websites, serves as a quick board check as well as a basic reference design.

Power Supplies

The CoolRunner-II requires three power supplies (V_{CORE}, V_{IO1}, and V_{IO2}), so the XC2-XL has three separate circuits for power delivery. The V_{CORE} and V_{IO1} supplies are routed only to the CoolRunner 2, and they are set to 1.8V and 3.3V respectively. V_{IO2} is routed to both CPLDs, and it is also set to 3.3V. V_{CORE} is generated from a 1.8V LM1117 LDO regulator that can supply up to 800mA of current. Jumper block JP3 allows V_{CORE} to be disconnected from the on-board regulator so that it can be brought in from an external supply. V_{IO1} and V_{IO2} both arise from the same 3.3V LM317 regulator that can supply up to 1.5A of current. Jumper-blocks JP2 and JP4 can disconnect V_{IO1} and V_{IO2} from the on-board regulators so that external I/O supplies can be used.

Jumper block JP1 selects whether V_{IO} is supplied from the 3.3V regulator, or from a source connected to J2. Regardless of the JP1 setting, the V_{CORE} regulator is used to generate the 1.8V supply. Jumper blocks JP2, JP3, and JP4 select whether V_{IO1}, V_{CORE}, and V_{IO2} are supplied from on-board or external supplies. The figure below shows the power supply routing and typical jumper settings.

Power can be supplied to the XC2-XL using any one of three modes. *Wall-plug* mode supplies power from any 5VCD-9VDC wall-plug-transformer supply connected to the power jack (J9) on the XC2-XL. The supply must source at least 250mA of current, and it must use a center-positive, 2.1mm ID/5.5mm OD connector. *Battery mode* supplies power from a battery pack (or other DC source) connected to the J2 header on the XC2-XL. The batteries must output between 2.8V and 3.6V. *External* mode uses the J8 header to bring regulated supplies from any external source. In the wall-plug mode, the V_{CORE} and V_{IO} regulators are used, so there is little chance of damaging the CPLDs by using incorrect supply voltages (both regulators can

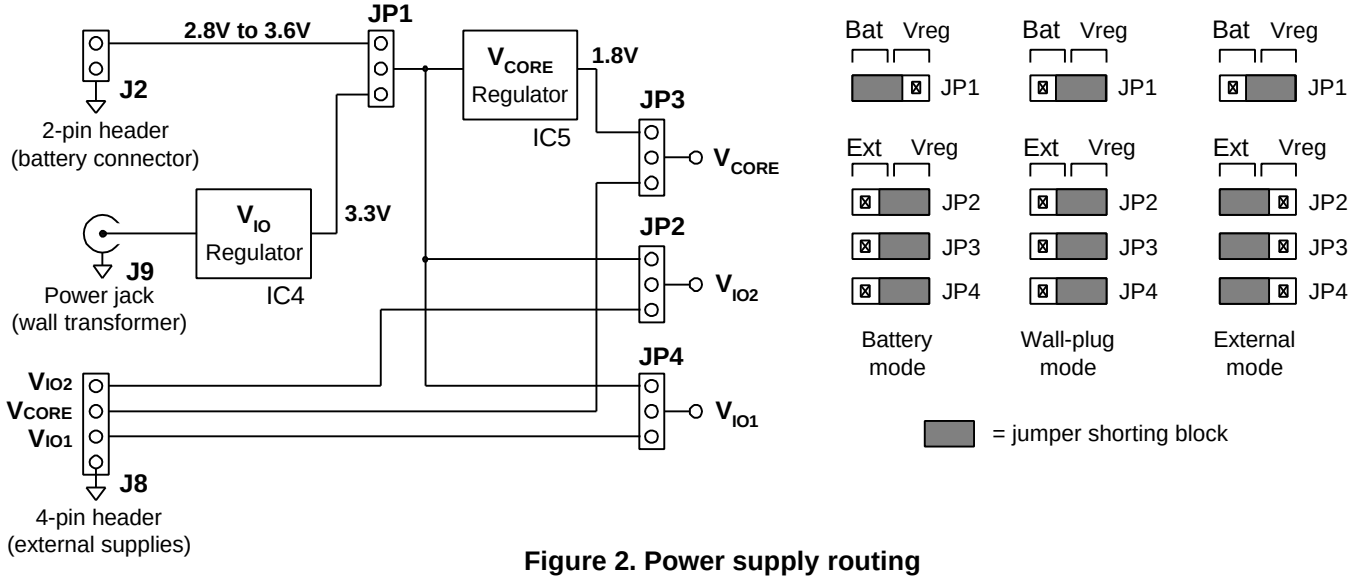

Figure 2. Power supply routing

handle up to 18VDC). In battery mode, the V_{CORE} regulator is used, but the supplied voltage directly drives the V_{IO} connections, so care must be taken to ensure no more than 3.8V is applied. In external mode, no regulators are used, so care must be taken to ensure CPLD voltage requirements are met.

CPLD Configuration

The CPLDs on the XC2-XL are connected in a JTAG scan chain as shown in the figure below. Either device can be removed from the chain by setting jumper blocks P5, JP6, JP9, and JP10 appropriately. The scan chain originates from a 6-pin header connector that is compatible with the JTAG3 cable from Digilent, and the P-3 and P-4 cables from Xilinx.

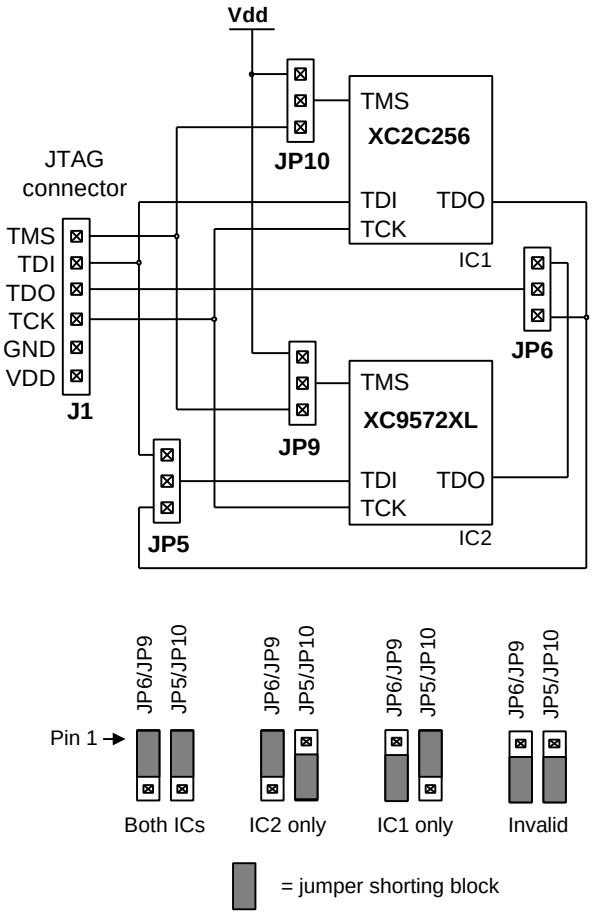

Figure 3. JTAG signal routing

Oscillator

The XC2-XL uses a half-size 8-pin DIP oscillator in an 8-pin socket. The board ships with a 1.842MHz oscillator, but oscillators from 32KHz to 100MHz can be used. The oscillator is connected to the GCK2 input on both CPLDs. It is bypassed with a 0.047uF capacitor, and it is as close to the CPLDs as possible.

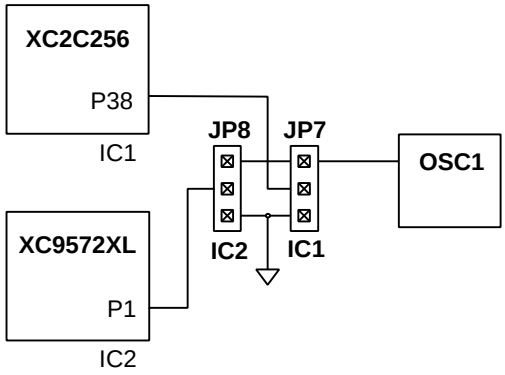

Figure 4. Clock signals

PushButton and LEDs

A pushbutton and two LEDs provide basic I/O functions on the XC2-XL. The LED can be illuminated to verify that configuration has been successful, or flashed at a given rate to indicate a particular status. The pushbutton can be used to provide a basic reset function, or to select an operating mode. The pushbutton drives the GSR input on both CPLDs, and the LED is driven from a general I/O pin.

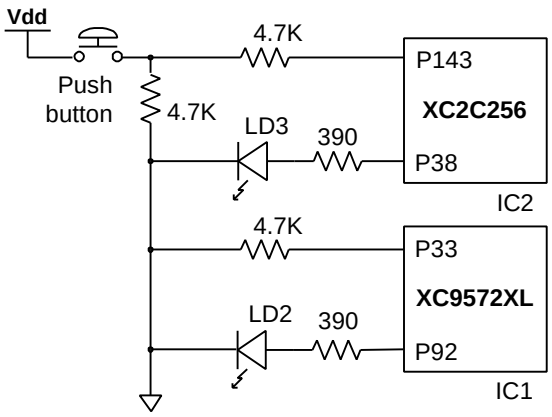

Figure 5. Pushbutton and LEDs

Expansion Connectors

Four expansion connectors have been provided to allow XC2 designs to be expanded on the included prototype area, or by attaching peripheral boards. The connectors use 2 x 20, 100-mil spaced right-angle sockets so that standard headers can be used on peripheral boards. Several Digilent expansion boards can be used with the XC2-XL, including solderless breadboards, wire-wrap boards, and analog and digital I/O boards. See Digilent's website at www.digilentinc.com/xc2xl for more information on available expansion boards.

All available signals are routed from the two CPLDs to the connectors as shown in the figure below. VCC (3.3V regulated), VU (depends on power supply used), and GND are also routed to the connector so that attached devices can draw power from the XC2-XL board. If the 3.3V regulated supply is used, no more than 1.5A should be drawn. Table 1 below shows XC2-XL expansion connector pinouts.

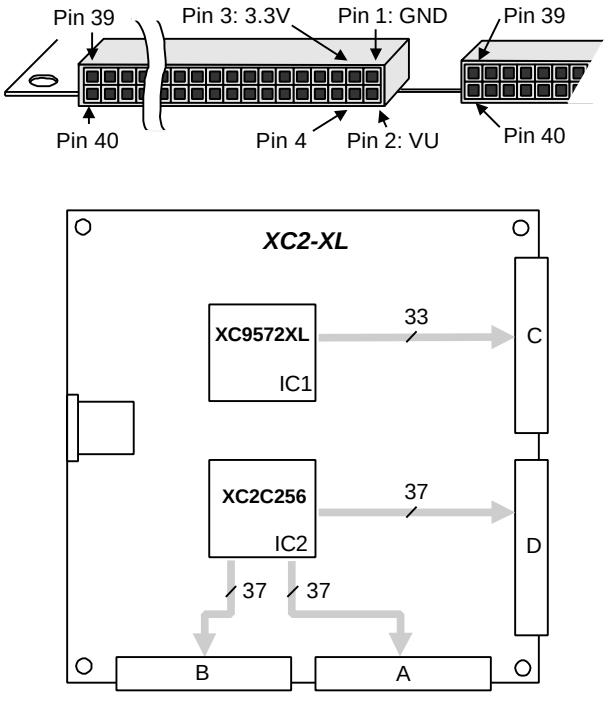

Figure 5. Expansion Connectors

CPLDs

The XC2-XL contains a Xilinx XC2C256 CoolRunner II CPLD in a TQ144 package, and an XC9572 CPLD in a VQ44 package. Both CPLDs have a clock source, pushbutton input, LED output, and connections to the JTAG programming signals. Other than these connections, all I/O signals are routed to the expansion connectors. CPLD pinouts are provided in tables 2 and 3 below.

The CPLDs can be programmed using the Xilinx ISE/WebPack software and the JTAG3 cable from Digilent (the P-3 or P-4 programming cable from Xilinx can also be used).

Please see the data sheets for the CPLDs available at the Xilinx web site for more information.

Table 1. XC2-XL board expansion connector pinouts												
A connector (J3)			B connector (J4)			C connector (J5)			D connector (J6)		
Pin	Signal	CR2 pin	Pin	Signal	CR2 pin	Pin	Signal	XC95 pin	Pin	Signal	CR2 pin
1	GND	-	1	GND	-	1	GND	-	1	GND	-
2	VU	-	2	VU	-	2	VU	-	2	VU	-
3	VDD33	-	3	VDD33	-	3	VDD33	-	3	VDD33	-
4	A4	43	4	B4/GSR	143	4	C4/LD3	44	4	D4	91
5	A5	42	5	B5	142	5	C5	43	5	L5	88
6	A6	41	6	B6	140	6	C6	42	6	D6	87
7	A7	39	7	B7	139	7	C7	41	7	D7	86
8	A8	40	8	B8	138	8	C8	40	8	D8	85
9	XCCLK	38	9	B9	137	9	C9	39	9	D9	83
10	A10	34	10	B10	136	10	C10	38	10	D10	82
11	A11	35	11	B11	135	11	C11	37	11	D11	81
12	A12	33	12	B12	134	12	C12	36	12	D12	80
13	A13	32	13	B13	133	13	C13	34	13	D13	79
14	A14	31	14	B14	132	14	C14/GSR	33	14	D14	78
15	A15	30	15	B15	131	15	C15	32	15	D15	77
16	A16	28	16	B16	130	16	C16	31	16	D16	76
17	A17	26	17	B17	129	17	C17	30	17	D17	75
18	A18	25	18	B18	128	18	C18	29	18	D18	74
19	A19	24	19	B19	126	19	C19	28	19	D19	71
20	A20	23	20	B20	125	20	C20	27	20	D20	70
21	A21	22	21	B21	124	21	C21	23	21	D21	69
22	A22	21	22	B22	121	22	C22	22	22	D22	68
23	A23	20	23	B23	120	23	C23	21	23	D23	66
24	A24	19	24	B24	119	24	C24	20	24	D24	64
25	A25	18	25	B25	118	25	C25	19	25	D25	61
26	A26	17	26	B26	117	26	C26	7	26	D26	60
27	A27	16	27	B27	116	27	C27		27	D27	59
28	A28	15	28	B28	115	28	C28		28	D28	58
29	A29	14	29	B29	114	29	C29		29	D29	57
30	A30	13	30	B30	113	30	C30	3	30	D30	56
31	A31	12	31	B31	112	31	C31	2	31	D31	54
32	A32	11	32	B32	111	32	XLCLK	1	32	D32	53
33	A33	10	33	B33	110	33	C33	18	33	D33	52
34	A34	9	34	B34	107	34	C34	16	34	D34	51
35	A35	7	35	B35	106	35	C35	14	35	D35	50
36	A36	6	36	B36	105	36	C36	13	36	D36	49
37	A37	5	37	B37	104	37	C37	12	37	D37	48
38	A38	4	38	B38	103	38	C38	8	38	D38	46
39	A39	3	39	B39	102	39	C39	6	39	D39	45
40	A40	2	40	B40	101	40	C40	5	40	D40	44

Table 2. XC2C256-TQ144 pinout							
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	**VCORE**	37	**VCORE**	73	**VIO1**	10	**VIO2**
2	A40	38	***XCCLK***	74	D18	11	B33
3	A39	39	A7	75	D17	11	B32
4	A38	40	A8	76	D16	11	B31
5	A37	41	A6	77	D15	11	B30
6	A36	42	A5	78	D14	11	B29
7	A35	43	A4	79	D13	11	B28
8	**VAUX**	44	D40	80	D12	11	B27
9	A34	45	D39	81	V18	11	B26
10	A33	46	D38	82	V16	11	B25
11	A32	47	**GND**	83	V14	11	B24
12	A31	48	D37	84	**VCORE**	12	B23
13	A30	49	D36	85	V13	12	B22
14	A29	50	D35	86	V12	12	**TDO**
15	A28	51	D34	87	V8	12	**GND**
16	A27	52	D33	88	V6	12	B21
17	A26	53	D32	89	**GND**	12	B20
18	A25	54	D31	90	**GND**	12	B19
19	A24	55	**VIO1**	91	V5	12	**VIO2**
20	A23	56	D30	92	***LD2***	12	B18
21	A22	57	D29	93	**VIO1**	12	B17
22	A21	58	D28	94	SCK	13	B16
23	A20	59	D27	95	SDO	13	B15
24	A19	60	D26	96	SDI	13	B14
25	A18	61	D25	97	C32	13	B13
26	A17	62	**GND**	98	V2	13	B12
27	**VIO1**	63	**TDI**	99	**GND**	13	B11
28	A16	64	D24	10	V3	13	B10
29	**GND**	65	**TMS**	10	B40	13	B9
30	A15	66	D23	10	B39	13	B8
31	A14	67	**TCK**	10	B38	13	B7
32	A13	68	D22	10	B37	14	B6
33	A12	69	D21	10	B36	14	**VIO2**
34	A10	70	D20	10	B35	14	B5
35	A11	71	D19	10	B34	14	***BTN***
36	**GND**	72	**GND**	10	**GND**	14	**GND**

Table 3. XC9572XL-VQ44 pinout							
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	***XLCLK***	12	C37	23	C21	34	C13
2	C31	13	C36	24	**TDO**	35	**VCORE**
3	C30	14	C35	25	**GND**	36	C12
4	**GND**	15	**VCORE**	26	**VIO**	37	C11
5	C40	16	C34	27	C20	38	C10
6	C39	17	**GND**	28	C19	39	C9
7	C26	18	C33	29	C18	40	C8
8	C38	19	C25	30	C17	41	C7
9	**TDI**	20	C24	31	C16	42	C6
10	**TMS**	21	C23	32	C15	43	C5
11	**TCK**	22	C22	33	***BTN***	44	***LD3***