Receiver for 2D λ-t OCDMA with Quantizer, CDR and FEC

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Abstract *We demonstrate experimentally the impact of forward-error correction on the performance of 2D λ-t OCDMA with no global clock. A receiver with clock recovery and Reed-Solomon decoding more than doubles the number of supported users.*

Introduction

The attractions of code-division multiplexing lie in the asynchronous, completely decentralized and uncoordinated transmissions among users. Bit rates considered moderate by optical standards (155 Mb/s and 622 Mb/s) are more than sufficient to meet the requirements for video and data delivery for the first generation of fiber to the home. The soft capacity of a code-division multiple access (CDMA) system permits growing the client base beyond the nominal maximum capacity (while accepting some quality of service degradation) without extensive upgrades to the infrastructure.

Practical considerations such as imperfect clock recovery and the efficiency of forward error correction (FEC) are required to give system designers accurate estimates of the quality of service guarantees that can be delivered, while still providing margin for exploiting the soft capacity. Note that TDMA systems proposed for current passive optical networks standards have hard capacity, and they require infrastructure upgrades to expand the client base.

In [1], FEC was used in a coherent optical CDMA (OCDMA) system, whereas in [2], FEC was used in a spectral amplitude coding OCDMA system. In this paper, we present FEC for a two-dimensional (2D) wavelength-time (λ-t) OCDMA system. Moreover, we present for the first time a complete, standalone OCDMA receiver that includes a quantizer to eliminate multiple access interference (MAI), a clock and data recovery (CDR) unit, and a FEC module. We address how soft capacity can be increased with the use of FEC while working with a recovered clock that provides practical, non-ideal sampling.

OCDMA system

The OCDMA setup is presented in Fig. 1. The desired information rate was 156.25 Mb/s. Since we use 8 chips per bit and a Reed-Solomon (RS) code introducing 15/14 of overhead [RS(255, 239)], we use a chip rate and a bit rate of 1.339 Gchip/s and 167.4 Mb/s, respectively. A broadband erbium doped fiber source is modulated by a polarization insensitive electro-absorption modulator (EAM). The modulating signal is a 2^{15}-1 pseudorandom binary sequence. The data is FEC-encoded in a return-to-zero (RZ) format. The modulated signal is amplified and sent to the

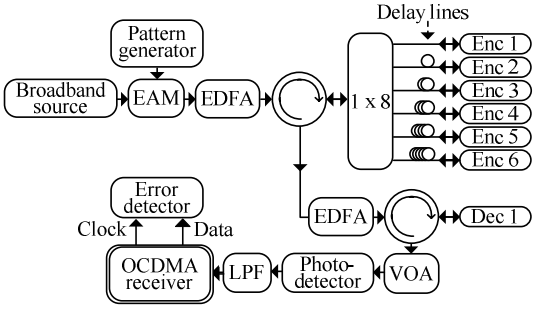

Fig. 1. Experimental setup. EAM: electro-absorption mod., VOA: variable-optical att., LPF: low-pass filter.

OCDMA encoders through an optical coupler. The encoders are preceded by optical delay lines to de-correlate their data. The OCDMA encoded signals are combined, amplified and sent to decoder 1. The optical power before the photo-detector is controlled with a variable optical attenuator (VOA). The output of the photo-detector is low pass filtered (LPF) by a 4th order Bessel-Thomson filter whose -3 dB cutoff frequency is 0.7 × chip rate, or 933 MHz. Such a filter reduces intensity noise from the incoherent broad-band source [3] while keeping inter-symbol interference to a minimum. Bit error rate (BER) measurements were performed on: 1) the RZ data sampled with a global clock (OCDMA receiver bypassed), and 2) the recovered non-return-to-zero (NRZ) data sampled with the recovered clock. In the second case, BER measurements were performed with and without RS decoding to study the impact of FEC. Each encoder in the system consists of eight fiber Bragg gratings (FBG) written in series, whose passbands and physical positions in the fiber determine the code. The FBG spectrums are 20 GHz wide and the channel spacing is 50 GHz. Code length and weight are 29 and 8, respectively. Encoder 2 has five common wavelengths with encoder 1, whereas encoders 3 to 5 have two and encoder 6 has a single wavelength in common. The delays between decoded user 1 and the five interferers are adjusted such that interfering wavelengths appear within the autocorrelation peak of user 1 (Fig. 2). This corresponds to a worst case scenario, thus allowing testing of the OCDMA receiver under severe conditions. The codes for encoders 1 to 6 are given in [4], in which they are labeled respectively as K, O, I, G, H, and C.

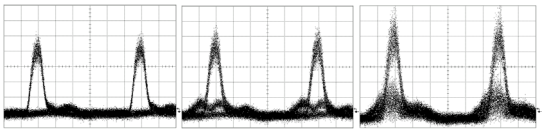

Fig. 2. Oscilloscope traces after LPF for one, two and six users respectively.

OCDMA receiver

The OCDMA receiver is shown in Fig. 3. The blocks outside of the dotted area correspond to the receiver that was used in [5, 6]. The quantizer (Q) applies a threshold on the incoming data in order to filter out MAI. The CDR recovers the clock at the chip rate for optimum sampling. In [5, 6], the deserializer was used for RZ to NRZ conversion, whereas here it is used to reduce the frequency of the data for further processing by digital logic. The blocks inside the dotted area, which were implemented on a Virtex II Pro FPGA from Xilinx, enhance the OCDMA receiver described in [5, 6] with automatic detection of the payload chips and RS(255, 239) decoding. The RZ to NRZ converter determines the index (0 to 7) of the payload chips. This process happens quickly after reset. Once the RZ to NRZ converter has identified the payload index, it remains locked on that index until the receiver is reset again. Only the payload chips make it through the RZ to NRZ converter, therefore dividing down the parallel data rate by eight. Hence, the operating frequency of the comma detector, the framer, and the decoder is around 21 MHz (1.339 GHz/8/8). This frequency is easily supported by most FPGAs. Upon reset, the comma detector looks for a preprogrammed comma – a unique 16-bit character. The framer uses the comma to realign the data. The realigned data is then sent to the RS decoder, which either outputs decoded or undecoded data as selected by the operator. The 8:1 serializer finally performs a parallel-to-serial conversion to output NRZ data at 167.4 Mb/s (chip rate/number of chips per bit).

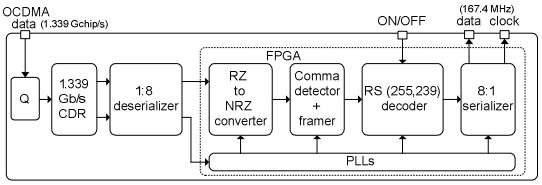

Fig. 3. Block diagram of the OCDMA receiver. The blocks within the dotted area were implemented on an FPGA. Q: quantizer, RS: Reed-Solomon, PLL: phase-locked loop.

Results and discussion

The performance of the OCDMA system with the global clock (solid lines, filled markers) and the recovered clock (solid lines, empty markers) is shown in Fig. 4. The results were obtained with worst case MAI and no FEC. Note that the abscissa is the useful power, i.e., the optical power contributed by the desired user at the photodiode. When sampling with the recovered clock, we observe no appreciable power penalty compared to the global clock case. This result is an improvement over the result obtained in [6], where a power penalty of 3.3 to 3.5 dB was measured at a BER of 10^{-9}. The improvement is due to a sampling optimization. In this work, the CDR operates at the chip rate; in [6], the CDR was operating at twice the chip rate due to the unavailability of a 1:8 deserializer for RZ to NRZ conversion. The chips were therefore sampled on each side of the optimum sampling point, explaining the power penalty. Fig. 4 also shows the BER with FEC enabled (dashed lines). The system can support five users simultaneously in the detection window without error (compared to two users when FEC is disabled). The BER floor is eliminated for five users or less. At a BER of 10^{-9}, the coding gain for the one user case is roughly 3 dB.

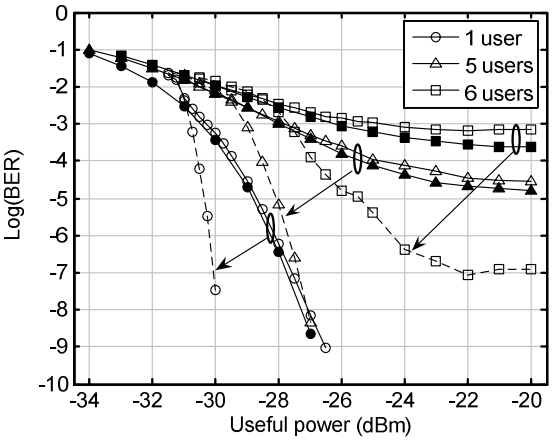

Fig. 4. BER with global clock (solid lines, filled markers), with recovered clock no FEC (solid lines, empty markers) and with recovered clock and FEC (dashed lines, empty markers).

Conclusions

We demonstrated experimentally that FEC can improve the soft-capacity of a 2D λ-t OCDMA network. No global clock was used in the system. Instead, we used a standalone OCDMA receiver with CDR, automatic detection of the payload chips, and RS decoding. In addition to filtering out MAI and recovering the clock, the receiver eliminated a BER floor and increased the maximum number of simultaneous users in the detection window from two to five.

References

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