MALVINO & BATES

Electronic PRINCIPLES

SEVENTH EDITION

Chapter 8

Transistor Biasing

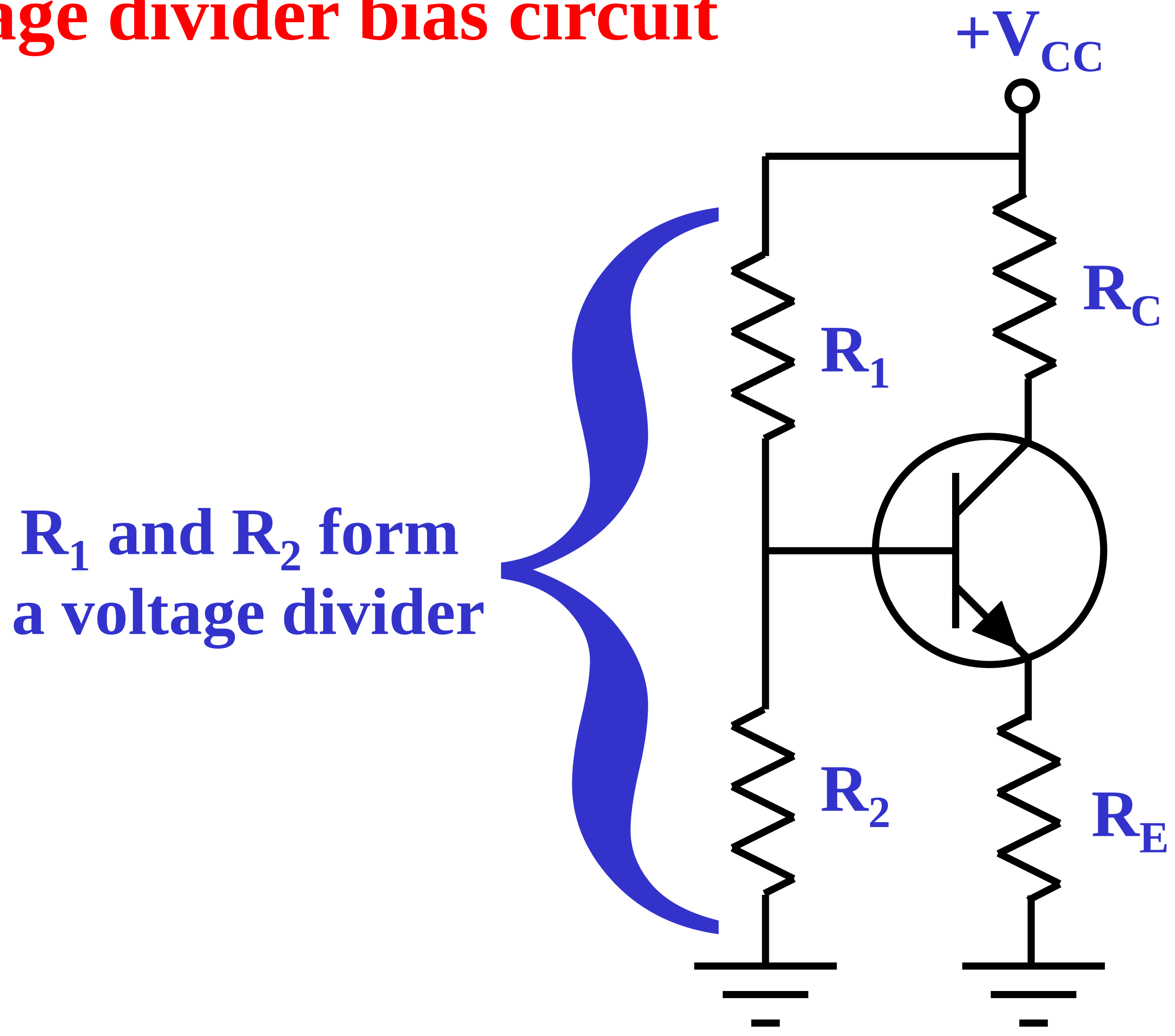
Topics Covered in Chapter 8

- Voltage-divider bias
- Accurate VDB analysis
- VDB load line and Q point
- Two-supply emitter bias
- Other types of bias
- Troubleshooting
- PNP transistors

Voltage divider bias

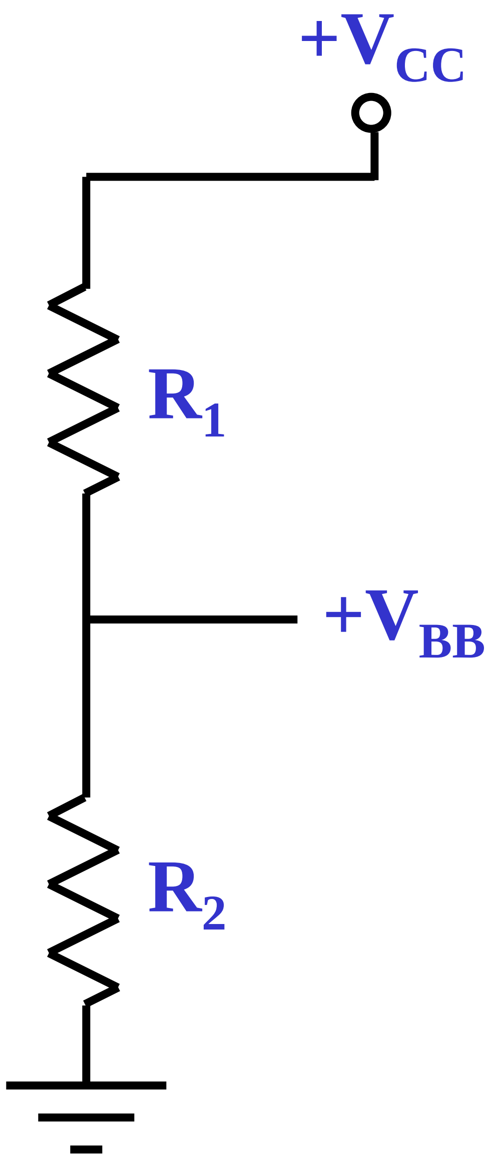
- Base circuit contains a voltage divider
- Most widely used
- Known as VDB

Voltage divider bias circuit



Divider analysis:

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$



ASSUMPTION: The base current is normally much smaller than the divider current.

Now the circuit can be viewed this way:

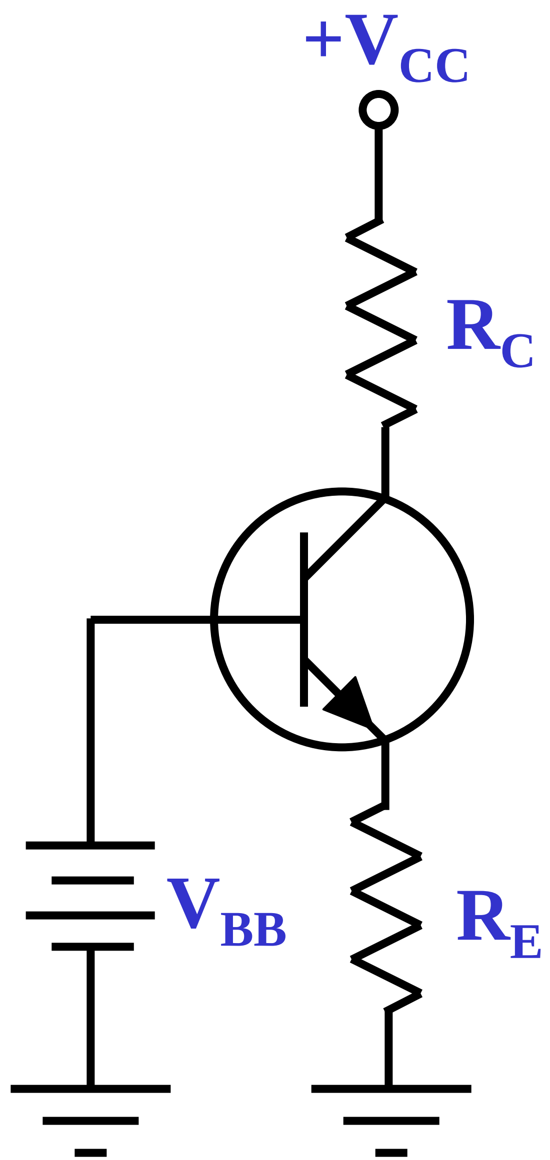
To complete the analysis:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E}$$

I_C @ I_E

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$



The six-step process

1. Calculate the base voltage using the voltage divider equation.
2. Subtract 0.7 V to get the emitter voltage.
3. Divide by emitter resistance to get the emitter current.
4. Determine the drop across the collector resistor.

The six-step process (Continued)

5. Calculate the collector voltage by subtracting the voltage across the collector resistor from V_{CC}.
6. Calculate the collector-emitter voltage by subtracting the emitter voltage from the collector voltage.

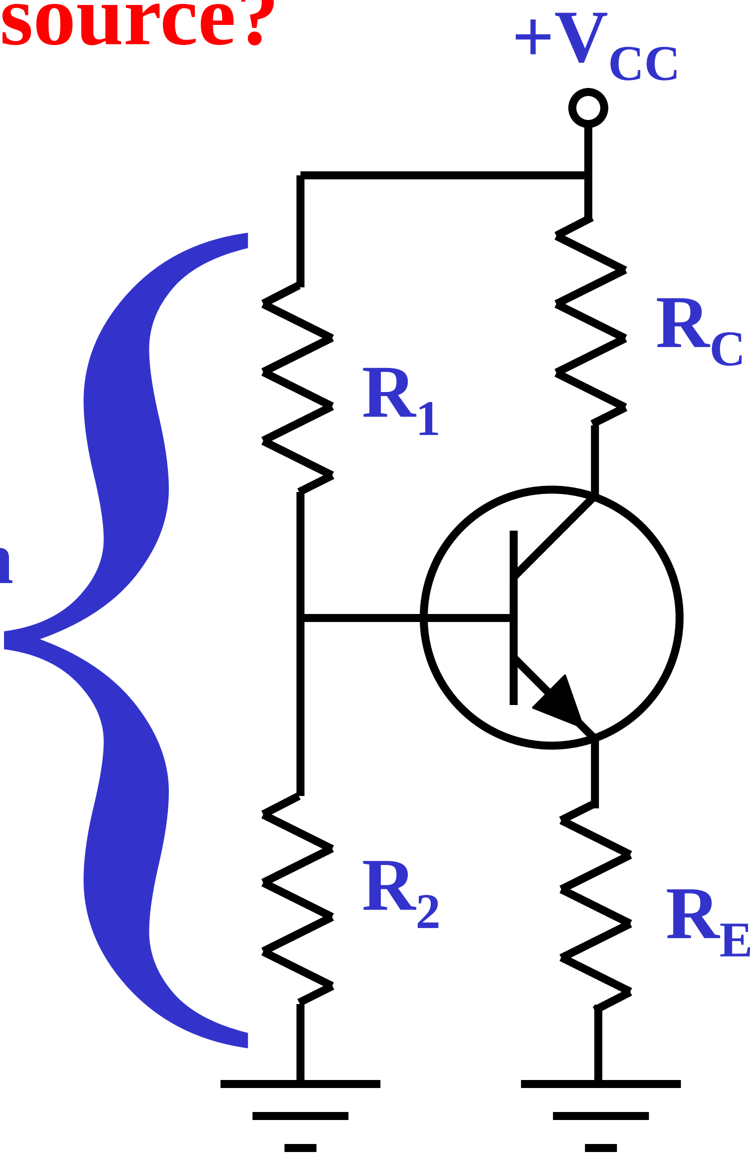
VDB analysis

- The base current must be much smaller than current through the divider
- With the base voltage constant, the circuit produces a stable Q point under varying operational conditions

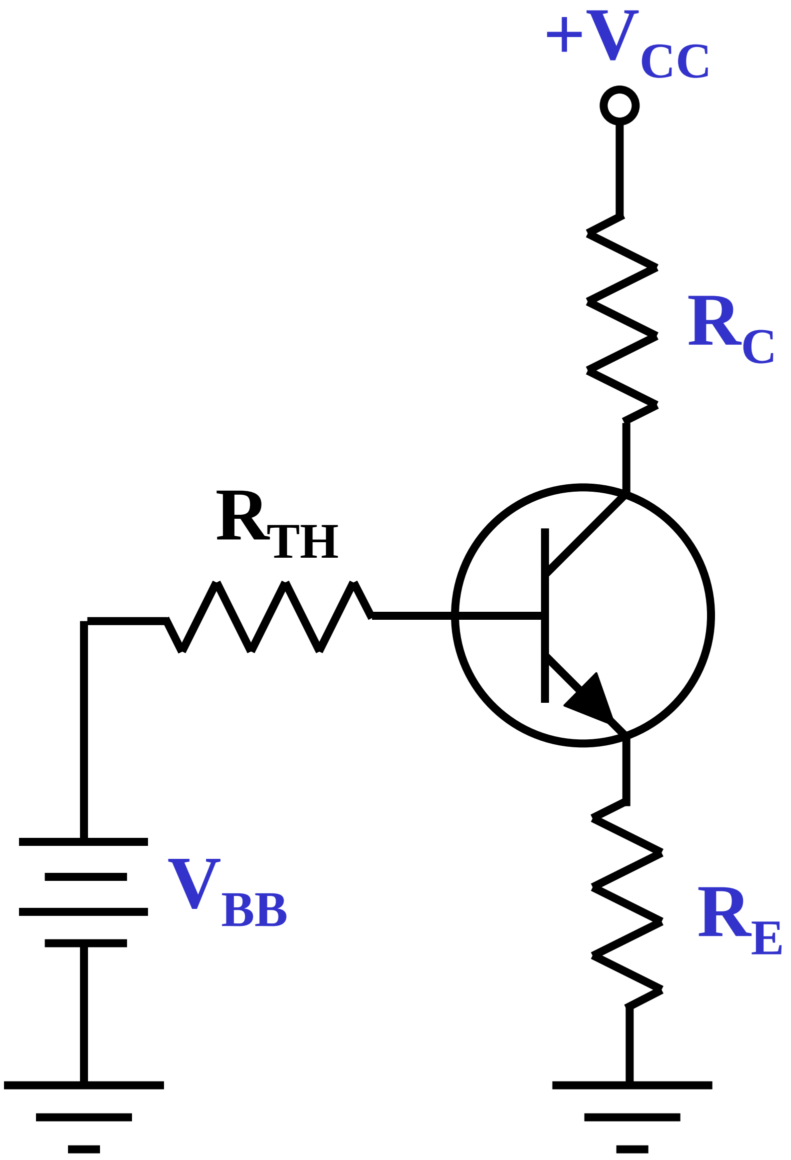
Is the divider a <u>stiff</u> source?

Find the Thevenin resistance.

$$R_{TH} = R_1 \| R_2$$

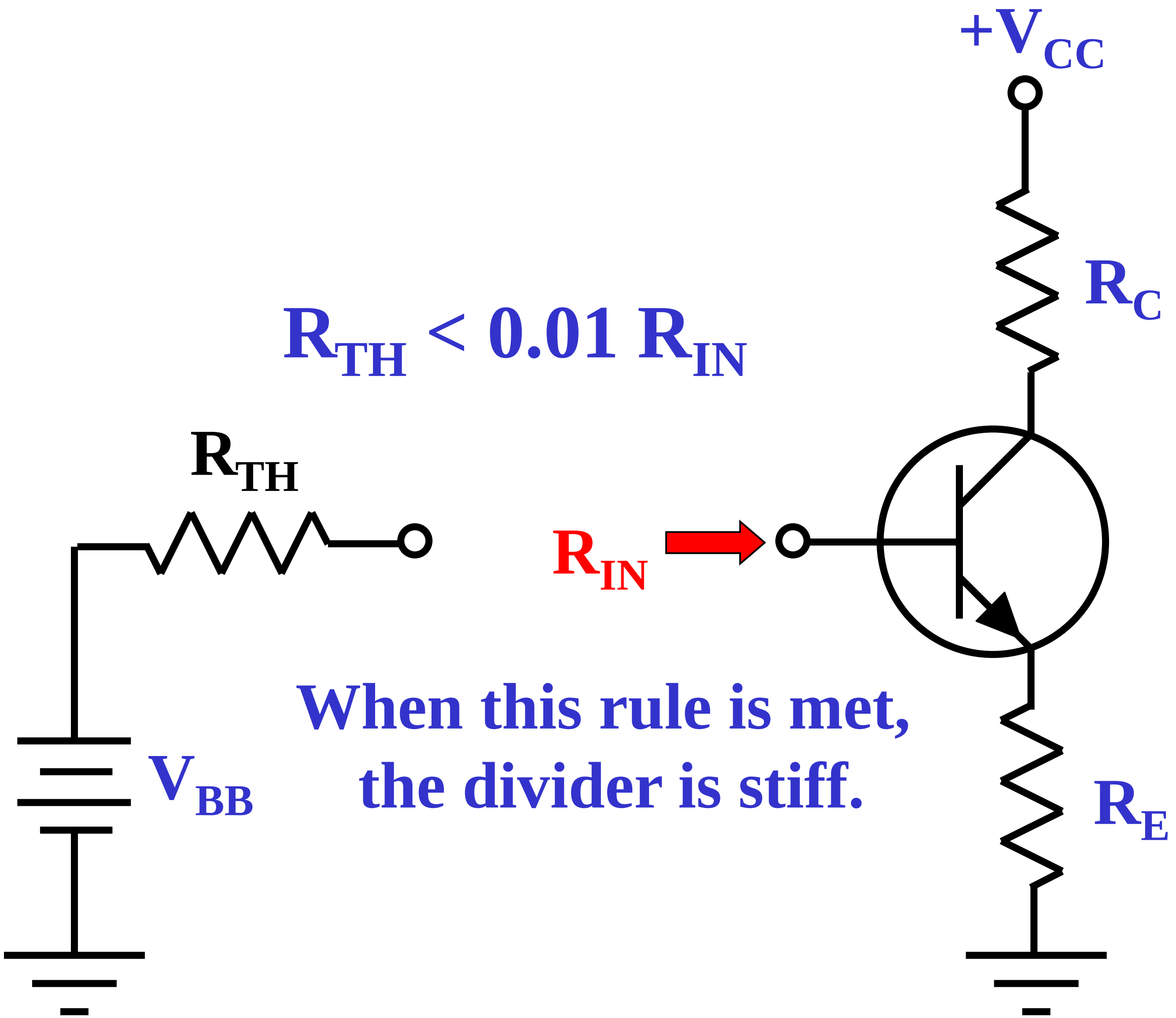


A Thevenin model of the bias circuit:



The 100:1 rule applied to the bias circuit:

$$R_{TH} < 0.01\ R_{IN}$$



**When this rule is met,
the divider is stiff.**

Firm voltage divider

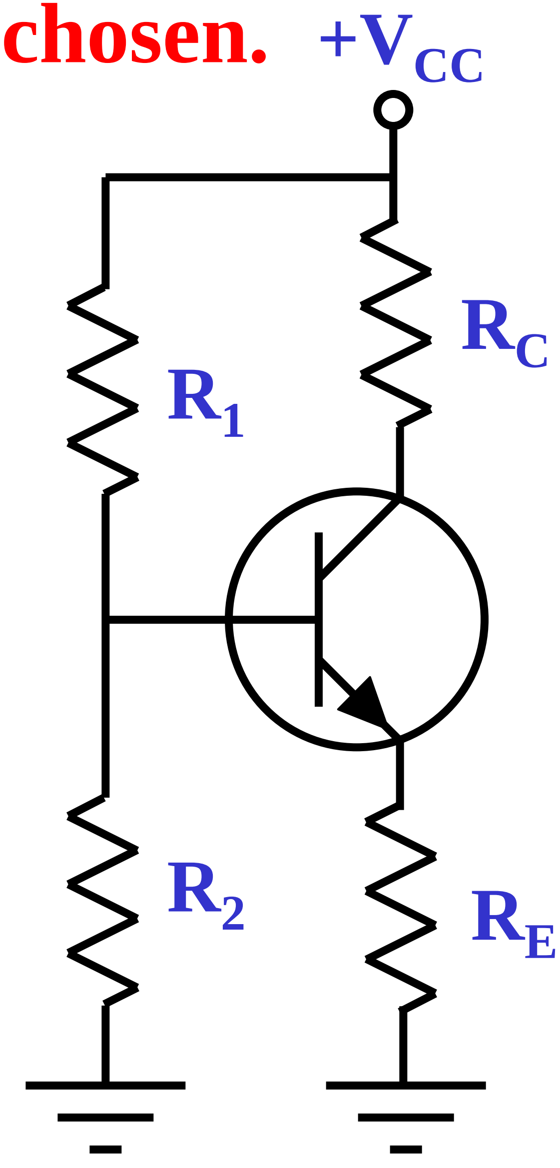
- **Used because divider resistors (e.g. R_1 and R_2) in a stiff design would be too small**
- **The <u>collector</u> current will be about 10% <u>lower</u> than the stiff value**

Sometimes a **firm divider** is chosen.

$$R_1 \| R_2 < 0.1\, b_{dc} R_E$$

A closer approximation:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \dfrac{R_1 \| R_2}{b_{dc}}}$$



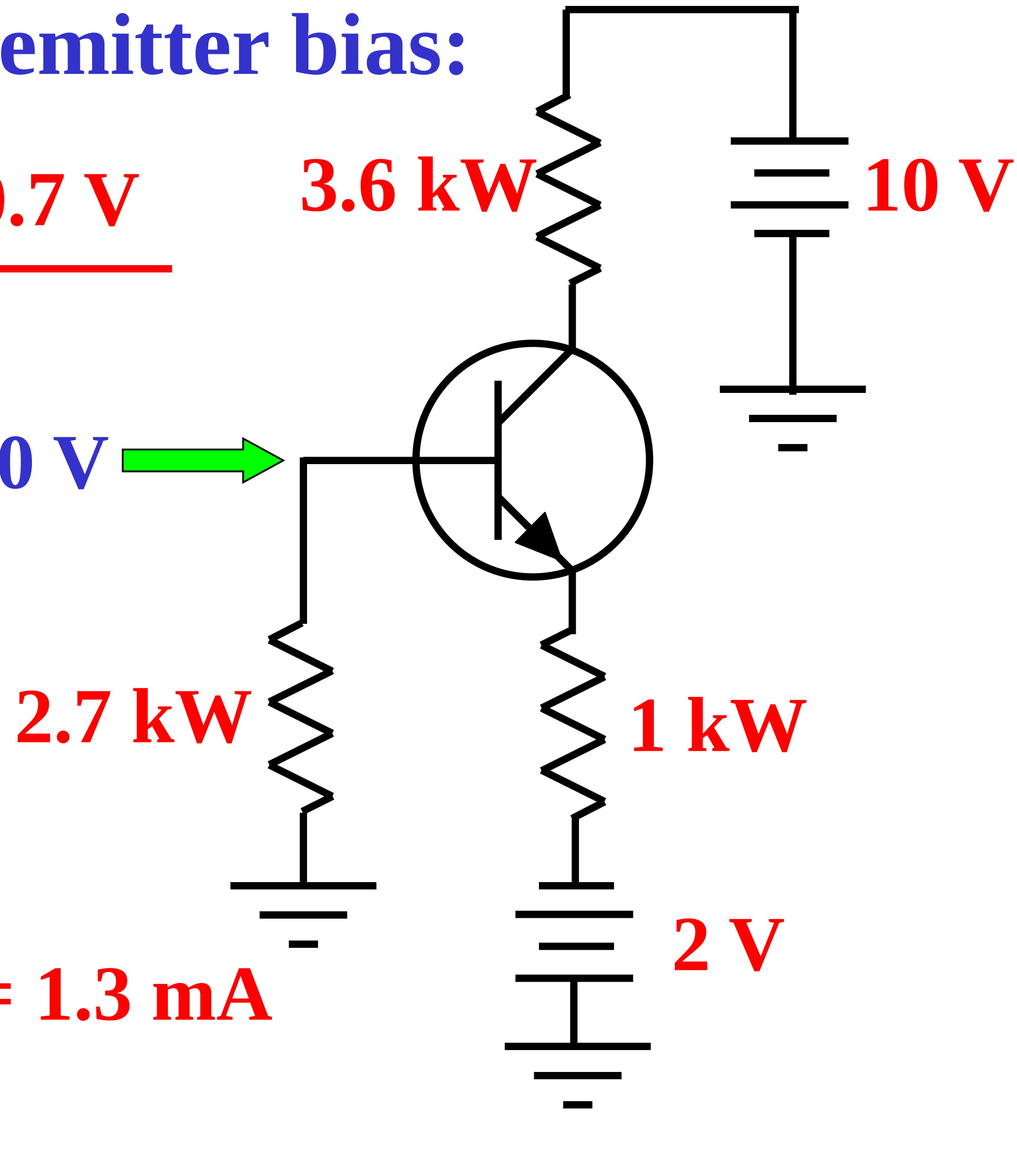
VDB load line and Q point

- VDB is derived from emitter bias
- The Q point is immune to changes in current gain
- The Q point is moved by varying the emitter resistor

Two-supply stiff emitter bias:

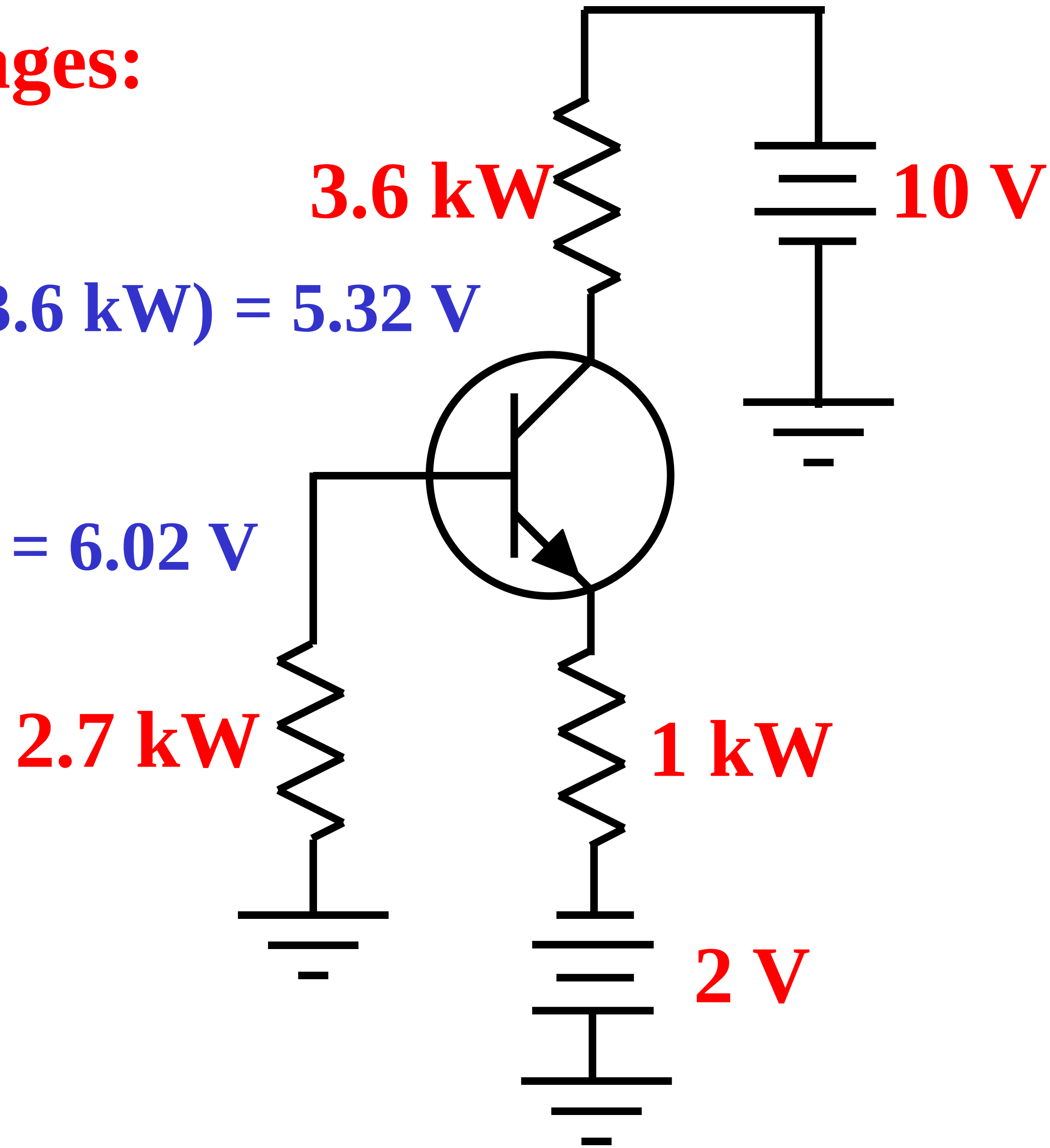
$$I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E}$$

Assume 0 V



$$I_E = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ kW}} = 1.3\text{ mA}$$

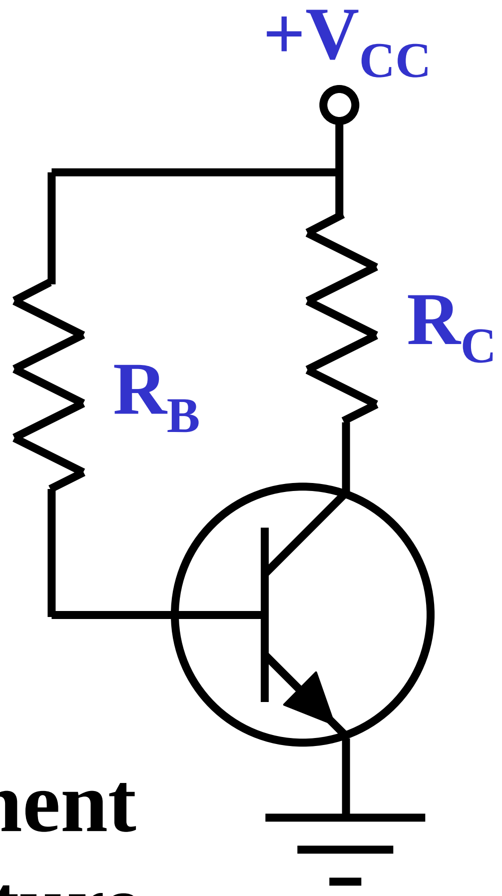
Find the voltages:



V_C = 10 V - (1.3 mA)(3.6 kW) = 5.32 V

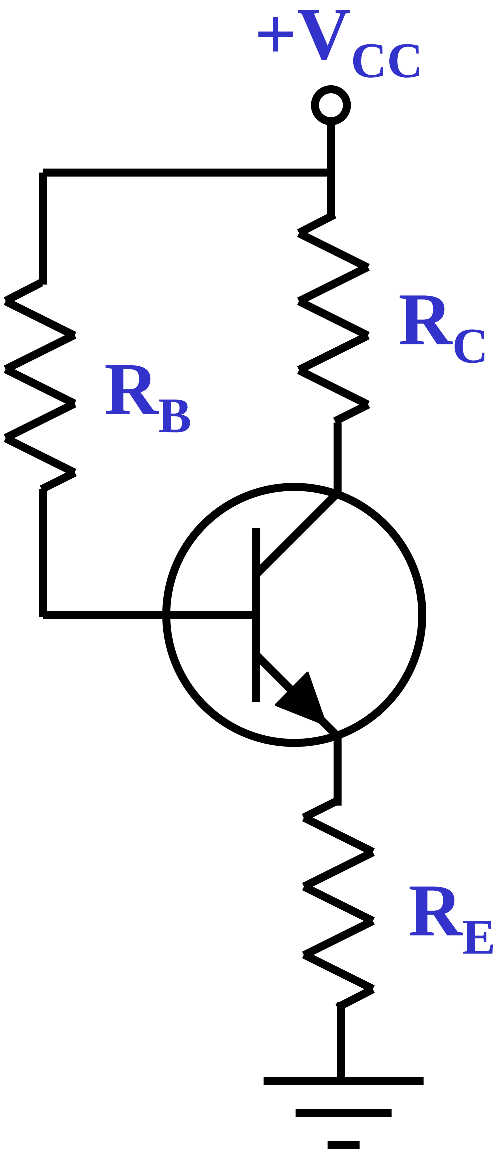
V_{CE} = 5.32 V - (-0.7 V) = 6.02 V

Base bias:



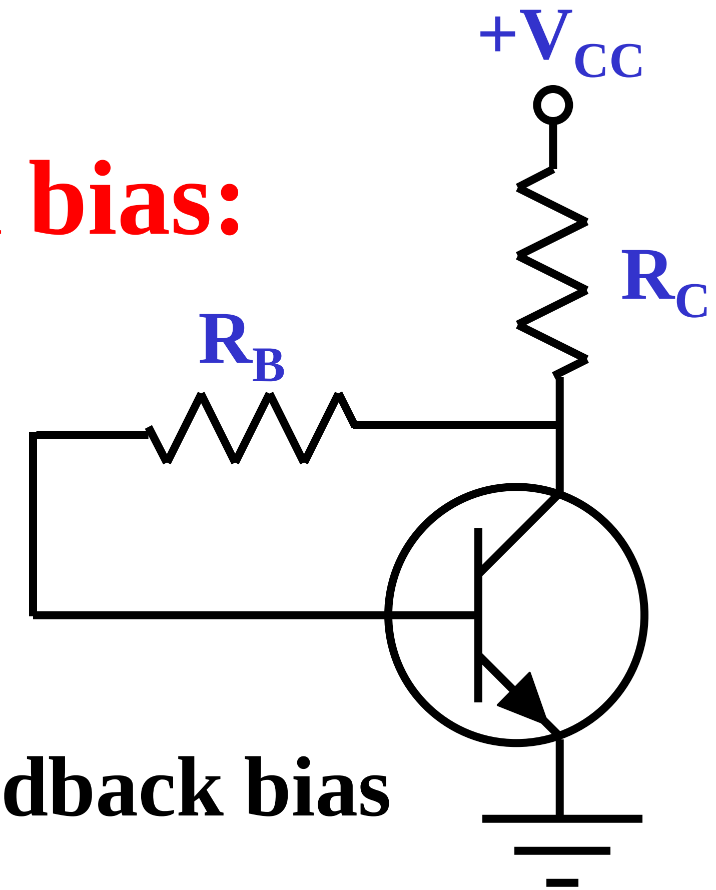
- The least predictable
- Q point moves with replacement
- Q point moves with temperature
- Not practical

Emitter-feedback bias:



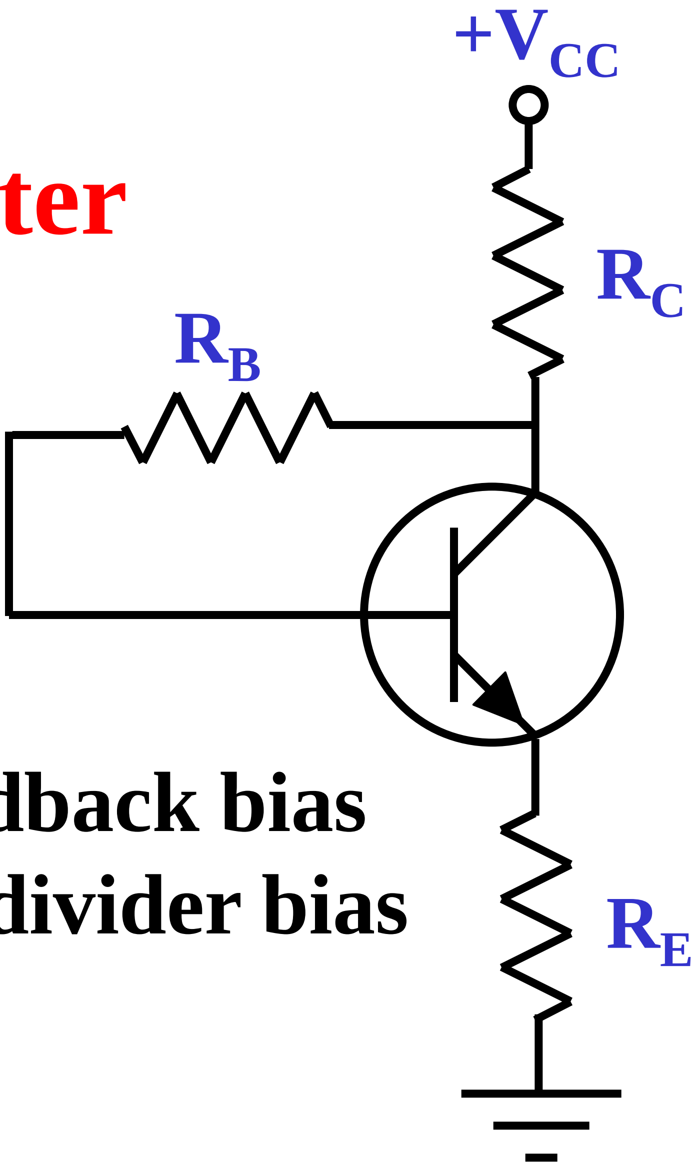
- Better than base bias
- Q point still moves
- Not popular

Collector-feedback bias:



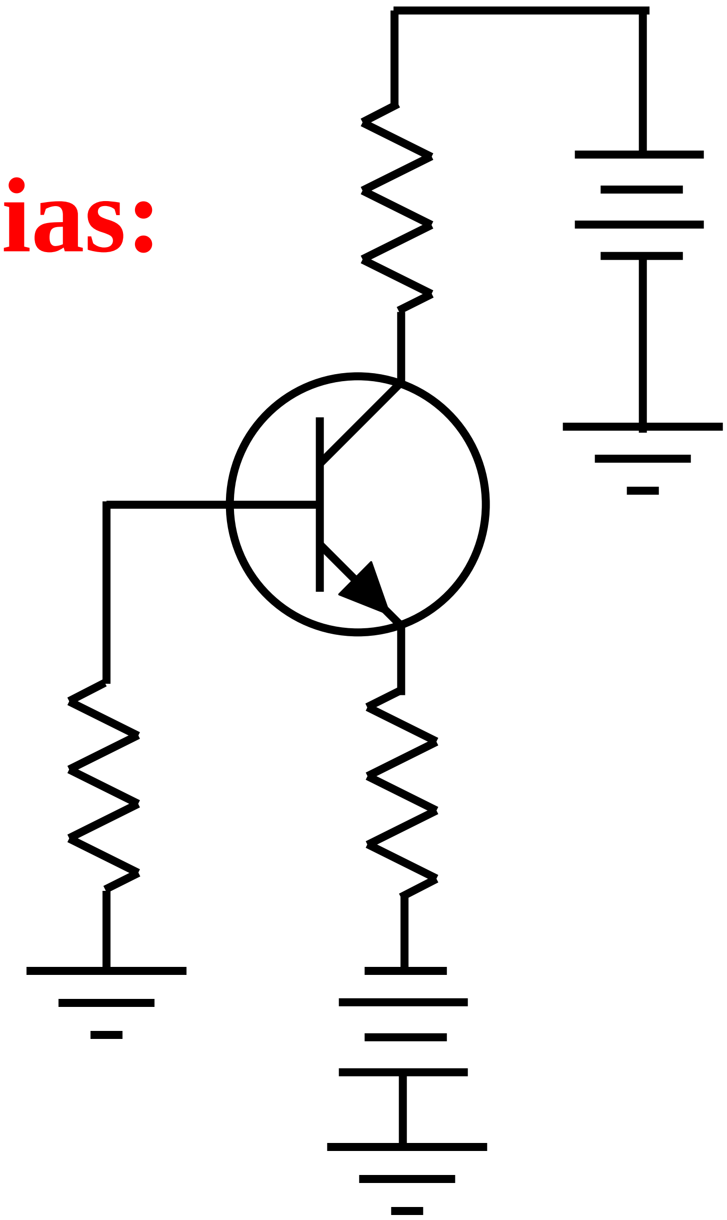
- Better than emitter-feedback bias
- Q point still moves
- Some applications because of circuit simplicity

Collector- and emitter -feedback bias:



- Better than emitter-feedback bias
- Not as good as voltage-divider bias
- Limited application

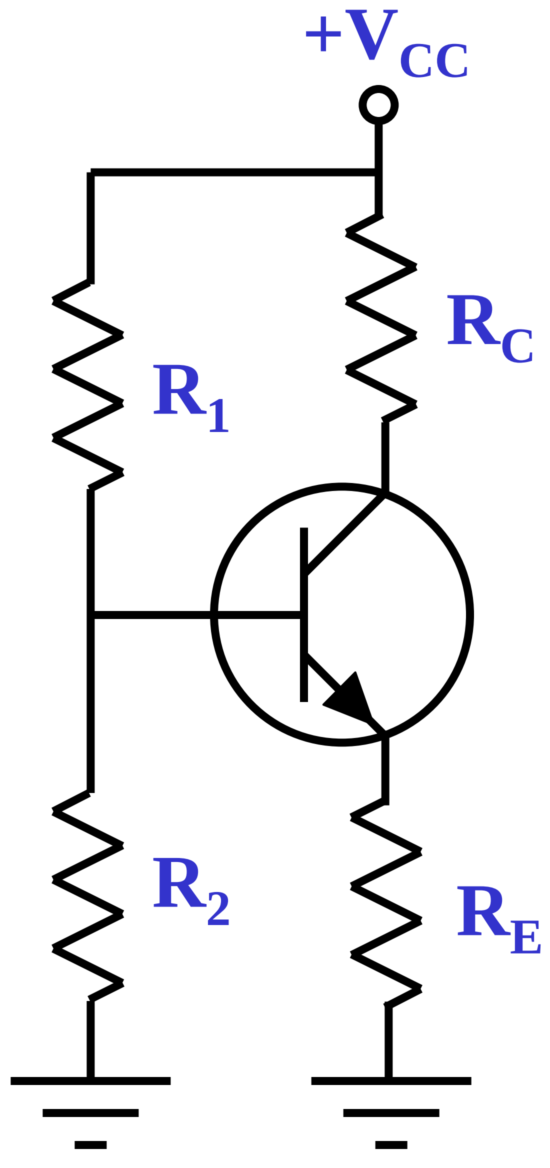
Two-supply emitter bias:



- Very stable
- Requires 2 supplies

Note: Also called TSEB

Voltage divider bias:



- Very stable
- Requires 1 supply
- The most popular

Note: Also called VDB

Troubleshooting

- **Voltage measurements**
- **Use 10 MΩ input voltmeter**
- **Troubles include:**

ü **Opens**

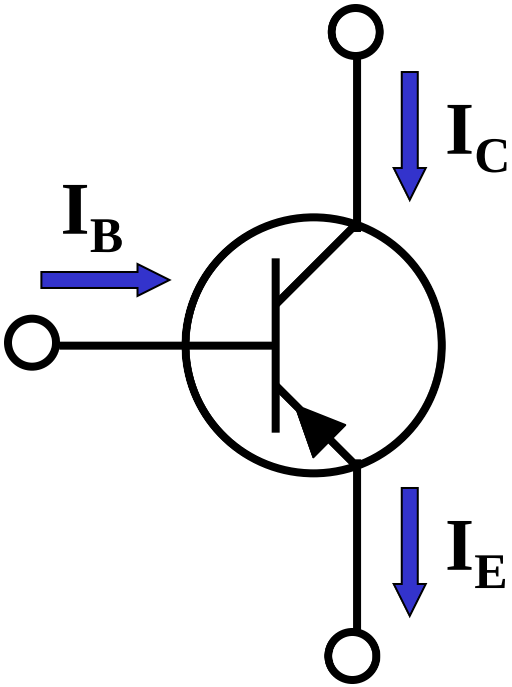
ü **Shorts**

ü **Faulty transistors**

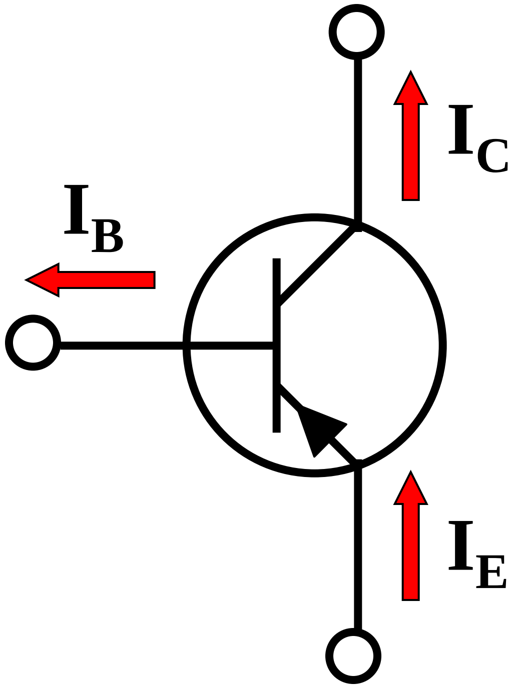
PNP transistor

- The base is n-type material
- The collector and emitter are p-type material
- The emitter arrow points in
- Can be used with a negative power supply

PNP transistor symbol and current flow

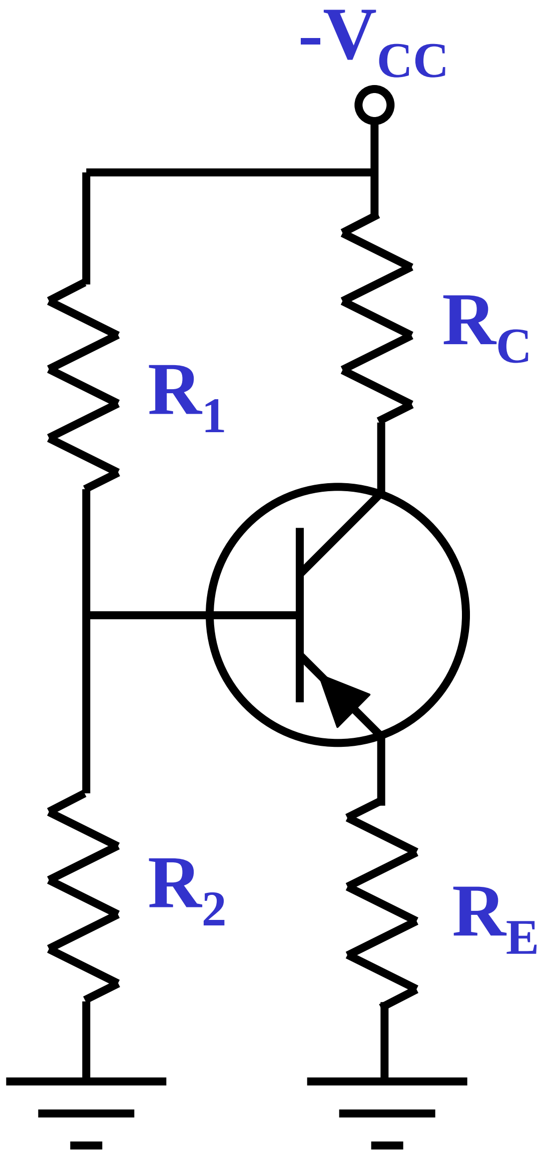


Electron flow



Conventional flow

PNP Biasing with a negative supply



PNP Biasing with a <u>positive</u> supply