Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE432: VLSI Modeling and Design
Sheet 3 : Interconnects

1. Estimate the resistance per mm of a minimum pitch Cu wire for each layer in the Intel 45 nm process described in Table 6.1. Assume a 10 nm high-resistance barrier layer and negligible dishing.

Layer	*t* (nm)	*w* (nm)	*s* (nm)	pitch (nm)
M9	7 μm	17.5 μm	13 μm	30.5 μm
M8	720	400	410	810
M7	504	280	280	560
M6	324	180	180	360
M5	252	140	140	280
M4	216	120	120	240
M3	144	80	80	160
M2	144	80	80	160
M1	144	80	80	160

2. Consider a 5 mm-long, 4 λ-wide metal2 wire in a 0.6 μm process. The sheet resistance is 0.08 Ω/□ and the capacitance is 0.2 fF /μm. Construct a 3-segment π-model for the wire.

3. A 10x unit-sized inverter drives a 2x inverter at the end of the 5 mm wire from Exercise 2. The gate capacitance is C=2 fF/μm and the effective resistance is R=2.5 kΩ·μm for nMOS transistors. Estimate the propagation delay using the Elmore delay model; neglect diffusion capacitance.

4. Find the best width and spacing to minimize the RC delay of a metal2 bus in the 180 nm process described in Figure 6.12 if the pitch cannot exceed 960 nm. Minimum width and spacing are 320 nm. First, assume that neither adjacent bit is switching. How does your answer change if the adjacent bits may be switching?

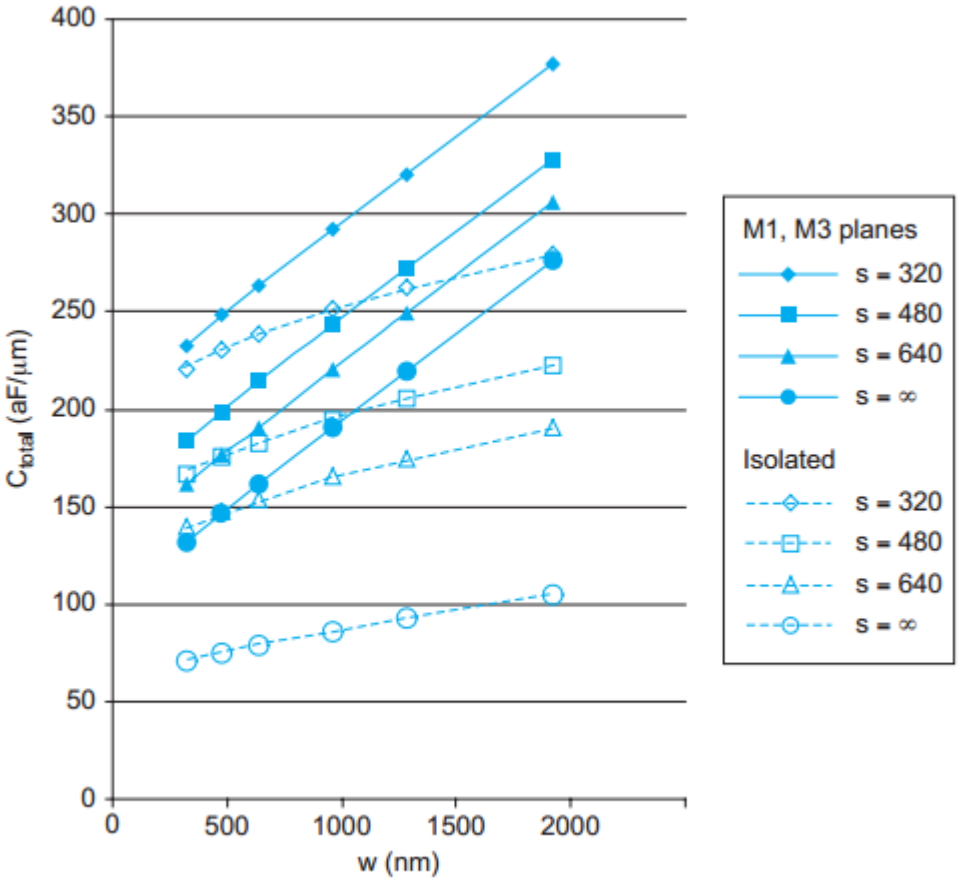

FIGURE 6.12 Capacitance of metal2 line as a function of width and spacing

5. Derive EQ (6.27)–(6.30). Assume the initial driver and final receiver are of the same size as the repeaters so the total delay is N times the delay of a segment.

$$\frac{l}{N} = \sqrt{\frac{2RC\left(1+p_{\text{inv}}\right)}{R_w C_w}} \qquad \textbf{(6.27)}$$

$$\frac{l}{N} = 0.77\sqrt{\frac{\text{FO4}}{R_w C_w}} \qquad \textbf{(6.28)}$$

$$\frac{t_{pd}}{l} = \left(2+\sqrt{2\left(1+p_{\text{inv}}\right)}\right)\sqrt{RCR_w C_w} \approx 1.67\sqrt{\text{FO4}\, R_w C_w} \qquad \textbf{(6.29)}$$

$$W = \sqrt{\frac{RC_w}{R_w C}} \qquad \textbf{(6.30)}$$

6. Revisit Exercise 6.5 using a pair of inverters (a non-inverting buffer) instead of a single inverter. The first inverter in each pair is W1 times unit width. The second is a factor of k larger than the first. Derive EQ (6.33)–(6.36).

$$\frac{l}{N} = \sqrt{\frac{2RC\left(k+\frac{1}{k}+2p_{\text{inv}}\right)}{R_w C_w}} \approx 1.22\sqrt{\frac{\text{FO4}}{R_w C_w}} \qquad \textbf{(6.33)}$$

$$\frac{t_{pd}}{l} = 1.81\sqrt{\text{FO4}\, R_w C_w} \tag{6.34}$$

$$W_1 = \frac{W}{\sqrt{k}}, \quad W_2 = W\sqrt{k} \tag{6.35}$$

$$\frac{E}{l} \approx 2.2 C_w V_{DD}^2 \tag{6.36}$$

7. Compute the characteristic velocity (delay per mm) of a repeated metal2 wire in the 180 nm process. A unit nMOS transistor has resistance of 2.5 kΩ and capacitance of 0.7 fF, and the pMOS has twice the resistance. Use the data from Figure 6.12. Consider both minimum pitch and double-pitch (twice minimum width and spacing) wires. Assume solid metal above and below the wires and that the neighbors are not switching.

8. Prove EQ (6.39).

$$C_i\left(R_{i-1} + R_{w_{i-1}}\right) = R_i\left(C_{i+1} + C_{w_{i+1}}\right) \tag{6.39}$$