Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE432: VLSI Modeling and Design
Sheet 2: Power

1. You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You are using a standard cell process with an average switching capacitance of 450 pF/mm^2. Estimate the dynamic power consumption of your chip if it has an area of 70 mm^2 and runs at 450 MHz at VDD=0.9 V.

2. You are considering lowering V_{DD} to try to save power in a static CMOS gate. You will also scale V_t proportionally to maintain performance. Will dynamic power consumption go up or down? Will static power consumption go up or down?

3. The stack effect causes the current through two series OFF transistors to be an order of magnitude less than I_{off} when DIBL is significant. Show that the current is $I_{off}/2$ when DIBL is insignificant (e.g., η=0). Assume γ=0, n=1.

4. Determine the activity factor for the signal shown in Figure 5.34. The clock rate is 1 GHz.

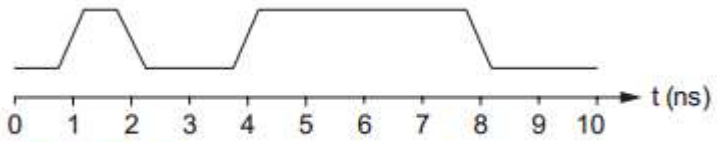

FIGURE 5.34 Signal for Exercise 5.4

5. Consider the buffer design problem from Example 4.14. If the delay constraint is 20 τ, how many stages will give the lowest energy, and how should the stages be sized?

6. Repeat Exercise 5 if the load is 500 rather than 64 and the delay constraint is 30 τ

7. Derive the switching probabilities in Table 5.1.

TABLE 5.1 Switching probabilities

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \overline{P}_A \overline{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\overline{P}_A \overline{P}_B$
XOR2	$P_A \overline{P}_B + \overline{P}_A P_B$

8. Design an 8-input OR gate with a delay of under 4 FO4 inverters. Each input may present at most 1 unit of capacitance. The load capacitance is 16 units. If the input probabilities are 0.5, compute the switching probability at each node and size the circuit for minimum switching energy.

9. Construct a table similar to Table 5.2 for a 2-input NOR gate.

Input State (ABC)	I_{sub}	I_{gate}	I_{total}	V_x	V_z
000	0.4	0	0.4	stack effect	stack effect
001	0.7	0	0.7	stack effect	$V_{DD} - V_t$
010	0	1.3	1.3	intermediate	intermediate
011	3.8	0	10.1	$V_{DD} - V_t$	$V_{DD} - V_t$
100	0.7	6.3	7.0	0	stack effect
101	3.8	6.3	10.1	0	$V_{DD} - V_t$
110	5.6	12.6	18.2	0	0
111	28	18.9	46.9	0	0

10. Design a header switch for a power gating circuit in a 65 nm process. Suppose the PMOS transistor has an ON resistance of about 2.5 kΩ· Rm. The block being gated has an ON current of 100 mA. How wide must the header transistor be to cause less than a 2% increase in delay?