Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE432: VLSI Modeling and Design
Sheet 1 : Delay

Part I - Stage delay:

1. Sketch a 2-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter. Compute the rising and falling propaga-tion delays of the NOR gate driving identical NOR gates using the Elmore delay model. Assume that every source or drain has fully contacted diffusion when making your estimate of capacitance.

2. Sketch a stick diagram for the 2-input NOR. Repeat Exercise 4.1 with better capac-itance estimates. In particular, if a diffusion node is shared between two parallel transistors, only budget its capacitance once. If a diffusion node is between two series transistors and requires no contacts, only budget half the capacitance because of the smaller diffusion area.

3. Find the worst-case Elmore parasitic delay of an n-input NOR gate.

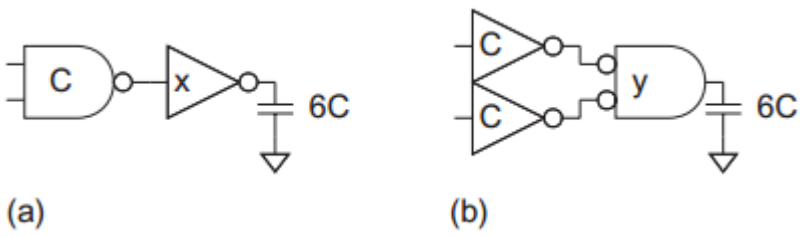
4. Sketch a delay vs. electrical effort graph like that of Figure 4.21 for a 2-input NOR gate using the logical effort and parasitic delay estimated in Section 4.4.2. How does the slope of your graph compare to that of a 2-input NAND? How does the y-intercept compare?

5. Suppose a unit inverter with three units of input capacitance has unit drive.
   a. What is the drive of a 4x inverter?
   b. What is the drive of a 2-input NAND gate with three units of input capacitance?

6. Sketch a 4-input NAND gate with transistor widths chosen to achieve equal rise and fall resistance as a unit inverter. Show why the logical effort is 6/3.

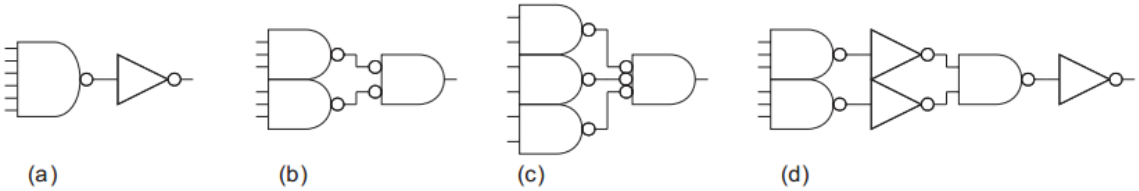
Part II - Path Delay:

1. Consider the two designs of a 2-input AND gate shown in Figure 4.39. Give an intuitive argument about which will be faster. Back up your argument with a calcu-lation of the path effort, delay, and input capacitances xand yto achieve this delay.



(a) (b)

2. Consider four designs of a 6-input AND gate shown in Figure 4.40. Develop an expression for the delay of each path if the path electrical effort is H. What design is fastest for H=1? For H=5? For H=20? Explain your conclusions intuitively.



3. Repeat the decoder design example from Section 4.5.3 for a 32-word register file with 64-bit registers. Determine the fastest decoder design and estimate the delay of the decoder and the transistor widths to achieve this delay.

4. Design a circuit at the gate level to compute the following function:
   if (a == b) y = a;
   else y = 0;
   Let a,b, and y be 16-bit buses. Assume the input and output capacitances are each 10 units. Your goal is to make the circuit as fast as possible. Estimate the delay in FO4 inverter delays using Logical Effort if the best gate sizes were used. What sizes do you need to use to achieve this delay?

5. Figure 4.41 shows a datasheet for a 2-input NOR gate in the Artisan Components standard cell library for the TSMC 180 nm process. Find the average parasitic delay and logical effort of the X1 NOR gate A input. Use the value of τ from Section 4.4.5.

NOR2

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B)}$

Logic Symbol

Functions

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (μm)	Width (μm)
NOR2XL	5.04	1.98
NOR2X1	5.04	1.98
NOR2X2	5.04	3.30
NOR2X4	5.04	4.62

AC Power

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
A	0.0110	0.0143	0.0275	0.0545
B	0.0139	0.0182	0.0365	0.0728

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0033	0.0045	0.0083	0.0169
B	0.0029	0.0040	0.0085	0.0160

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0426	0.0403	0.0347	0.0351
A → Y↓	0.0213	0.0196	0.0183	0.0187
B → Y↑	0.0536	0.0519	0.0485	0.0473
B → Y↓	0.0259	0.0244	0.0247	0.0245

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	9.4704	6.7329	3.3656	1.6550
A → Y↓	3.5015	2.3672	1.2659	0.6330
B → Y↑	9.4589	6.7278	3.3647	1.6542
B → Y↓	3.5234	2.3779	1.2717	0.6357

6. Find the parasitic delay and logical effort of the X2 and X4 NOR gate A input using Figure 4.41. By what percentage do they differ from that of the X1 gate? What does this imply about our model that parasitic delay and logical effort depend only on gate type and not on transistor sizes?

7. Parasitic delay estimates in Section 4.4.2 are made assuming contacted diffusion on each transistor on the output node and ignoring internal diffusion. Would parasitic delay increase or decrease if you took into account that some parallel transistors on the output node share a single diffusion contact? If you counted internal diffusion capacitance between series transistors? If you counted wire capacitance with in the cell?

8. Some designers define a "gate delay" to be a fanout -of-3 2-input NAND gate rather than a fanout-of-4 inverter. Using Logical Effort, estimate the delay of a fanout-of-3 2-input NAND gate. Express your result both in τ and in FO4 inverter delays, assuming p_{inv} =1.

9. Repeat Exercise 8 in a process with a lower ratio of diffusion to gate capacitance in which p_{inv} =0.75. By what percentage does this change the NAND gate delay, as measured in FO4 inverter delays? What if p_{inv} =1.25?

10. The clock buffer in Figure 4.43 can present a maximum input capacitance of 100 fF. Both true and complementary outputs must drive loads of 300 fF. Compute the input capacitance of each inverter to minimize the worst-case delay from

input to either output. What is this delay, in τ? Assume the inverter parasitic delay is 1.

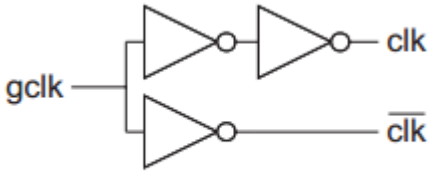


FIGURE 4.43 Clock buffer