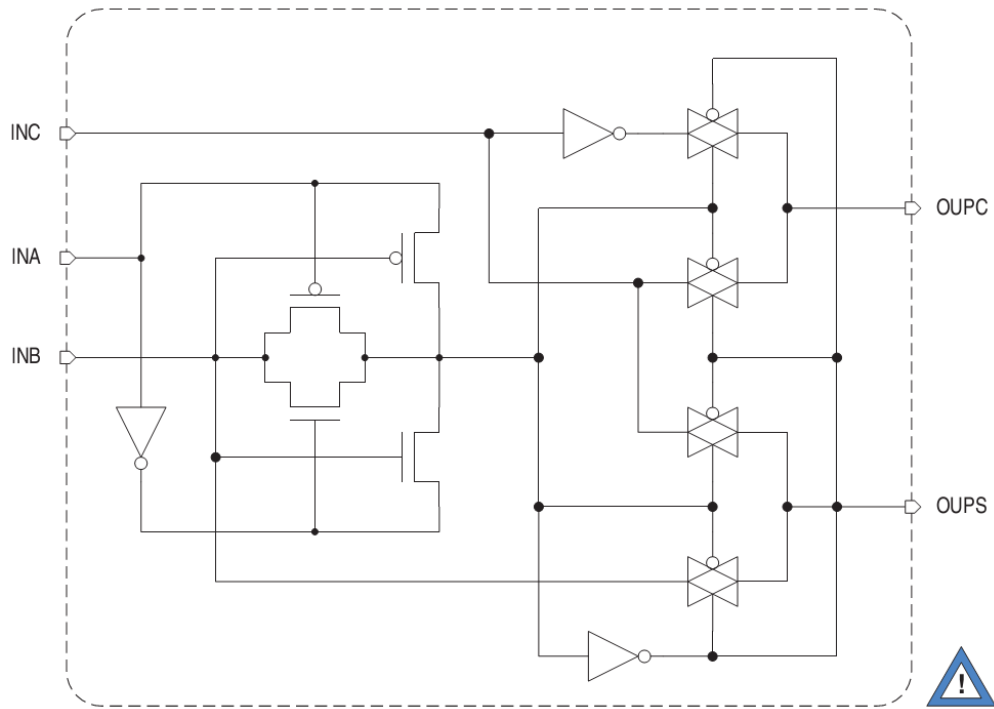
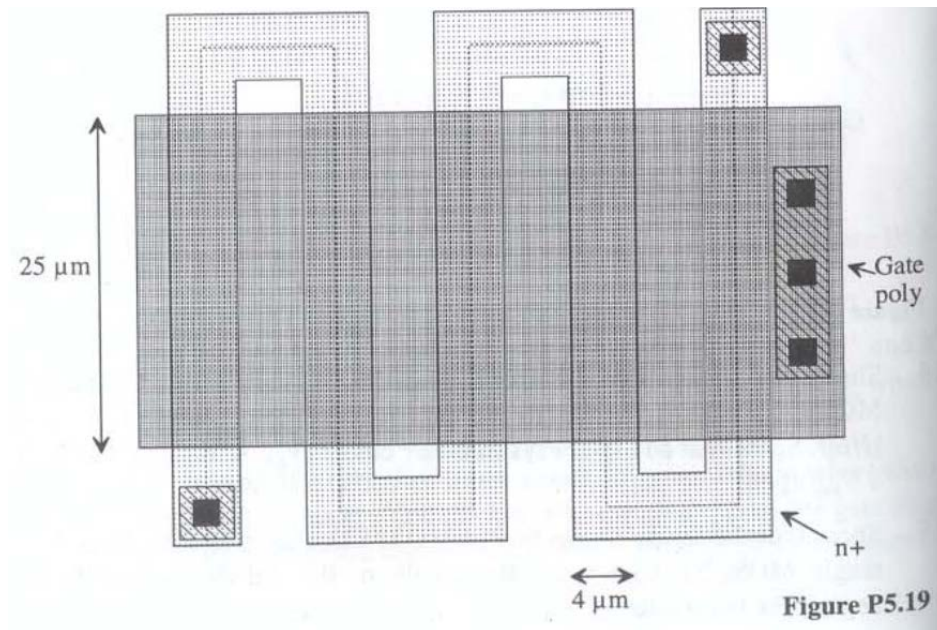


Layout Problems

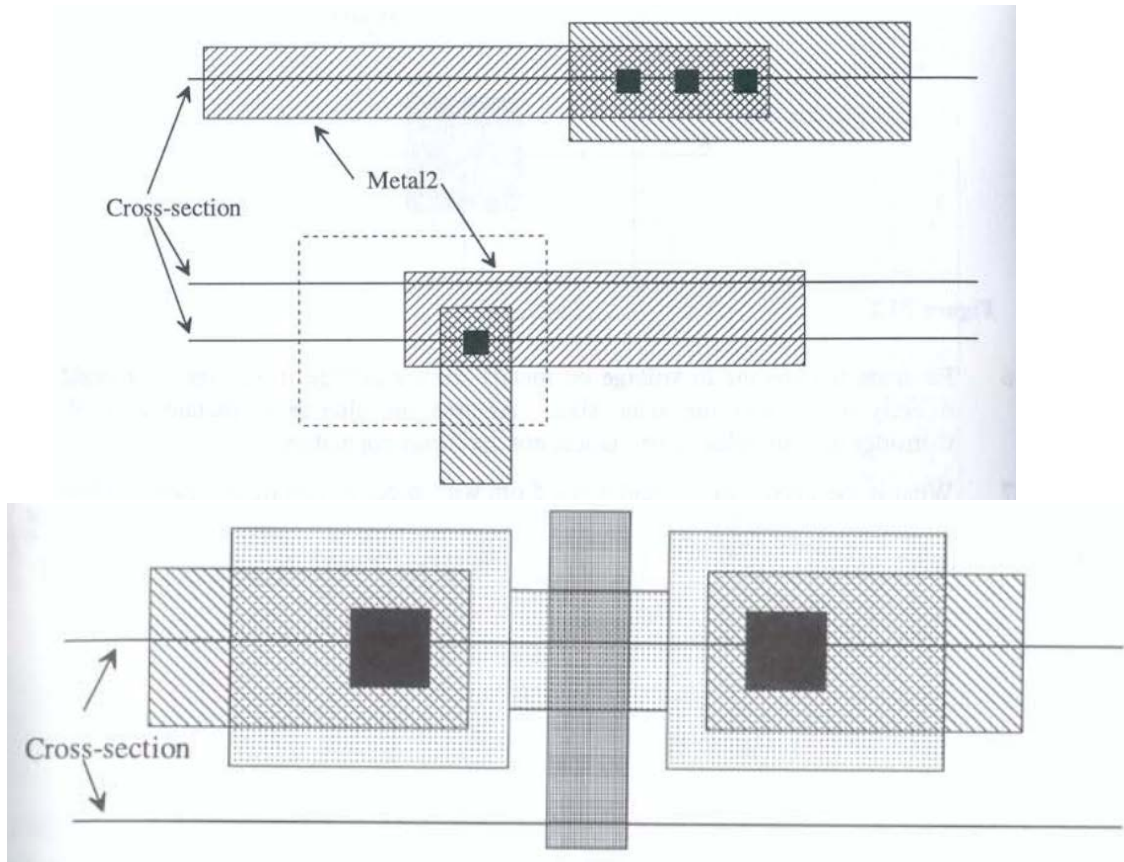
1. Consider the design of a CMOS compound OR-AND-INVERT gate computing $f = \overline{(a + b)}.c$
 - a. sketch a transistor-level schematic
 - b. sketch a stick diagram
 - c. estimate the area from the stick diagram
 - d. Draw the layout using unit-sized transistors
 - e. compare the layout size to the estimated area
2. Consider the design of a CMOS compound OR-OR-AND-INVERT gate computing $f = \overline{(a + b).(c + d)}$
 - a. sketch a transistor-level schematic
 - b. sketch a stick diagram
 - c. estimate the area from the stick diagram
 - d. Draw the layout using unit-sized transistors
 - e. compare the layout size to the estimated area
3. A carry lookahead adder computes $G = G_3 + P_3(G_2 + P_2(G_1 + P_1G_0))$. Consider designing a compound gate to compute G .
 - a. sketch a transistor-level schematic
 - b. sketch a stick diagram
 - c. estimate the area from the stick diagram
4. For the following schematic
 - a. What function does it implement
 - b. Sketch a stick diagram
 - c. estimate the area from the stick diagram
 - d. Draw the layout using unit-sized transistors
 - e. compare the layout size to the estimated area



5. For the layout shown in figure::
 - a. What structure does it represent
 - b. Calculate the minimum width and length of the layout



6. Sketch the cross-sectional views of the layouts shown in Figure at the indicated locations



7. Sketch the schematic corresponding to the layout seen below. Label all four terminals of the MOSFET in your schematic and comment on how the body of the MOSFET is tied to ground. Which terminal, of the MOSFET, would you label the drain and which would you label the source? Why?

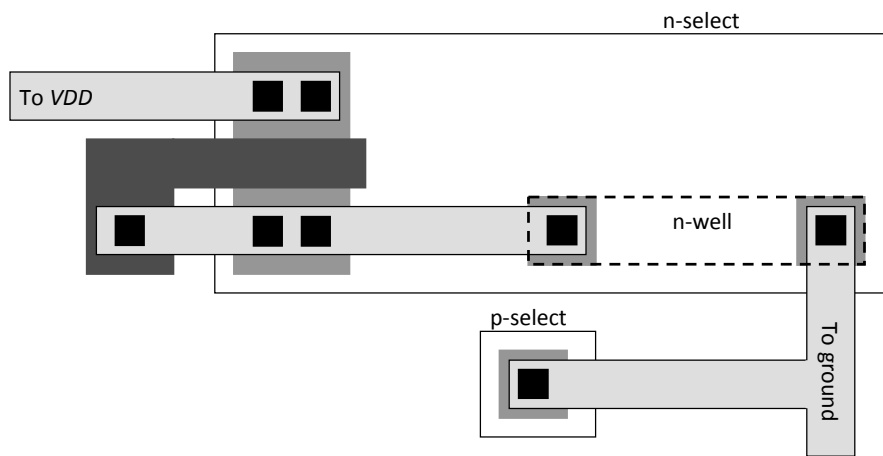


Figure A5.1 Sketching a schematic from a layout.

8. Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic.

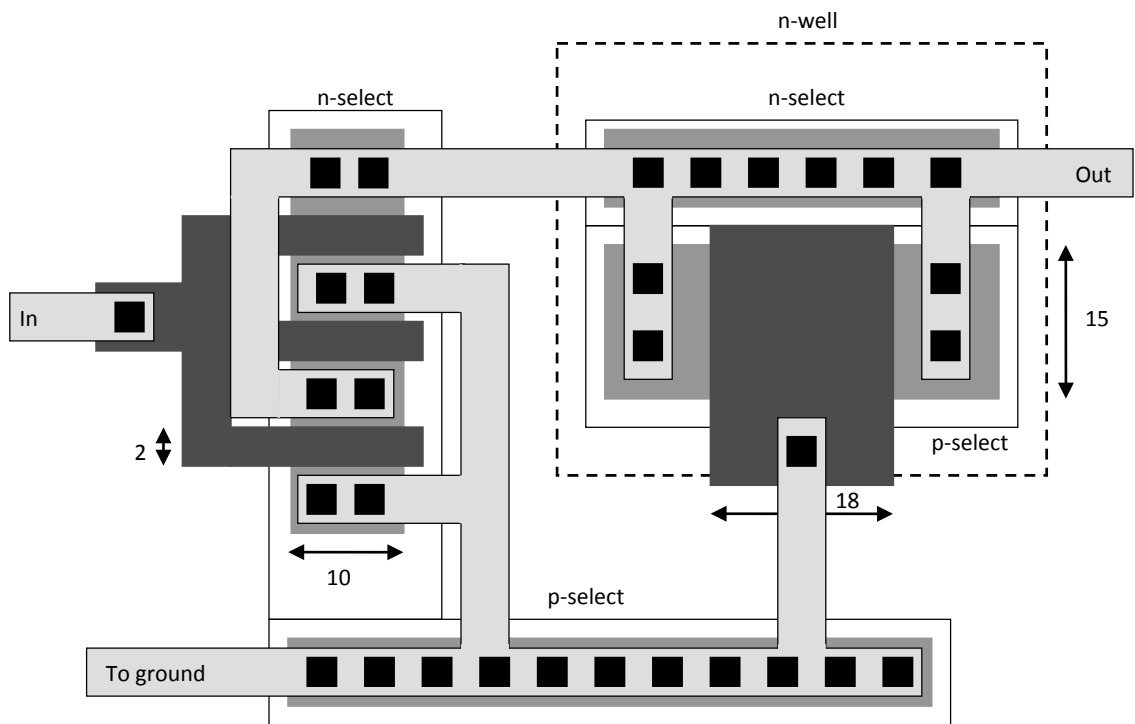


Figure A5.2 Sketching a schematic from a layout.

9. The straight forward CMOS implementation of the XOR gate ($f = a \oplus b$) employs inverter gates to implement \bar{a} and \bar{b} . The following realization of the XOR gate eliminates the need to such inverters and results in a reduced area gate.

$$f = \overline{ab} + \overline{\bar{a}\bar{b}} = \overline{ab} + \overline{(a + b)}$$

- sketch a transistor-level schematic for the straight forward CMOS implementation of XOR ($f = a\bar{b} + \bar{a}b$), and the previous realization
 - sketch a stick diagram for both XOR realizations
 - Draw an optimized layout for both XOR realizations using unit-sized transistors
10. You need to practice solving previous VLSI exams for years 2008-2012.