Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE432: VLSI Modeling and Design
Sheet 4
Verilog: Behavioral modeling

1- Design a 4 to 1 multiplexer using behavioral modeling, write down the test-bench.

2- Design a 4-bit binary counter using behavioral modeling, write down the test-bench.

3- Declare a register named oscillate, initialize it to zero and make it toggle every 30 time units, do not use ***always*** statement. (*Hint: use forever loop)*

4- Design a clock with time period 40 and duty cycle of 20% using behavioral modeling. It should be initialized to zero.

5- In the given code below, at what simulation time was each statement executed? What are the intermediate and final values of a, b, c and d.

```
initial
begin
    a = 1'b0;
    b = #10 1'b1;
    c = #5 1'b0;
    d = #20 {a, b, c};
end
```

6- Repeat the previous example for using non-blocking assignments.

7- What is the order of execution of the following code? What are the final values for a. b, c and d?

```
initial
begin
        a = 1'b0;
        #0 c = b;
end
initial
begin
        b = 1'b1;
        #0 d = a;
end
```

8- Design a negative edge D FF with synchronous clear, using behavioral statements only. Write a test-bench with clock period of 10 time units to test this block.

9- Redesign the D FF with asynchronous clear.

10- Design a level sensitive latch using **wait** statement.

11- Using **case** statement, design an 8-function ALU that takes 4-bit inputs *a* and *b*, and a 3-bit signal *select* and gives a 5-bit output *out*. The ALU implements the following functions based on the 3-bit input *select*. Ignore any overflow or underflow.

Select Signal	Function
3'b000	out = a
3'b001	out = a + b
3'b010	out = a - b
3'b011	out = a / b
3'b100	out = a % b (remainder)
3'b101	out = a << 1
3'b110	out = a >> 1
3'b111	out = (a > b) (magnitude compare)

12- Using repeat statement, delay the statement a = a+1 by 20 positive edges of the clock.