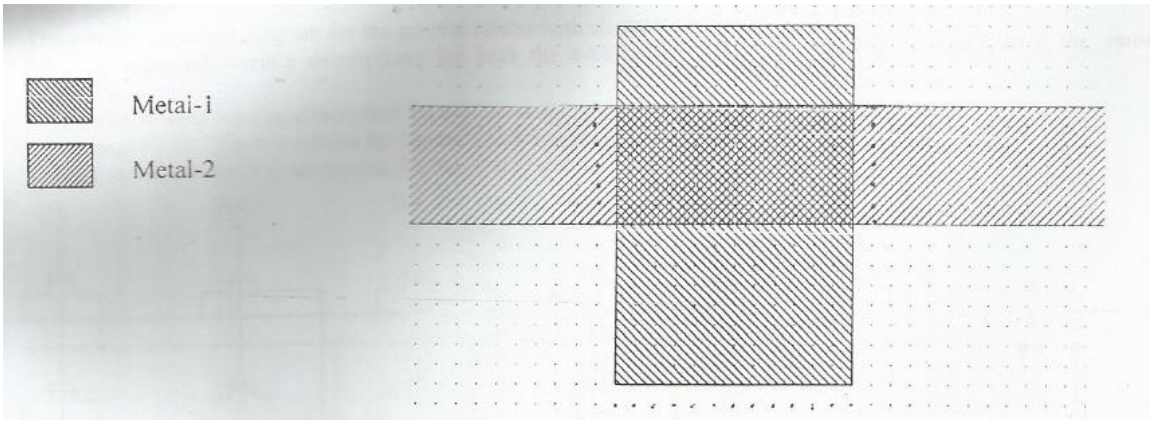
Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE432: VLSI Modeling and Design
Sheet 1

1- For the figure shown, a layout of Metal-2 interconnection wire crossing another Metal-1 interconnection wire. The layout is to be realized in scalable 0.5µm CMOS process having the following parameters:
   a. $\lambda = 0.5\mu m$, the distance between two grid points is λ.
   b. Metal-1 to substrate capacitance = $0.042 fF/\mu m^2$
   c. Metal-2 to substrate capacitance = $0.02 fF/\mu m^2$
   d. Metal-1 to Metal-1 capacitance = $0.036 fF/\mu m^2$

   Metal-2 is connected to voltage source while Metal-1 is left floating, the substrate is grounded, estimate the voltage change on Metal-1 wire if the voltage on Metal-2 changes abruptly from 0 to 5V, this is called "cross talk".

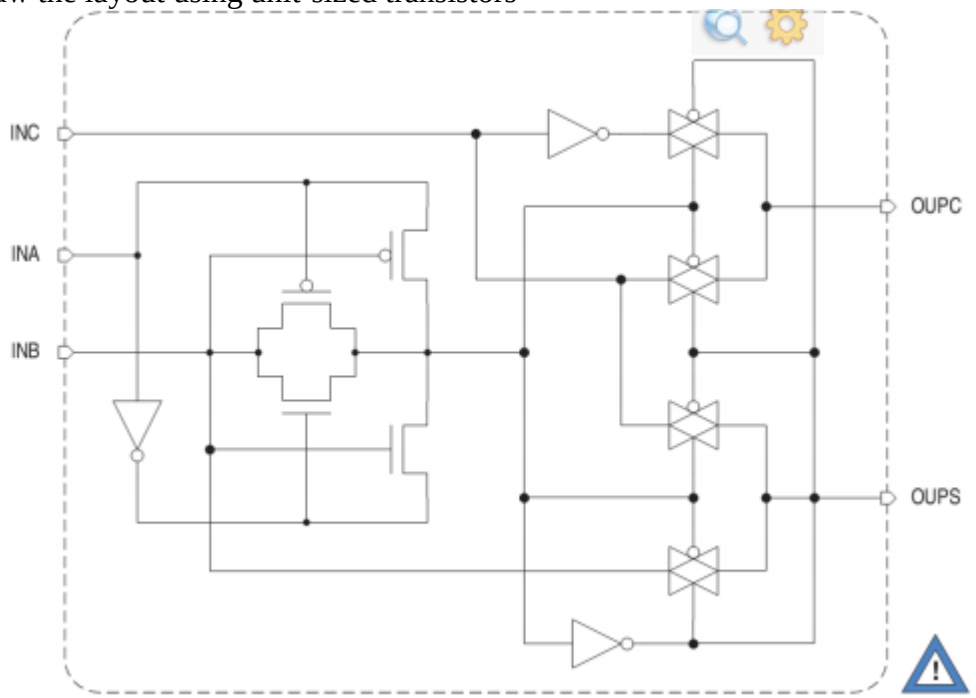


2- Consider the design of a CMOS compound OR-AND-INVERT gate computing $f = \overline{(a+b).c}$
   a. Sketch transistor level schematic.
   b. Sketch stick diagram.
   c. Draw layout using unit sized transistors.

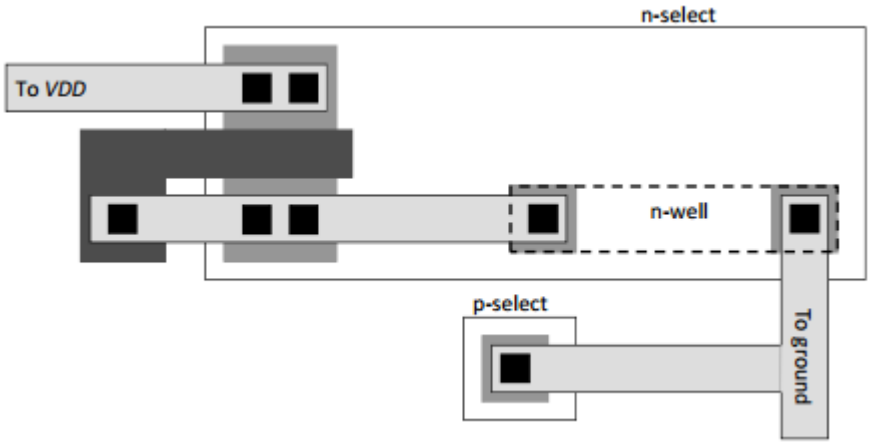
3- Consider the design of a CMOS compound OR-OR-AND-INVERT gate computing $f = \overline{(a+b).(c+d)}$.
   a. Sketch transistor level schematic.
   b. Sketch stick diagram.
   c. Draw layout using unit sized transistors.

4- For the following schematic
   a. What function does it implement
   b. Sketch a stick diagram
   c. Estimate the area from the stick diagram

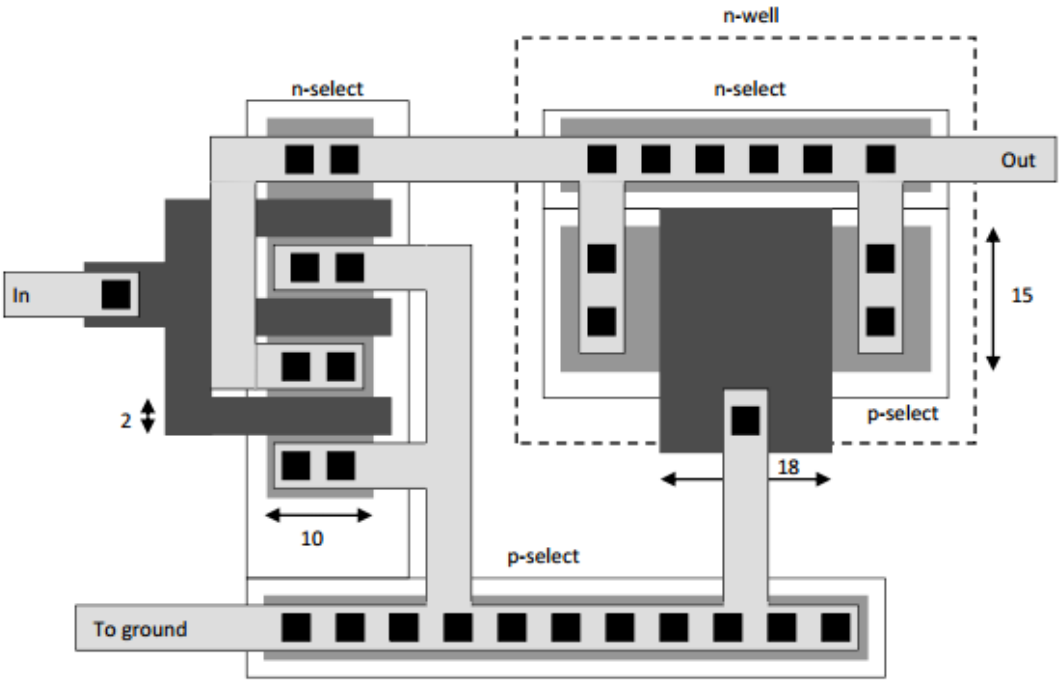
d. Draw the layout using unit-sized transistors



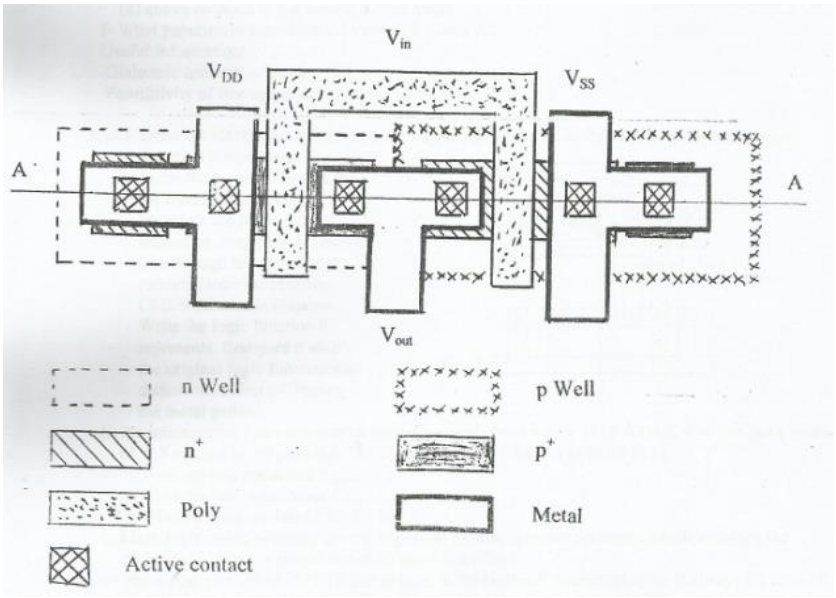
5- Sketch the schematic corresponding to the layout seen below. Label all four terminals of the MOSFET in your schematic and comment on how the body of the MOSFET is tied to ground. Which terminal, of the MOSFET, would you label the drain and which would you label the source? Why?



6- Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic.

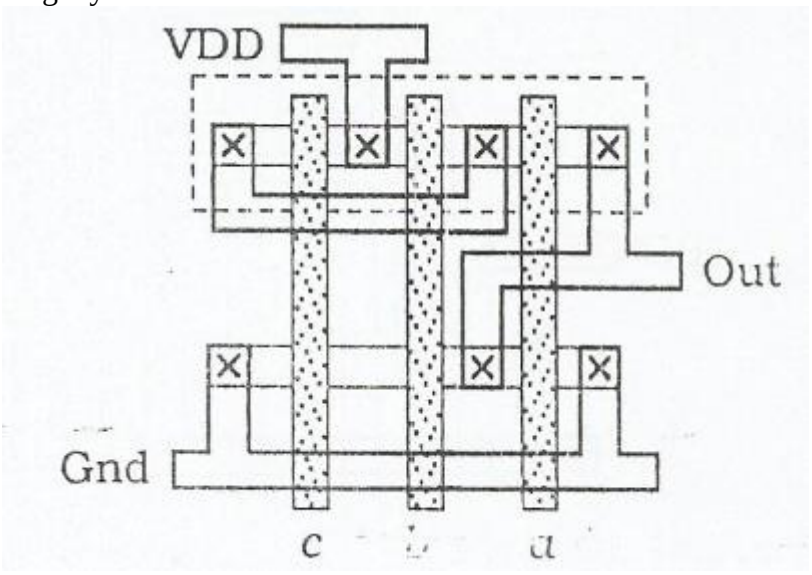


7- For the layout shown below



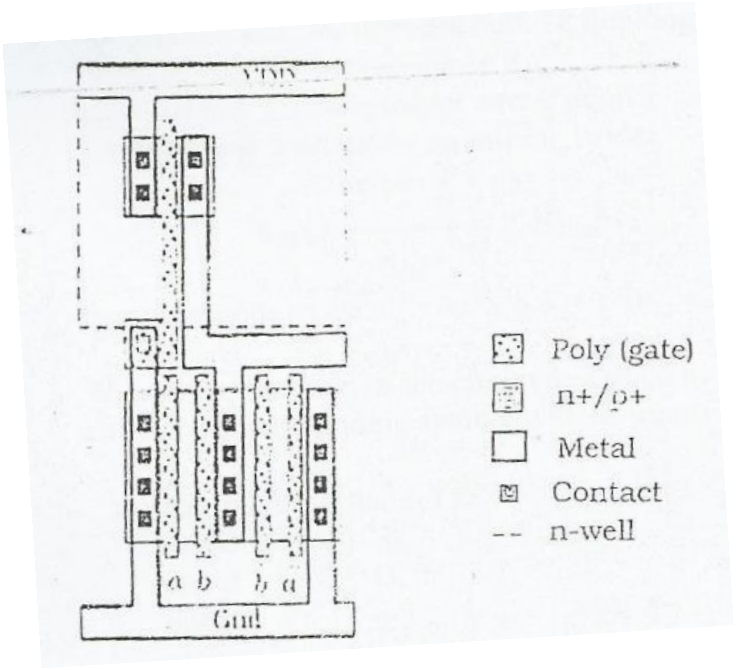
a. What is the function of the circuit?
b. Draw the cross section of the circuit A-A showing the gate oxide and the field oxide.

8- For the following layout

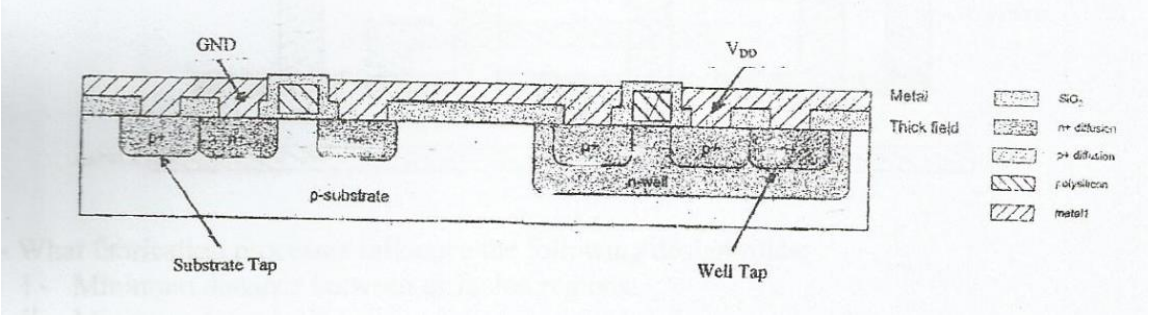


a. Draw the CMOS schematic of the layout and write down the funcion of this circuit.
b. If we flip the metal interconnects vertically, what is the resultant circuit? Draw the schematic ?

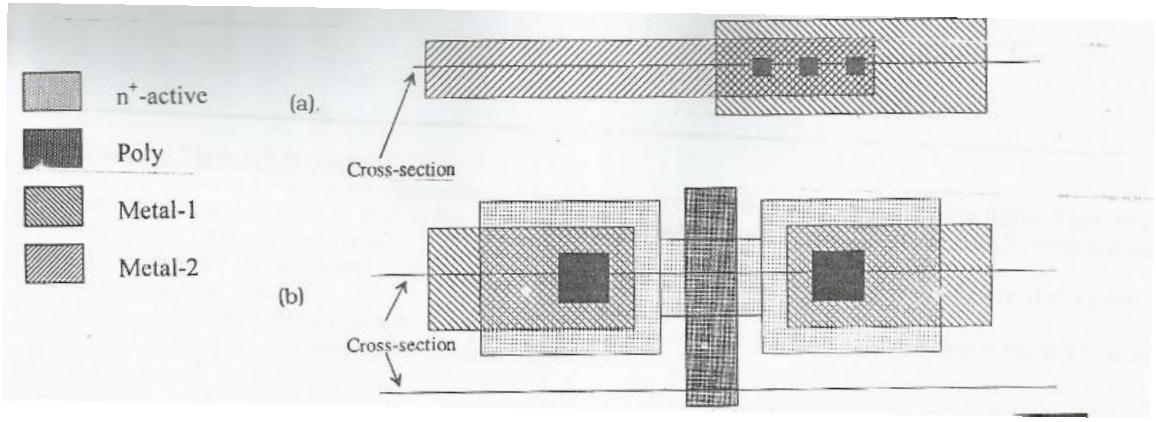
9- For the following layout, draw the schematic of this circuit, write down the function of the circuit and explain how it operates.



10- For the following cross section draw the stick diagram/layout, the schematic and the function of the circuit

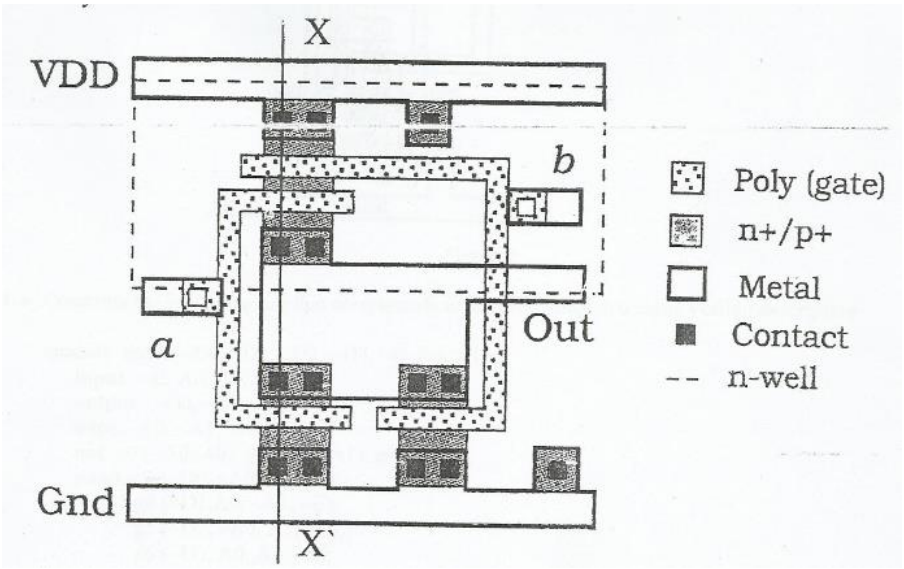


11- For the following layouts

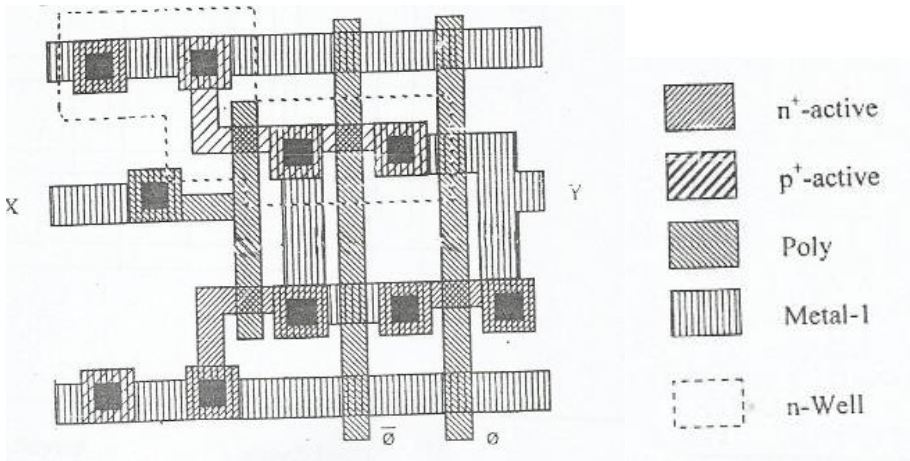


a. Sketch the cross sectional views of those figures.
b. Indicate on the layout the minimum dimensions and spacing between different layers so that the design rules would not be violated. Use MOSIS scalable design rules.

12- For the following layout write down the function of this circuit and draw the cross section X-X



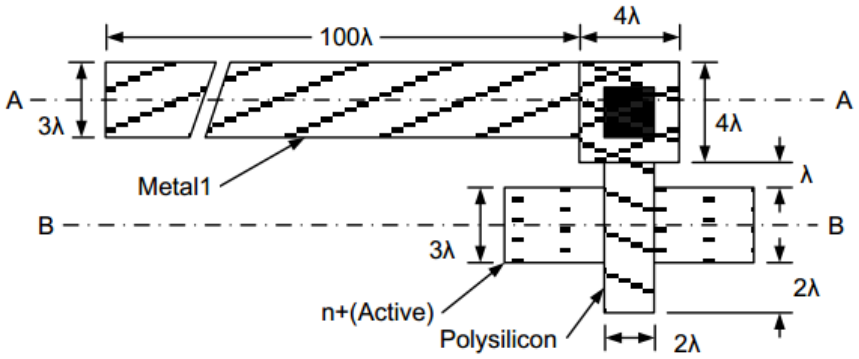
13- For the following layout, extract the schematic from the layout and construct a truth table for the cicruit.



14- For the layout shown below:

a. What structure does it represent?
b. The structure is to be fabricated in a scalable 1.2µm n-well CMOS process having the following parameters:
   i. λ=0.6 µm
   ii. Gate-to-Channel capacitance =1.6 fF/µm^2
   iii. Metal-to-Substrate capacitance=0.03 fF/µm^2
   iv. Polysilicon-to-Substrate capacitance=0.06 fF/µm^2

Estimate the total capacitance associated with the structures as seen from Metal1 layer to ground. Note that the substrate is connected to ground.



15- For the layout shown in the figure
a. Sketch the cross sectional views of the layout at the locations indicated.
b. Calculate the minimum n to p pitch and the minimum inverter height with and without the poly contact to the gate (in). Use MOSIS scalable design rules.
c. Briefly describe the physical limitations and potential problems associated with four design rules of different classes.