VLSI MODELING AND DESIGN

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Course Staff

- Instructor:
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- TA:
  - Mohammed Mogahed
- Office hours :
  - Saturday: 1:00 – 2:00 PM
  - Thursday: 10:00-11:30 PM

Course Text

- Textbook
  - "INTRODUCTION TO VLSI CIRCUITS AND SYSTEMS", John P. Uyemura
  - "Verilog HDL A Guide to Digital Design and Synthesis", Samir Palnitkar
- Reference books
  - "CMOS VLSI Design A Circuits and Systems Perspective", Neil Weste, David Harris
  - "Digital Integrated Circuit Design From VLSI Architectures to CMOS Fabrication", Hubert Kaeslin

Course Objectives

- Describe the digital VLSI design flow including both top-down and bottom-up approaches
- Design and analyze digital VLSI chips using CMOS technology
- Introduce basic concepts of CMOS VLSI design, layout, and fabrication
- Understand RTL design guidelines (new)
- Learn to use HDLs to capture, simulate, and synthesize VLSI circuits and systems
- Describe general VLSI system components including combinational and sequential logic gates, arithmetic circuits, and memory elements
- Learn to build VLSI architectures from DSP algorithms (new)

Course Objectives

- Learn to use physical layout tools to design and simulate basic combinational and sequential logic circuits
- Learn to use Verilog to design complex digital circuits, using simulation and synthesis tools
  - Structural, Dataflow, Behavioral Design
  - Test-bench Design and Digital Simulation
  - Design of Combinational & Sequential artifacts
  - Digital Synthesis using tools

Course Organization

- VLSI circuits modeling and design
- VLSI layout and fabrication
- Physical layout software
- Layout design and simulation Labs and project
- Midterm
- VLSI systems design using Verilog HDL
- RTL design guidelines
- HDL simulation and synthesis labs and project
- Final exam

Course Work

- 6 Labs
- 2 Projects
- A Midterm exam
- A Final Exam
- Tools:
  - Tanner L-edit http://www.tannereda.com/
  - Xilinx ISE http://www.xilinx.com/
  - Altera Quartus http://www.altera.com/

Grading

- Steady and persistent effort is rewarded
  - Labs: 25 marks
    - Attendance: 5 marks
    - Lab work: 10 marks
    - Projects (2): 10 marks
  - Midterm exam: 25 marks
  - Final exam: 75 marks

History of VLSI

The Integrated Circuit

- 1959: Jack Kilby, working at TI, invented a monolithic "integrated circuit"
  - Components connected by hand-soldered wires and isolated by "shaping", PN-diodes used as resistors (U.S. Patent 3,138,743)

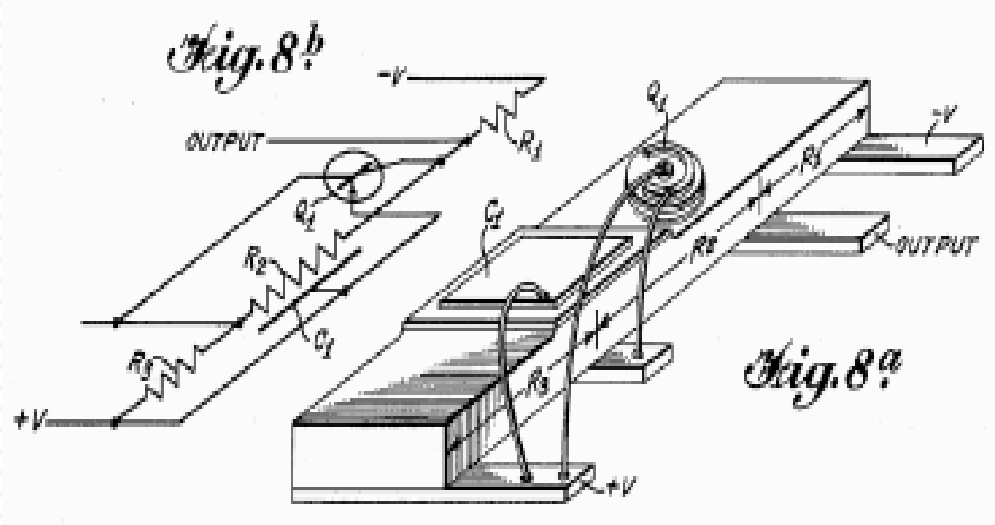


Figure 0.1 Diagram from patent application

Integrated Circuits

- 1961: TI and Fairchild introduced the first logic ICs ($50 in quantity)
- 1962: RCA developed the first MOS transistor

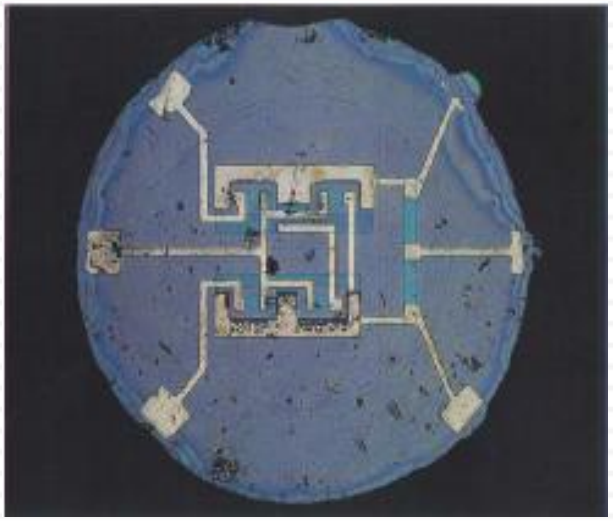


Figure 0.2 Fairchild bipolar RTL Flip-Flop

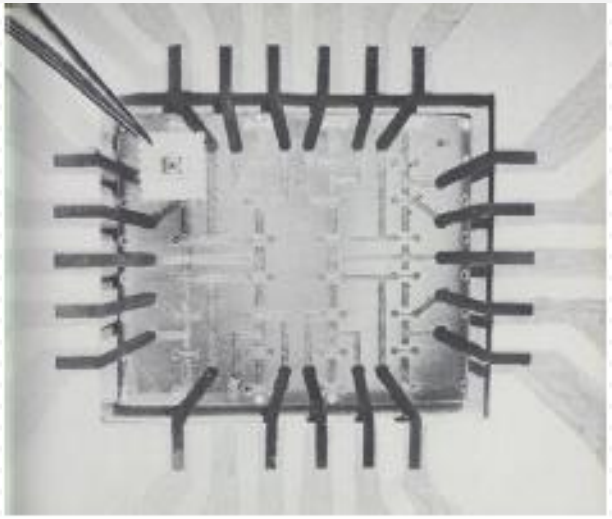
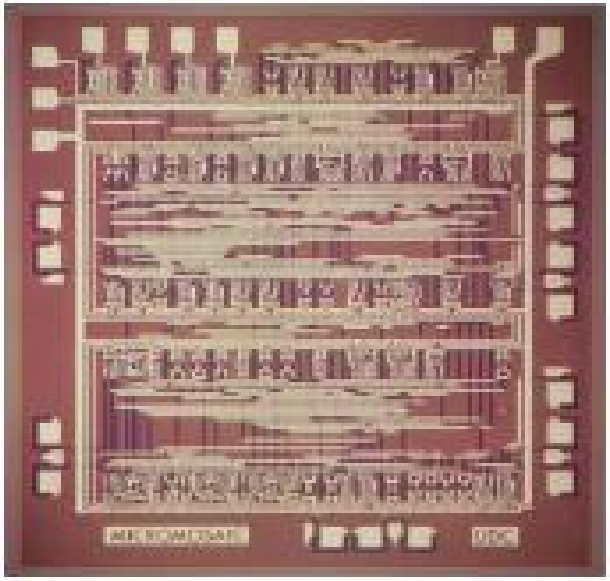


Figure 0.3 RCA 16-transistor MOSFET IC

Computer-Aided Design

- 1967: Fairchild developed the "Micromosaic" IC using CAD
  - Final layer of interconnect could be customized for different applications



- 1968: Noyce, Moore left Fairchild, started Intel

RAMs

- 1970: Fairchild introduced 256-bit Static RAMs
- 1970: Intel started selling 1K-bit Dynamic RAMs

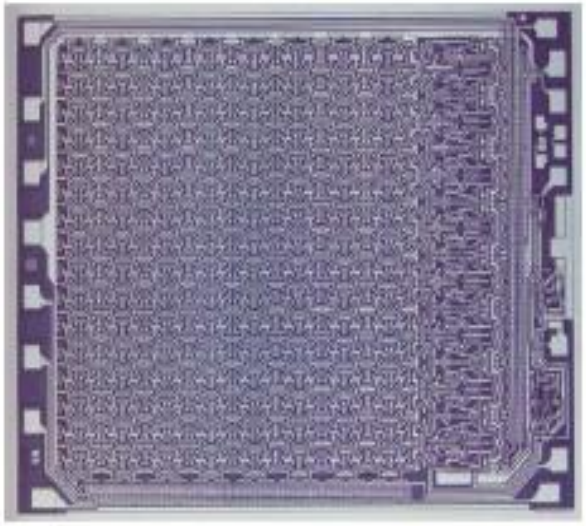


Figure 0.4 Fairchild 4100 256-bit SRAM

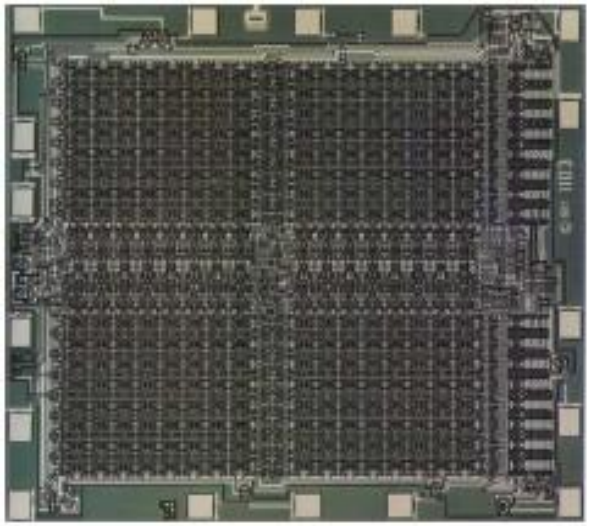


Figure 0.5 Intel 1103 1K-bit DRAM

The Microprocessor

- 1971: Intel introduced the 4004
  - General purpose programmable computer instead of a custom chip for a Japanese calculator company

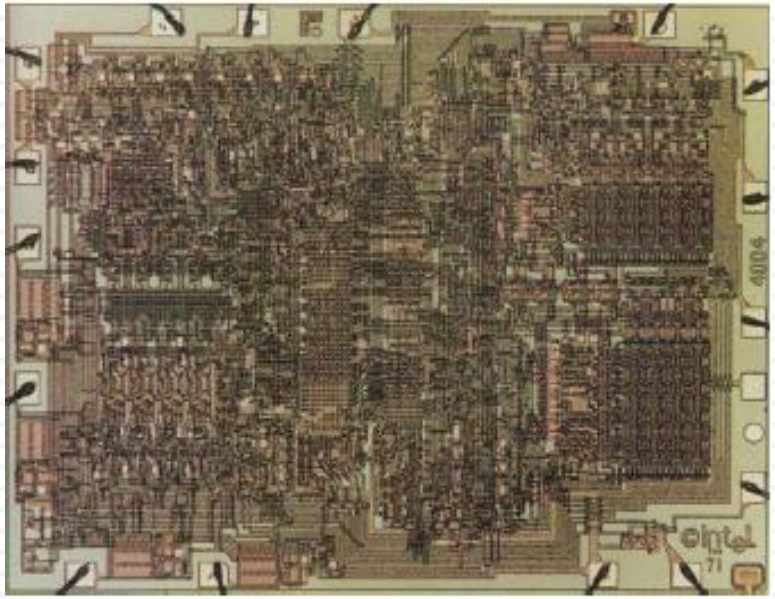
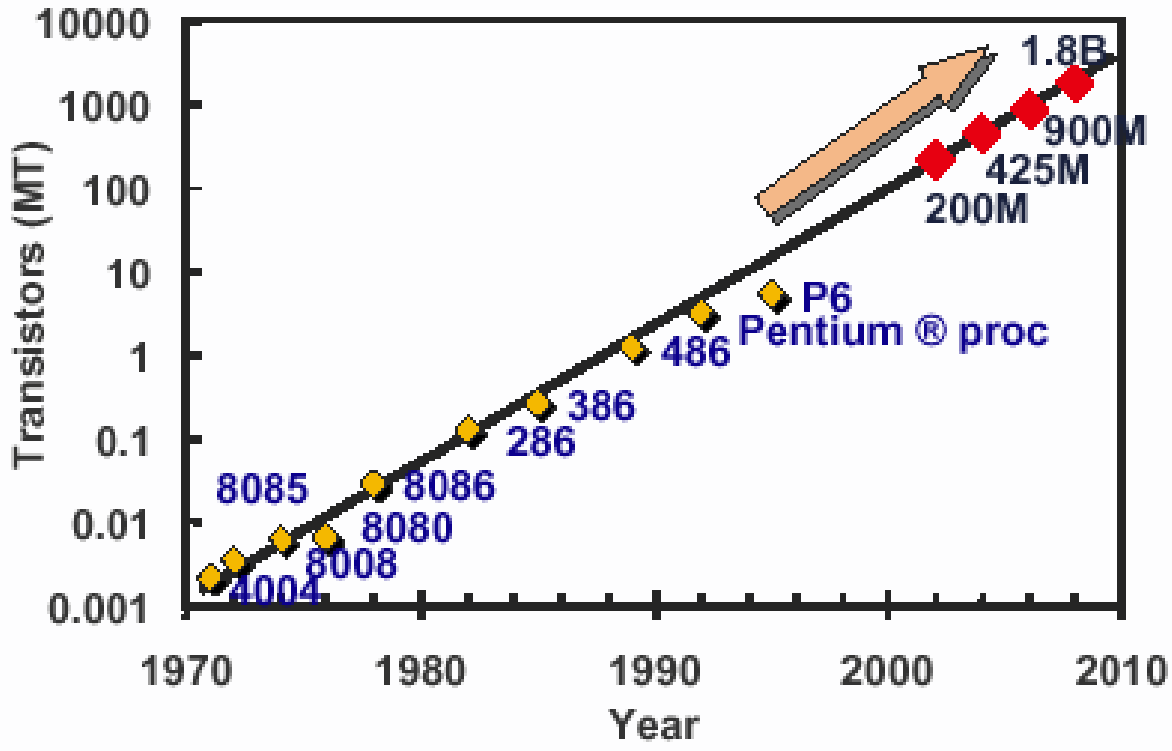


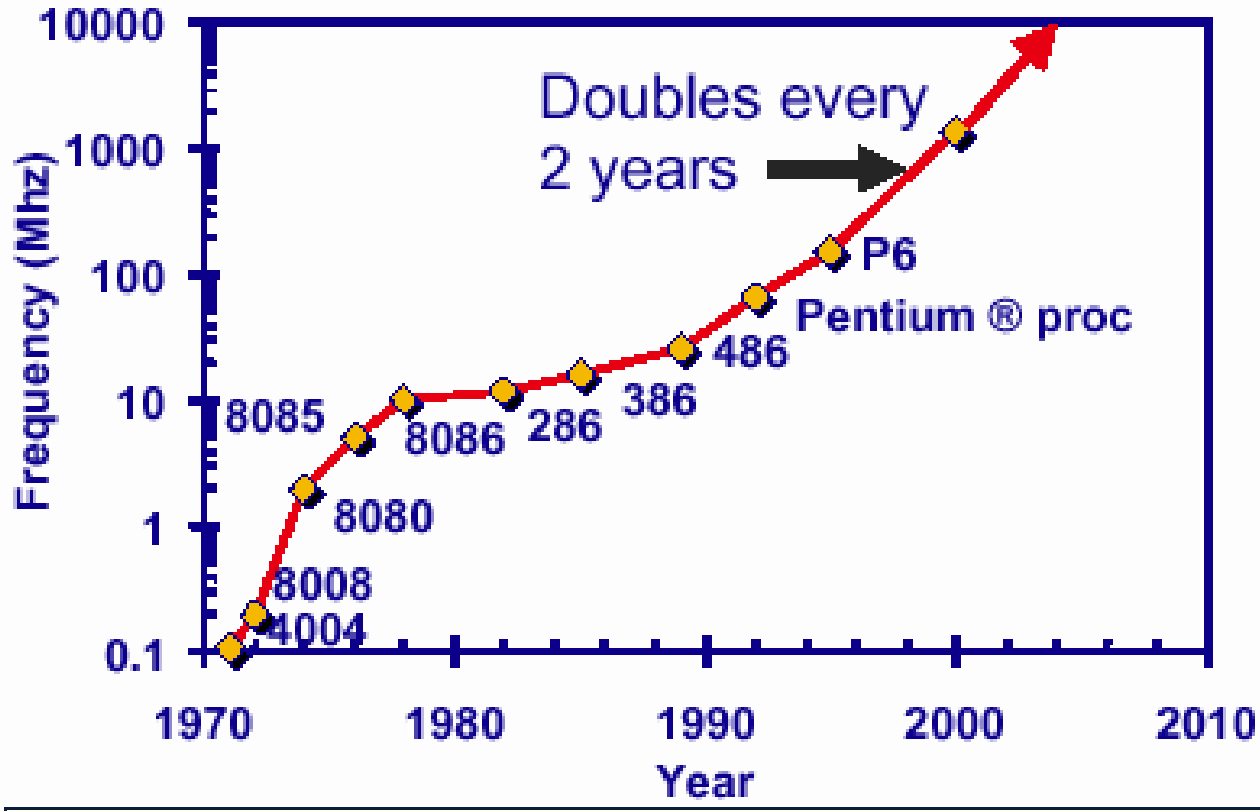
Figure 0.6 Intel 4004 Microprocessor

Moore's Law and Transistor Count



Transistors in Lead Microprocessors double every 2 years
Leads to 200M--1.8B transistors on the Lead Microprocessor

Moor's Law and Frequency



Lead Microprocessors frequency doubles every 2 years

Chapter 1

Introduction

Outline

- Introduction
- Complexity and Design
- Basic Concepts

Introduction

- IC: Integrated Circuits, many transistors on one chip
- VLSI: Very Large Scale Integration, a modern technology of IC design flow
- MOS: Metal-Oxide-Silicon transistor (also called device)
- CMOS: Complementary Metal Oxide Semiconductor
  - Fast, cheap, low power transistors
  - High integration, low cost
  - n-type MOS (nMOS): Majority carriers are Electrons
  - p-type MOS (pMOS): Majority carriers are Holes
- First: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip!!

Introduction

- The term VLSI is used to collectively refer to many fields of electrical and computer engineering that deal with the analysis and design of very dense ICs
- A VLSI chip contains more than 10^6 switching devices or logic gates
- Early in the first decade of the 21st century, the actual number of transistors has exceeded 10^8 on a silicon die of typically 1 cm^2 area

Outline

- Introduction
- Complexity and Design
- Basic Concepts

Complexity and Design

- Creating a design team provides a realistic approach to approaching a VLSI project, as it allows each person to study small sections of the system
  - VLSI project needs hundreds of engineers, scientists, and technicians
  - H*ierarchy design* and many different "*Level Views*" help to manage the complexity
  - Most work is conducted using computer-Aided Design (CAD) tools

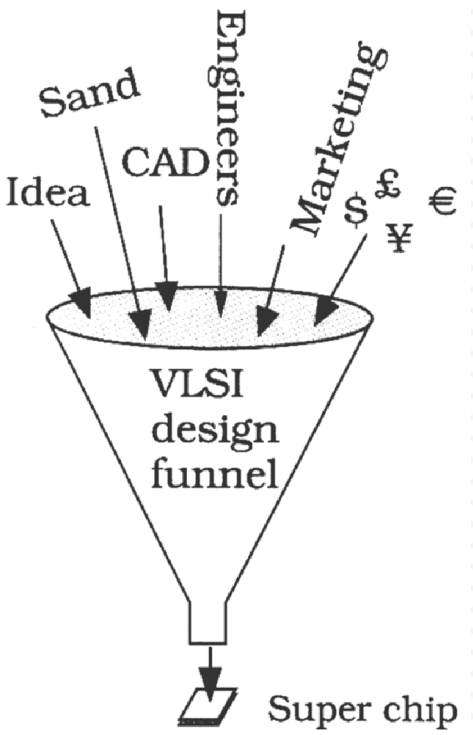


Figure 1.1 The VLSI design funnel

Complexity and Design

- Design teams provide a realistic approach to develop a VLSI chip
- The design hierarchy enables collaboration between team members and partitioning the work into a number of sub-tasks
- The chip is viewed at many abstraction levels from the system specifications to the physical implementation.

Design Hierarchy (1/2)

- System specifications: is defined in both general and specific terms, such as *functions*, *speed*, *size*, etc.
- Abstract high-level model: contains information on the behavior of each block and the interaction among the blocks in the system
- Logic synthesis: To provide the logic design of the network by specifying the primitive gates and units needed to build each unit
- Circuit design: where transistors are used as switches and Boolean variables are treated as vary voltage signal
- Physical design: the network is built on a tiny area on a slice of silicon
- Manufacturing: a completed design process is moved on to the manufacturing line

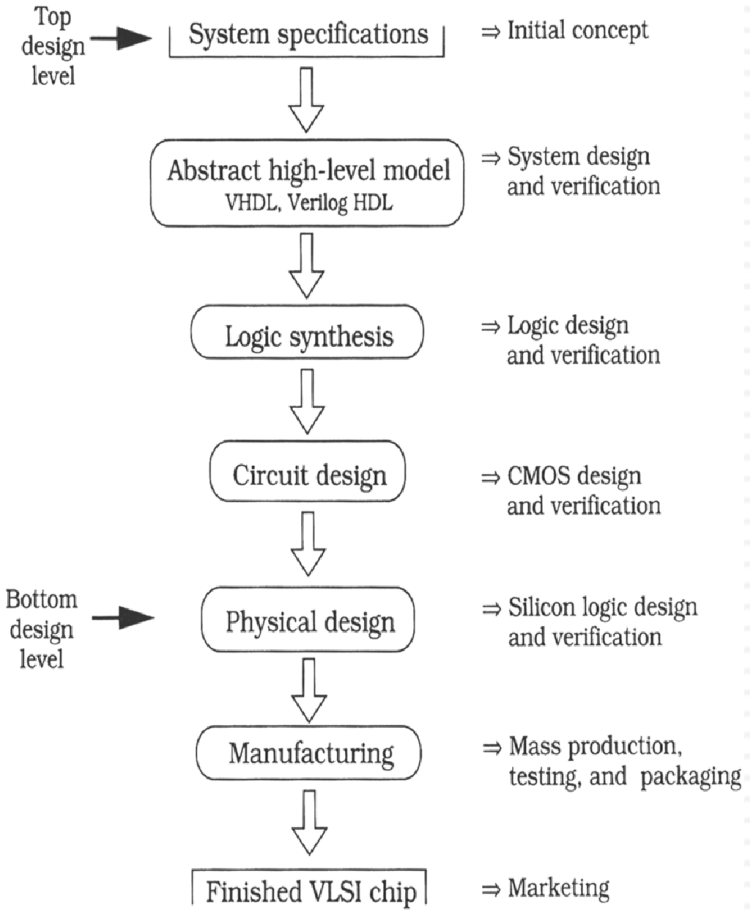


Figure 1.2 General overview of the design hierarchy

Design Hierarchy (2/2)

- Hierarchical design
  - **Top-down design**
    - The initial work is quite abstract and theoretical and there is no direct connection to silicon until many steps have been completed
    - Acceptable in modern digital system design
    - Co-design with combining HW/SW is critical
    - Similar to *Cell-based Design Flow*
  - **Bottom-up design**
    - Starts at the silicon or circuit level and builds primitive units such as logic gates, adders, and registers as the first steps
    - Acceptable for small projects
    - Similar to *Full-custom Design Flow*
- An example of a design hierarchy in Figure 1.3

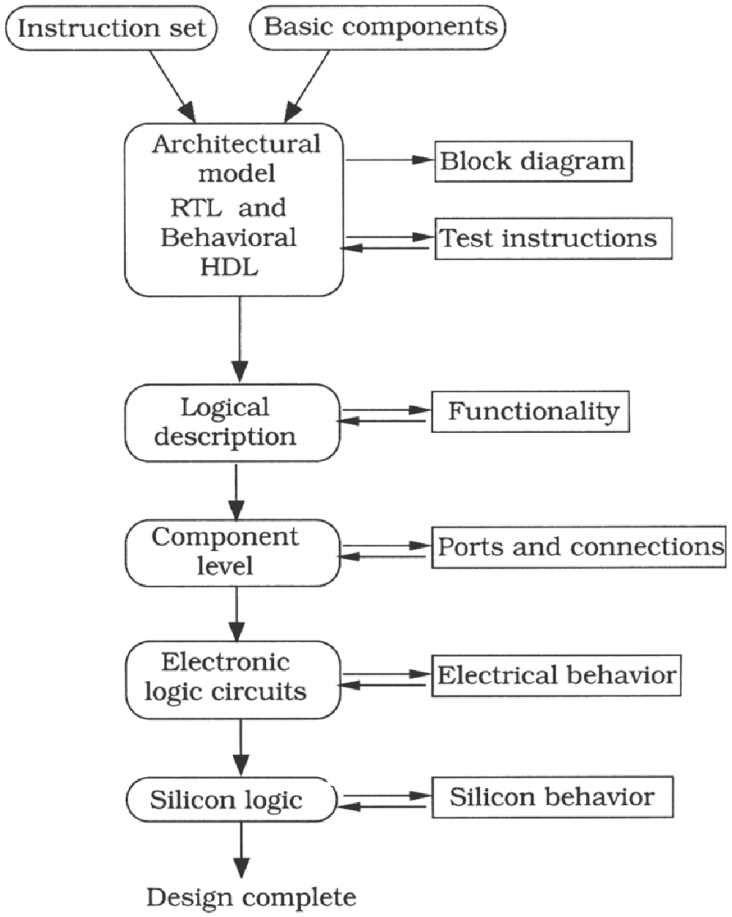


Figure 1.3 A simple design flow for a microprocessor

VLSI Chip Types

- At the engineering level, digital VLSI chips are classified by the approach used to implement and build the circuit
  - **Full-custom Design**: where every circuit is custom designed for the project
    - Extremely tedious
    - Time-consuming process
  - **Application-Specific Integrated Circuits (ASICs)**: using an extensive suite of CAD tools that portray the system design in terms of standard digital logic constructs
    - Including state diagrams, functions tables, and logic diagram
    - Designer does not need any knowledge of the underlying electronics or the physic of the silicon chip
    - Major drawback is that all characteristics are set by the architectural design
  - **Semi-custom Design**: between that of a full-custom and ASICs
    - Using a group of primitive predefined cells as building blocks, called *cell library*