SYSTEM SPECIFICATIONS USING VERILOG HDL

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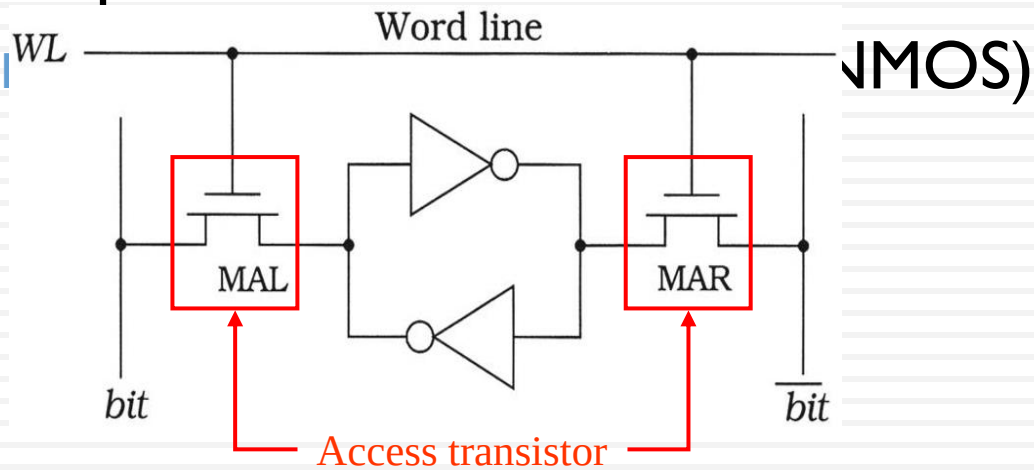
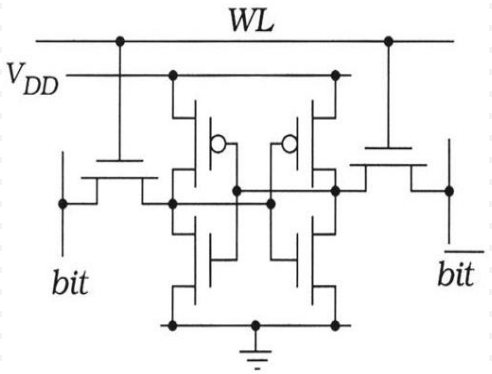
Static Random Access Memory, SRAM

- SRAM : cells use a simple bi-stable circuit to hold a data bit
  - Three states: hold, write, and read operations

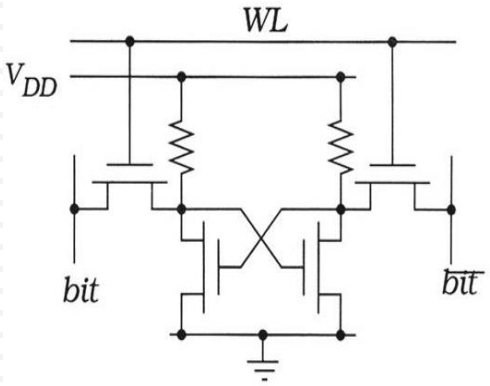


NMOS)

Figure 13.1 General SRAM cell



(a) 6T cell



(b) 4T cell with poly resistors

Figure 13.2 CMOS SRAM circuits

SRAM (1/2)

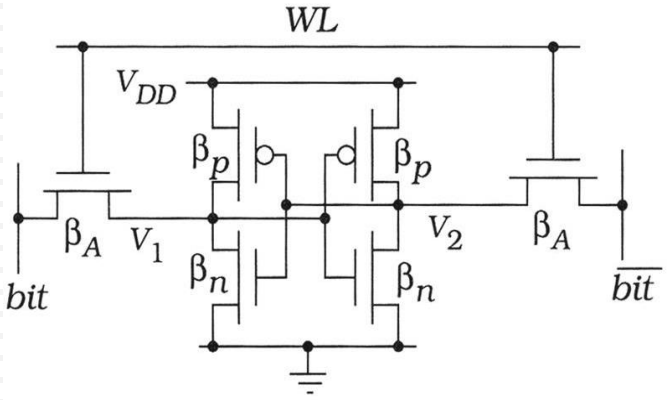
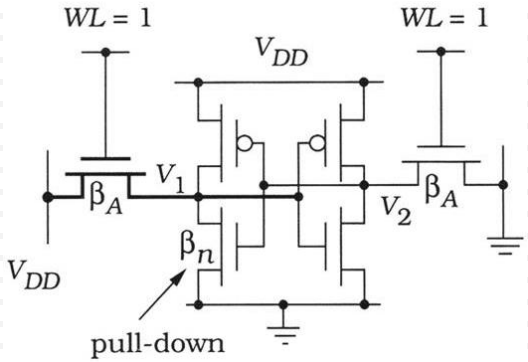


Figure 13.3 6T SRAM cell design parameters



(a) Write 1 operation

Write 1: in worst case, $V_1 = 0$, $V_2 = V_{DD}$
$\rightarrow(\beta_A/\beta_n = 2)$
Why??

$$\frac{(W/L)_{nA}}{(W/L)_n} \qquad (13.1)$$

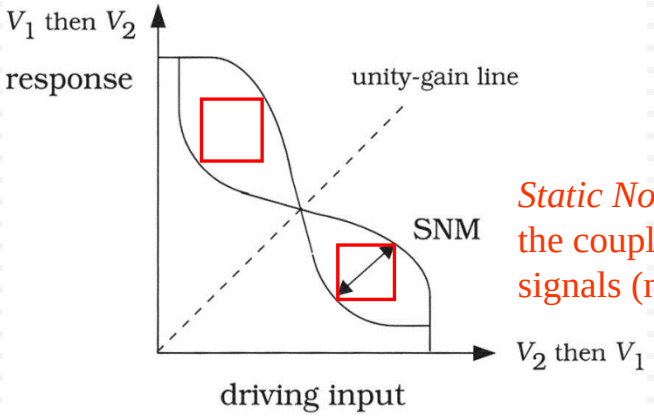
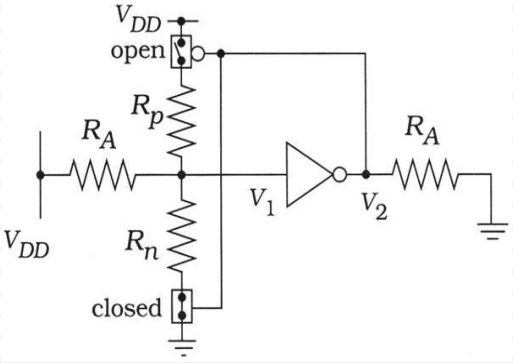


Figure 13.4 Butterfly plot

Static Noise Margin: immunity the coupled electromagnetic signals (noise)



(b) Resistor model

Figure 13.5 Writing to an SRAM

SRAM (2/2)

S: Source
D: Drain

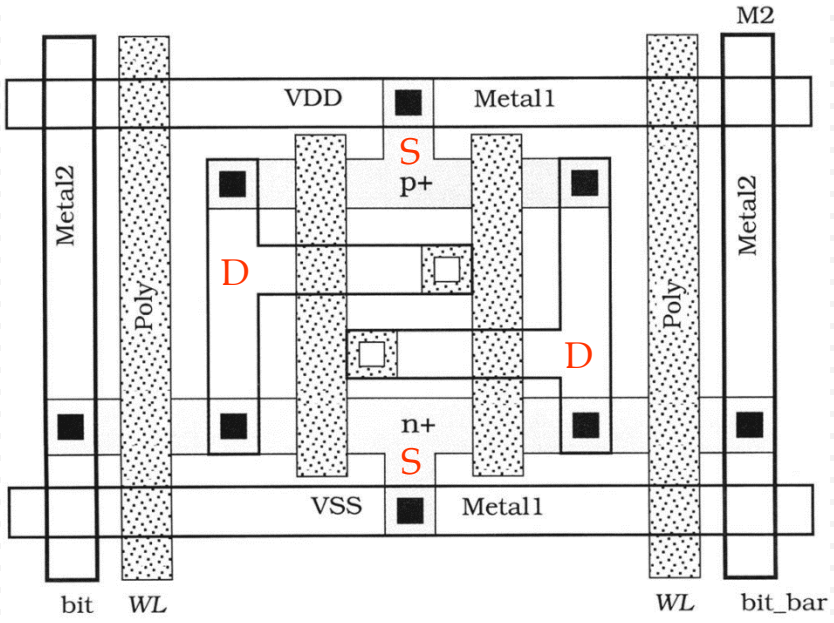


Figure 13.6 Example of a basic 6-T SRAM cell layout

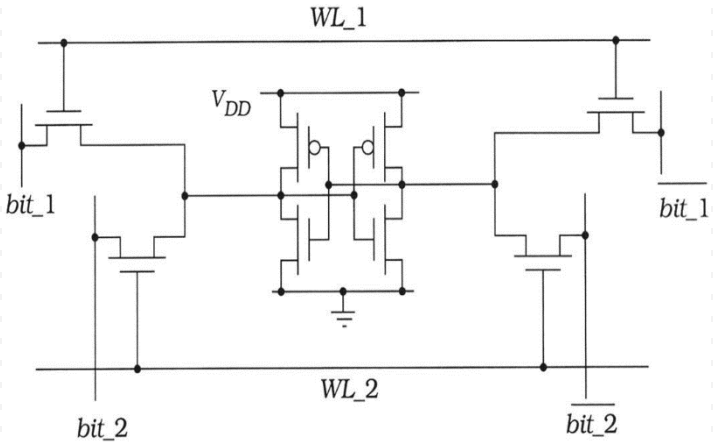


Figure 13.7 A 2-port CMOS SRAM cell

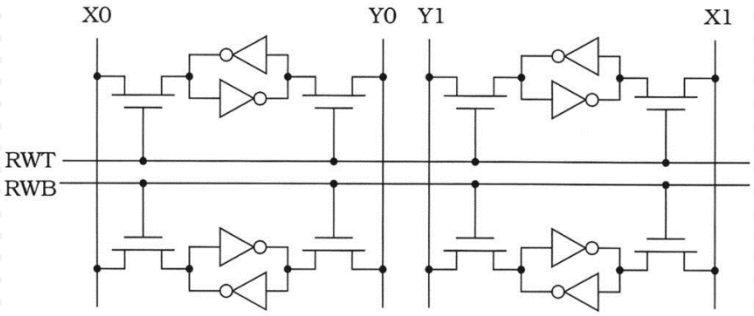
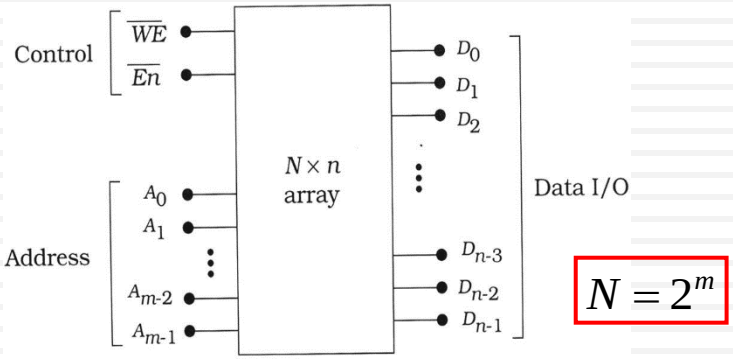


Figure 13.8 4-cell SRAM group

Outline

- The Static RAM
- SRAM Arrays
- Dynamic RAM
- ROM Arrays
- Logic Arrays

SRAM Arrays (1/4)



$$N = 2^m$$

Figure 13.9 High-level view of an SRAM

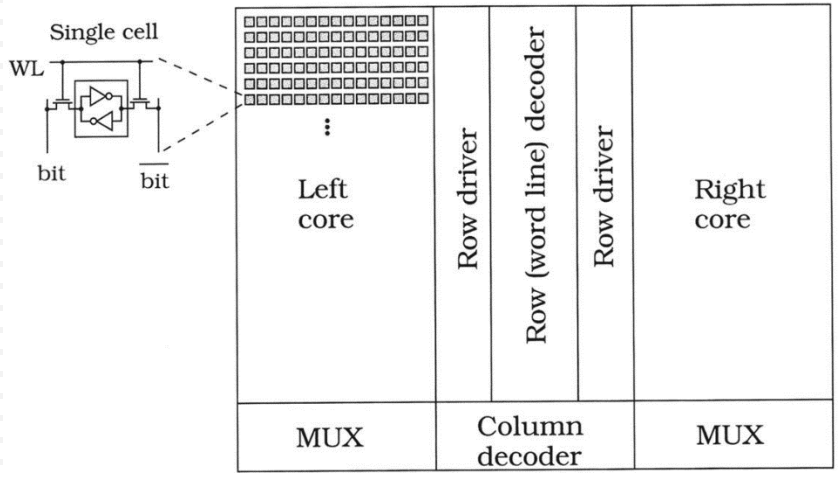


Figure 13.10 Central SRAM block architecture

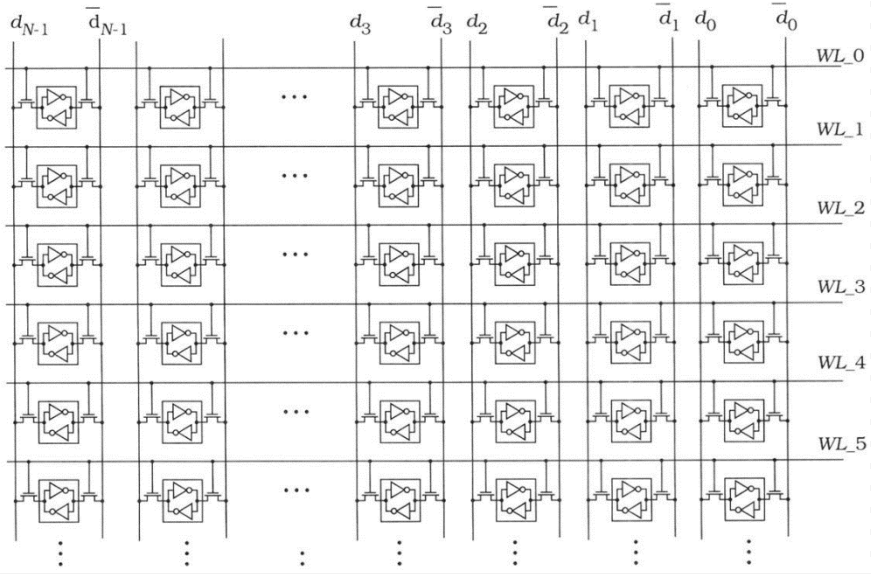


Figure 13.11 Cell arrangement in a core region

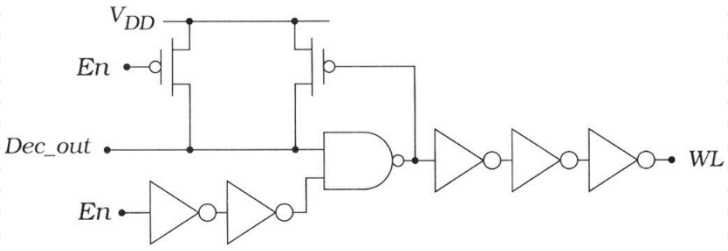


Figure 13.12 Row driver circuit

SRAM Arrays (2/4)

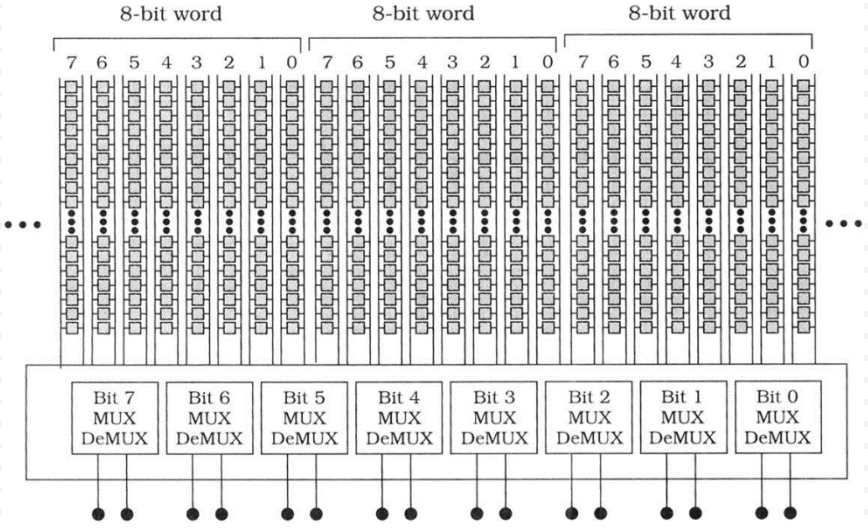


Figure 13.13 Column MUX/DeMUX network for 8-bit words

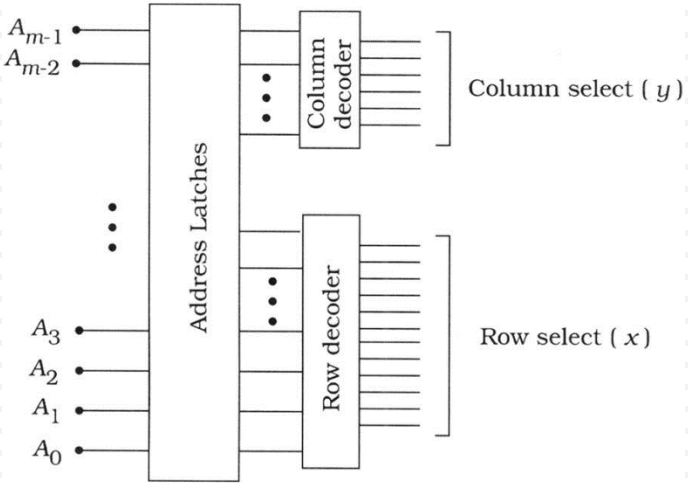


Figure 13.15 Basic addressing scheme

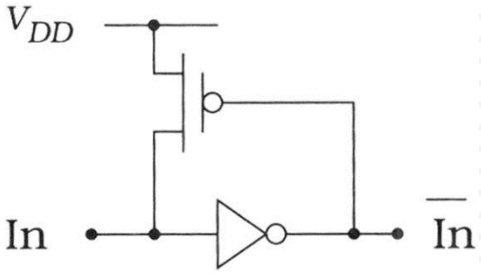


Figure 13.14 Logic 1 column driver

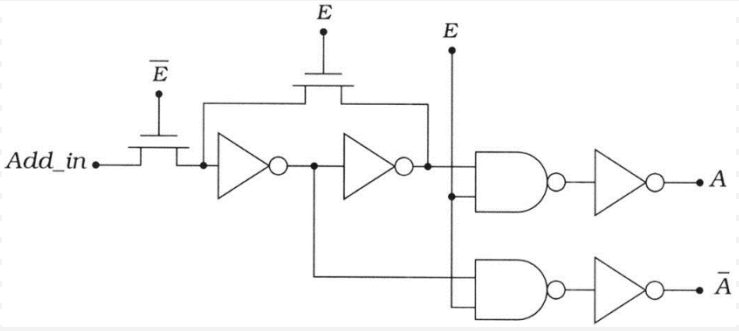


Figure 13.16 Address latch circuit

SRAM Arrays (3/4)

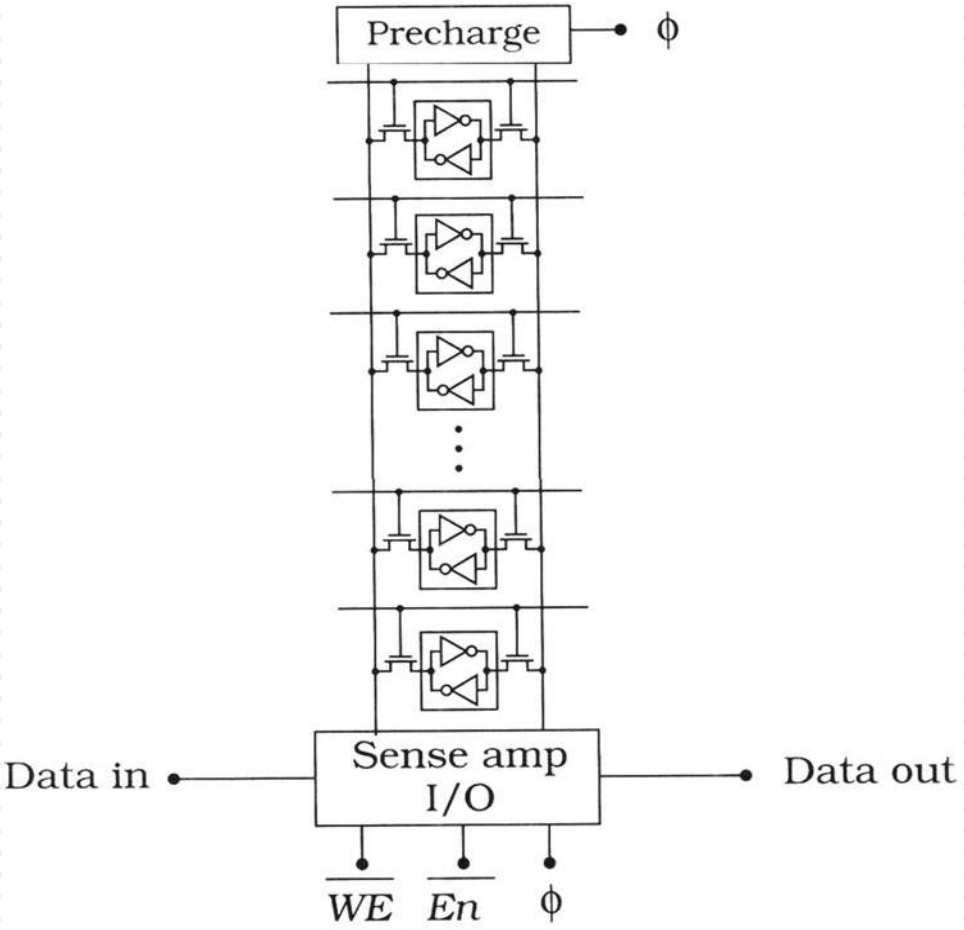


Figure 3.17 Pre-charge and I/O circuit for a single column

SRAM Arrays (4/4)

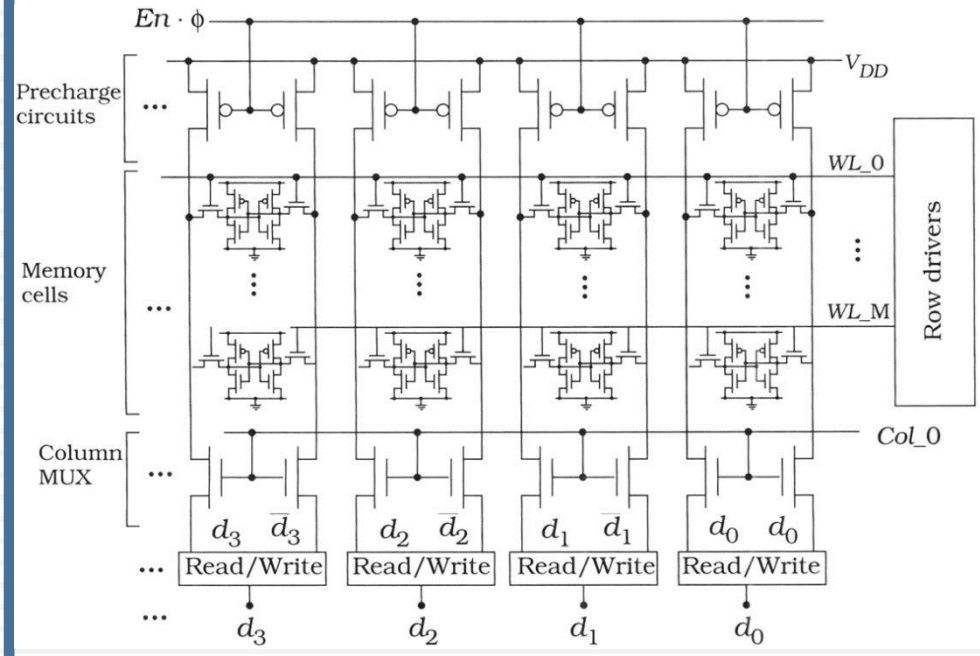


Figure 3.18 Expanded view of column circuitry

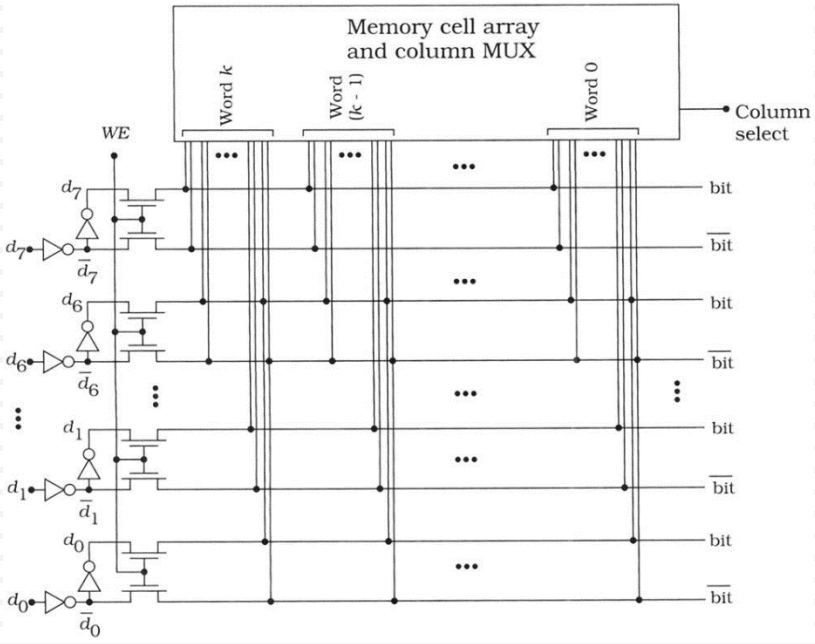


Figure 13.19 Write circuitry example

Sensing Operation

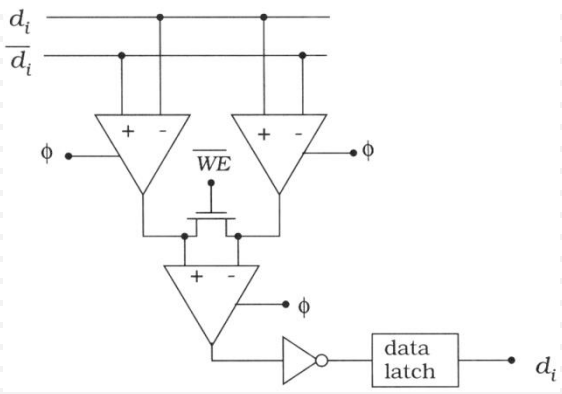
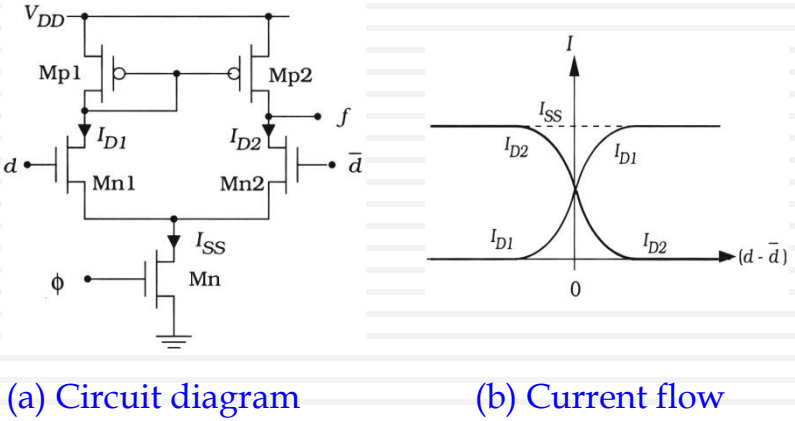


Figure 3.20 Example of a sensing scheme for the read operation



(a) Circuit diagram (b) Current flow

Figure 3.21 Single-ended differential amplifier

$$v_d = (v^+ - v^-) \qquad (13.5)$$

$$v_{out} = Av_d = A(v^+ - v^-) \qquad (13.6)$$

$$I_{SS} = I_{D1} + I_{D2} \qquad (13.7)$$

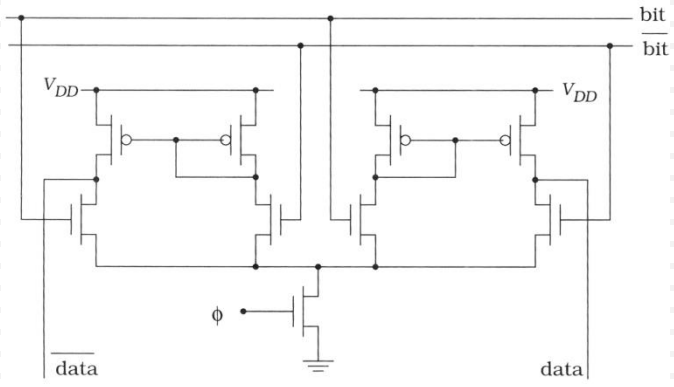
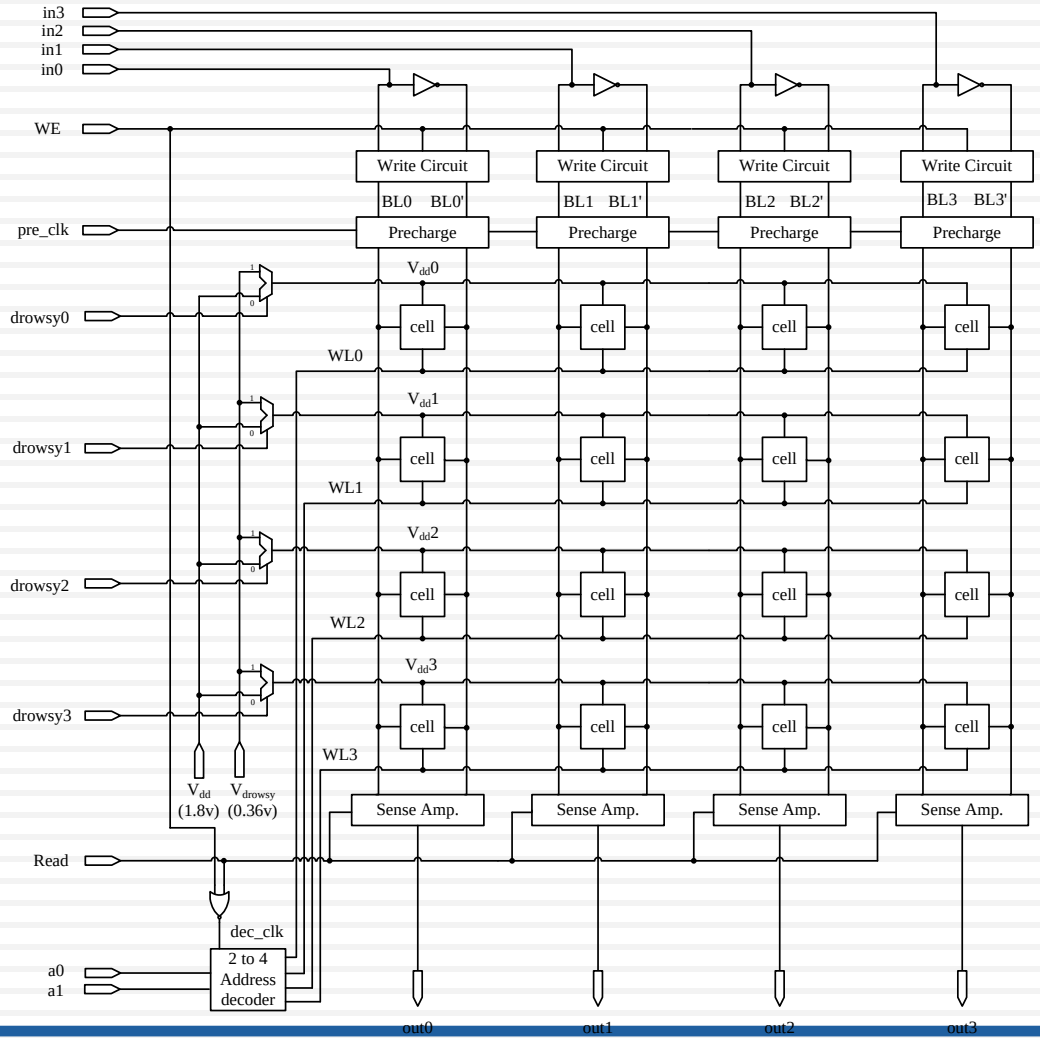


Figure 3.22 Dual-amplifier scheme for the sense amplifier network

An example: A Drowsy SRAM



Outline

- The Static RAM
- SRAM Arrays
- Dynamic RAM
- ROM Arrays
- Logic Arrays

DRAM (1/3)

- Dynamic RAM (DRAM)
  - Smaller than SRAM cells
  - Higher density storages arrays
  - As the central system memory in microcomputer systems
  - Require more peripheral circuitry

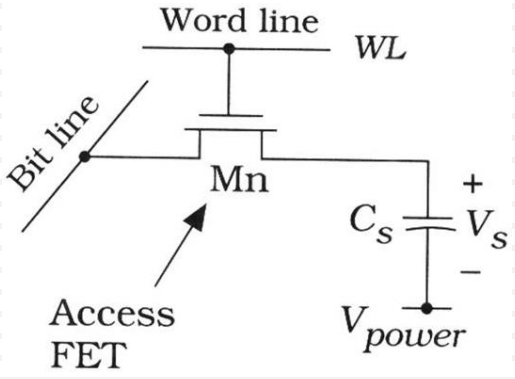


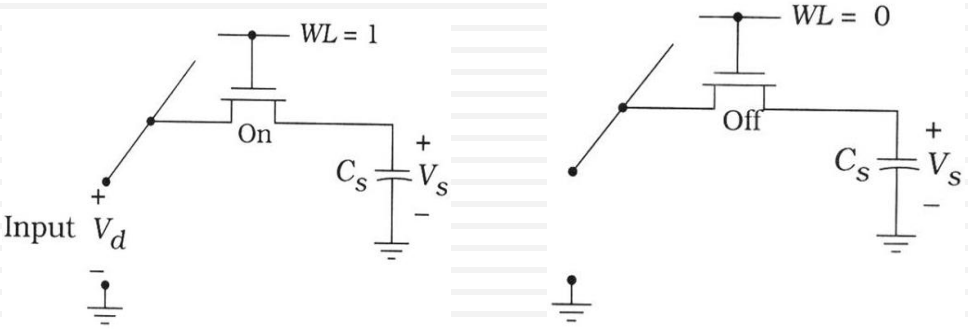
Figure 13.23 1T DRAM cell

$$Q_s = C_s V_s \qquad (13.8)$$

For writing 1,

$$V_s = V_{\max} = V_{DD} - V_{Tn} \qquad (13.9)$$

$$Q_{\max} = C_s (V_{DD} - V_{Tn}) \qquad (13.10)$$



(a) Write operation (b) Hold

Figure 3.24 Write and hold operations in a DRAM cell

DRAM (2/3)

- *Charge Leakage:* When $V_G < V_T$, a MOSFET is cutoff but still admits small leakage currents

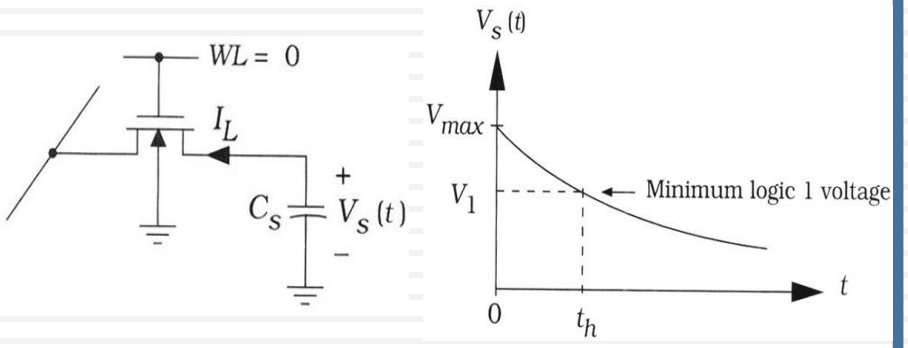


Figure 3.25 Charge leakage in a DRAM cell

$$I_L = -\left(\frac{dQ_s}{dt}\right) \quad (13.11)$$

$$I_L = -C_s\left(\frac{dV_s}{dt}\right) \quad (13.12)$$

$$I_L \approx -C_s\left(\frac{\Delta V_s}{\Delta t}\right) \quad (13.13)$$

$$t_h = |\Delta t| \approx \left(\frac{C_s}{I_L}\right)(\Delta V_s) \quad (13.14)$$ (hold time or retention time)

$$t_h = \left(\frac{50\times10^{-15}}{1\times10^{-9}}\right)(1) = 0.5\,\mu s \quad (13.15)$$ (I_L=1 nA, C_s=50 fF, and ΔV_s=1 V)

$$f_{refresh} \approx \frac{1}{2t_h} \quad (13.16)$$ (refresh frequency)

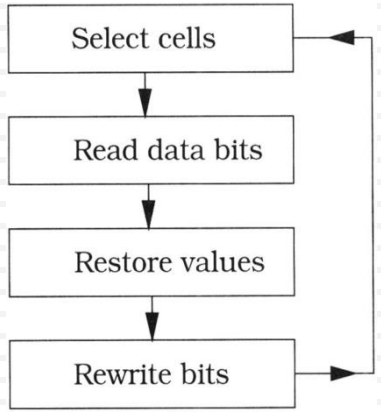


Figure 3.26 Refresh operation summary

DRAM (3/3)

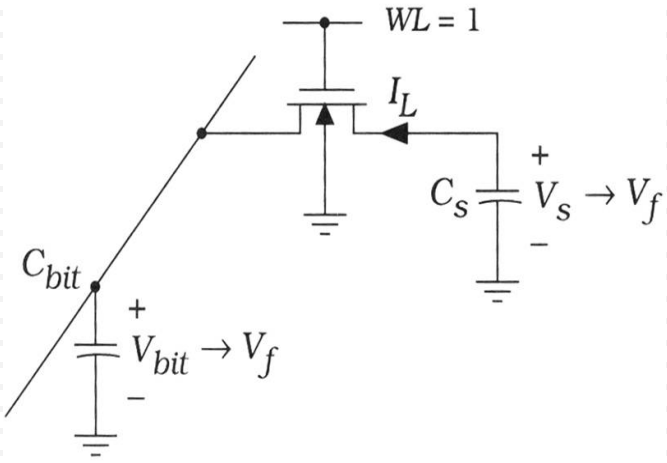


Figure 3.26 Read operation in a DRAM cell

$$Q_s = C_s V_s \qquad (13.17)$$

$$Q_s = C_s V_f + C_{bit} V_f \qquad (13.18)$$

$$V_f = \left(\frac{C_s}{C_s + C_{bit}} \right) V_s \qquad (13.19)$$

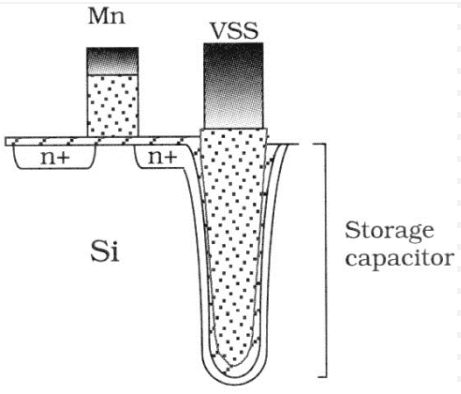


Figure 3.28 A DRAM cell using a trench capacitor

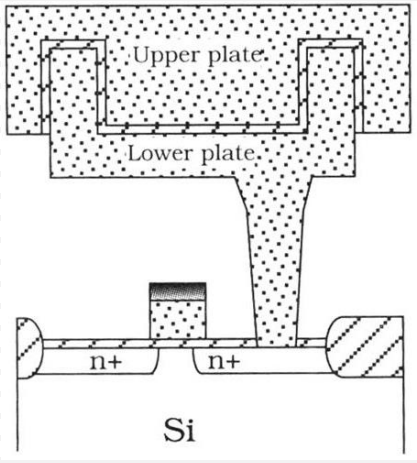
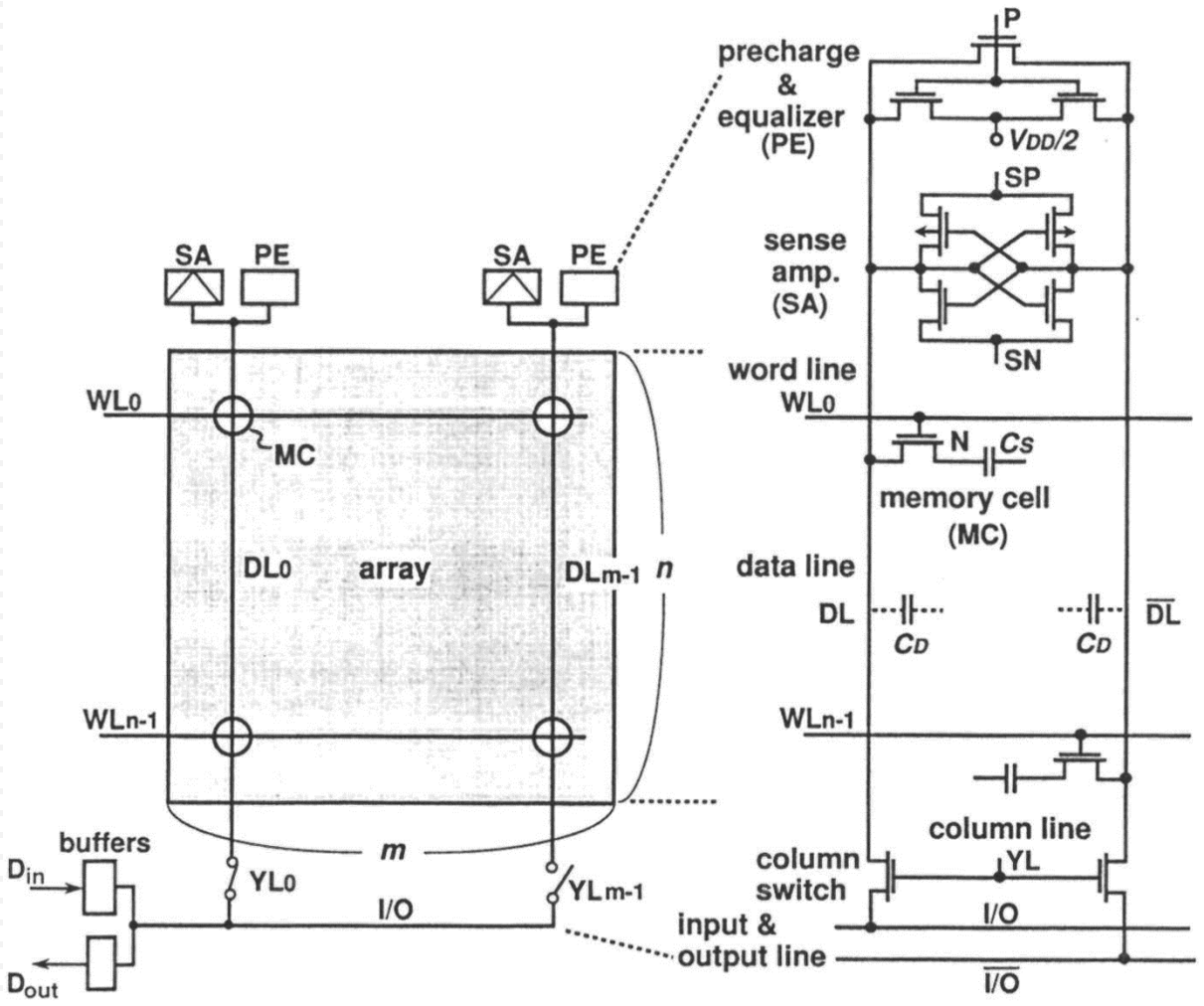


Figure 13.29 Visualization of stacked capacitor structure

DRAM Array and Peripheral Circuit



Divided-Word Line Architectures

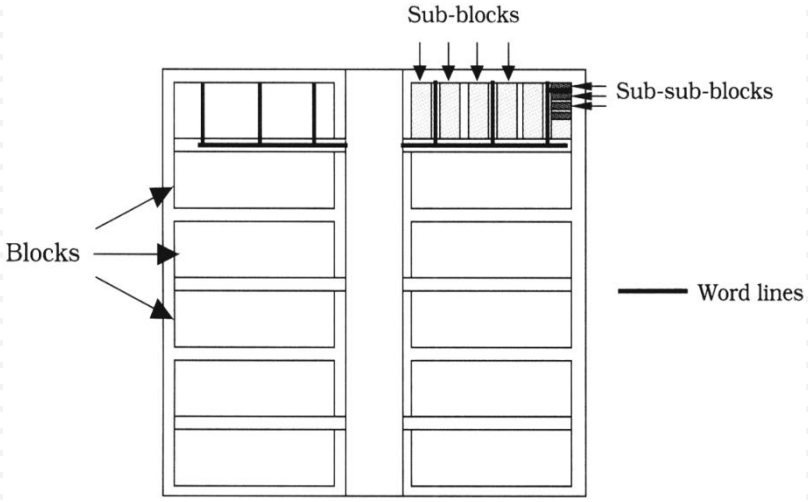


Figure 13.30 Basic for a divided-word line architecture RAM layout

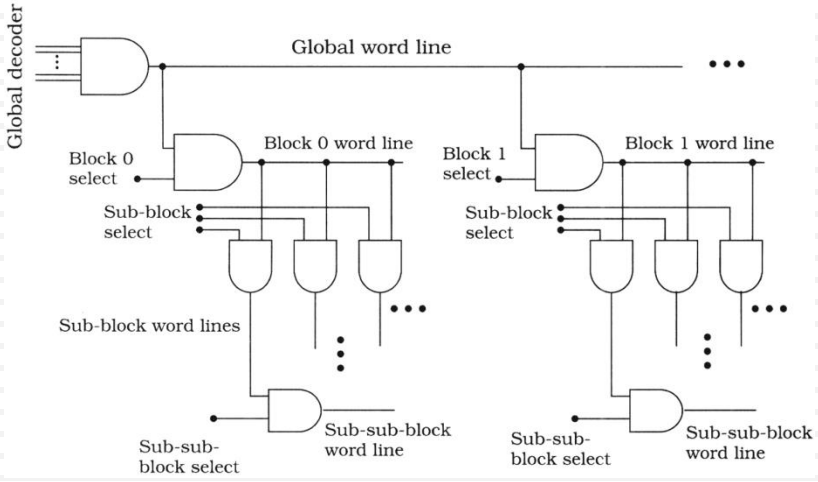
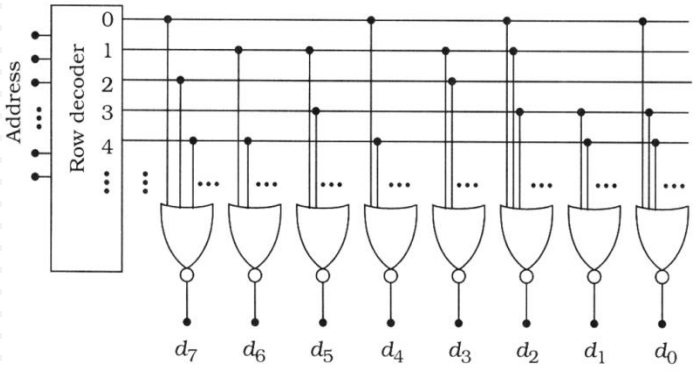


Figure 13.31 Logic for a DWL design

Outline

- The Static RAM
- SRAM Arrays
- Dynamic RAM
- ROM Arrays
- Logic Arrays

ROM



Row	Data
0	01101010
1	10010011
2	01110111
3	11011000
4	00101100

Figure 13.33 Logic diagram for a NOR-based ROM

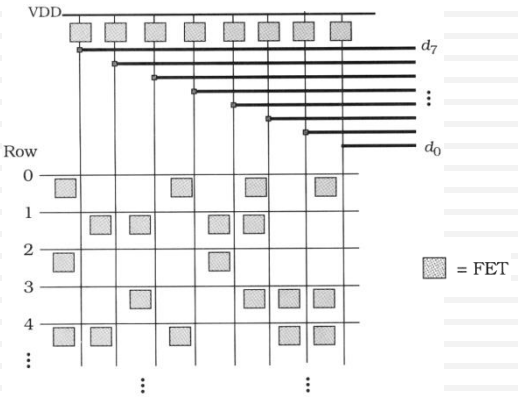


Figure 13.35 Map for ROM layout

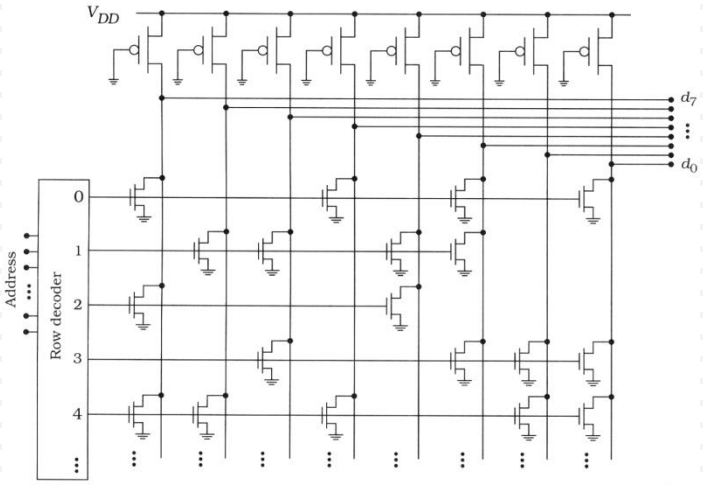


Figure 13.34 ROM array using pseudo-nMOS circuitry

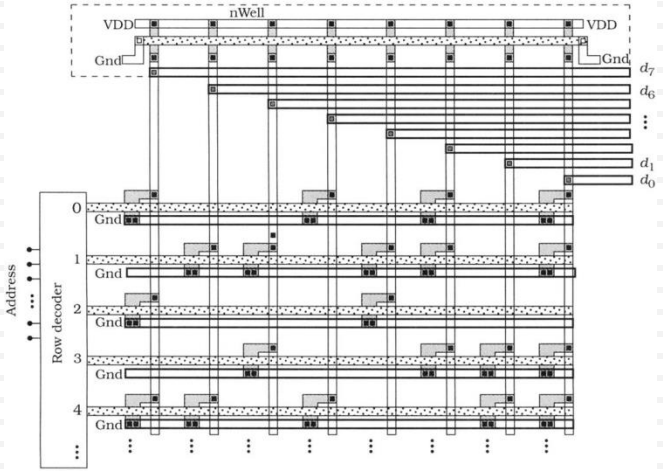
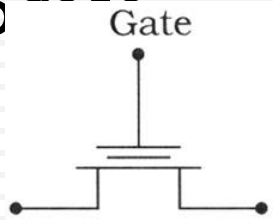


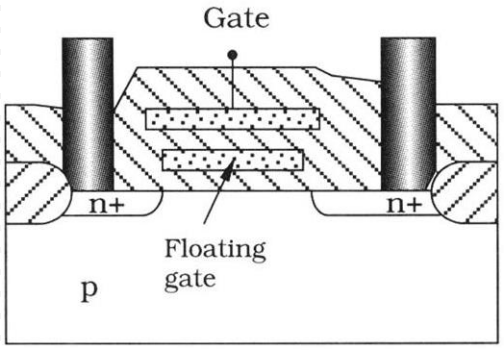
Figure 13.36 ROM layout based on FET map

User-Programmable ROMs

- Electrically-erasable EPROMs (E^2PROMs) are used to store the BIOS code in PC, and allow the user to up

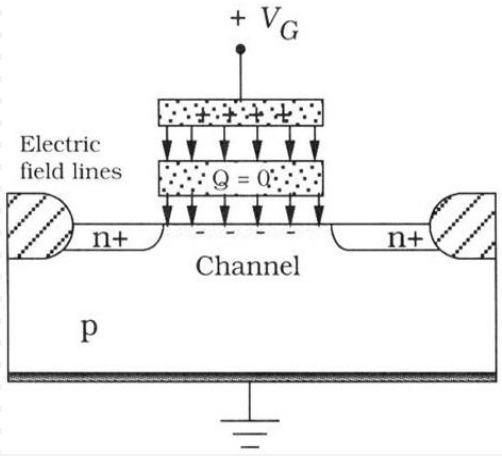


(a) Symbol

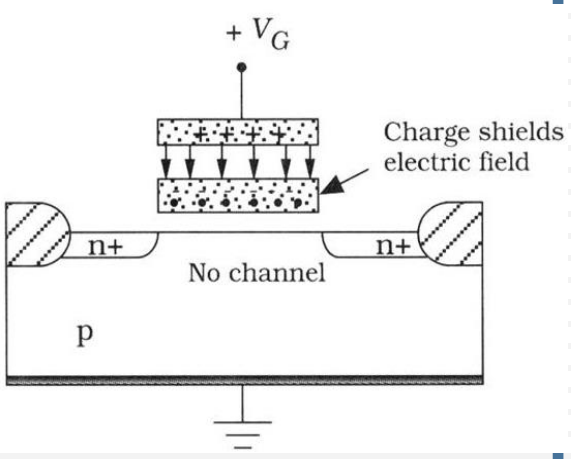


(b) Structure

Figure 13.37 Floating-gate MOSFET



(a) Normal V_{Tn} state



(b) Increased $V_{Tn,H}$ state

Figure 13.33 Logic diagram for a NOR-based ROM

E²PROMs

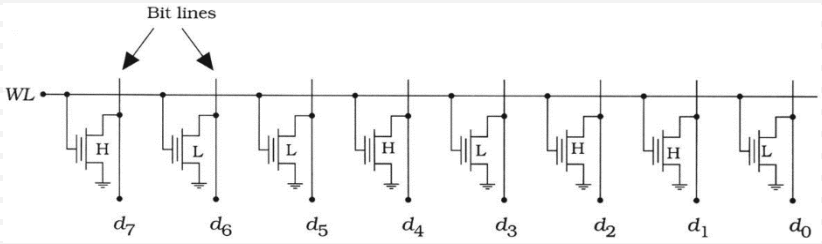


Figure 13.39 A E²PROM word using floating-gate nFETs

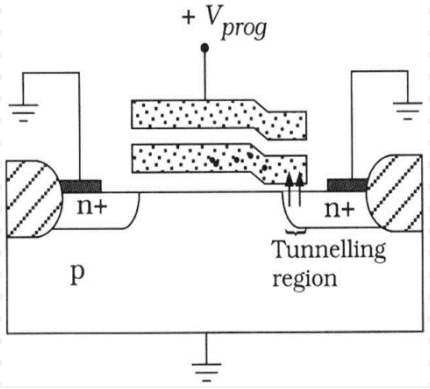


Figure 13.41 Fowler-Nordheim tunnelling

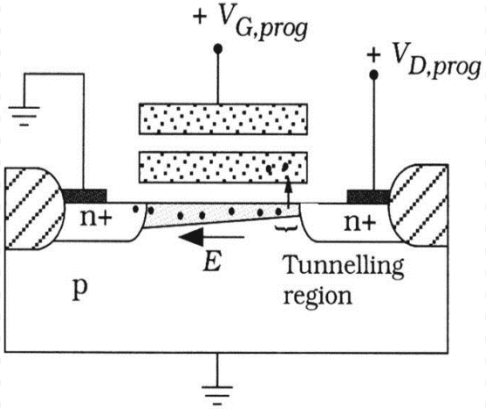


Figure 13.40 Programming a floating-gate FET

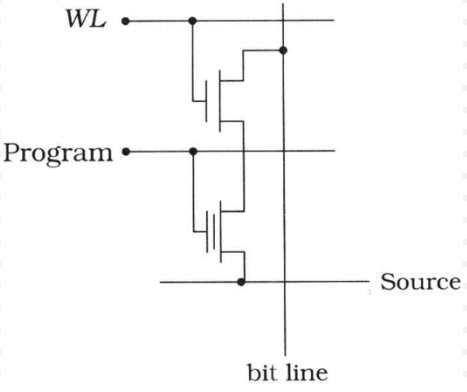


Figure 13.42 EEPROM cell with write line

Outline

- The Static RAM
- SRAM Arrays
- Dynamic RAM
- ROM Arrays
- Logic Arrays

Programmable Logic Array, PLA (1/2)

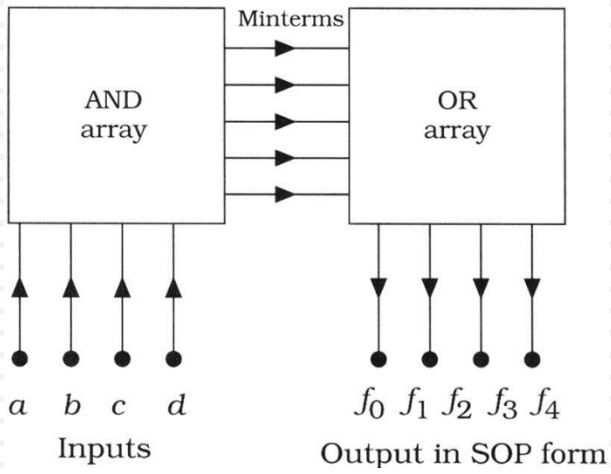


Figure 13.43 Structure of an AND-OR PLA

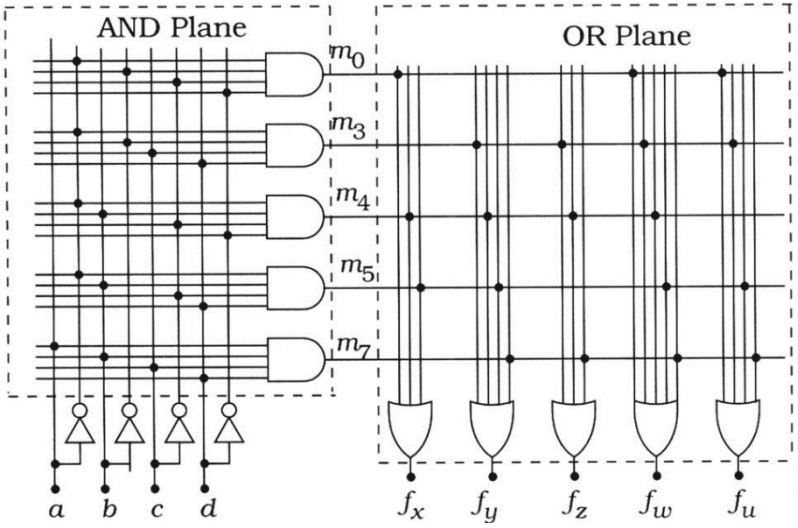
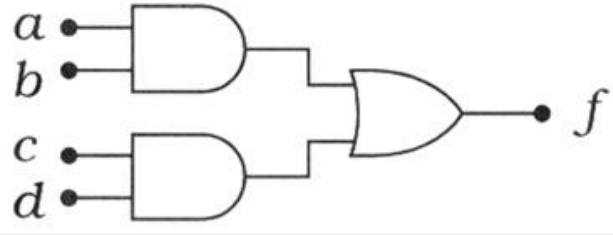
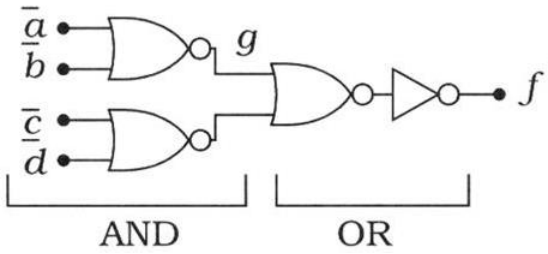


Figure 13.44 Logic gate diagram of the PLA

Programmable Logic Array, PLA (2/2)



(a) AND-OR logic



(b) NOR-based logic

Figure 13.45 NOR-gate PLA logic

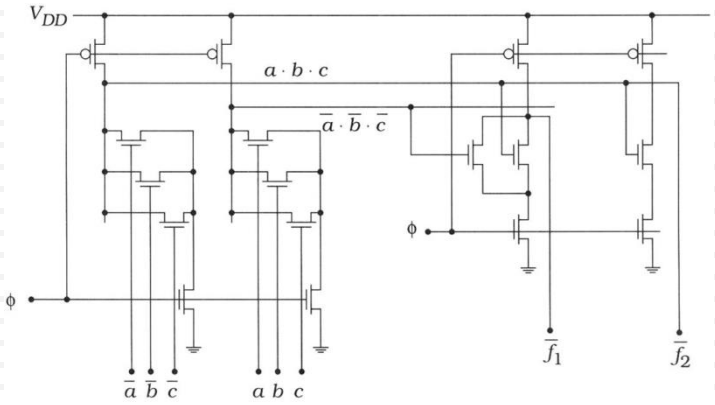


Figure 13.46 A dynamic CMOS PLA based on NOR gates

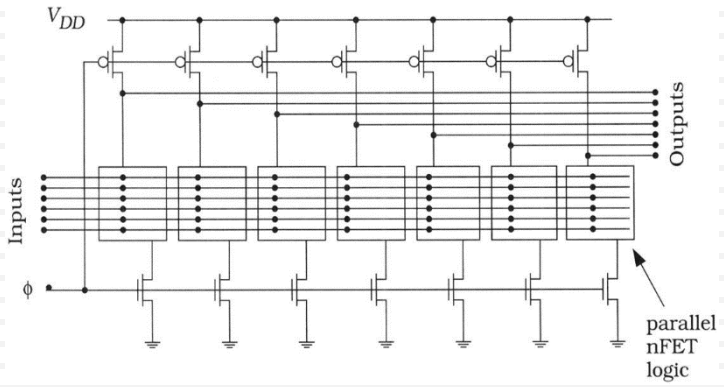
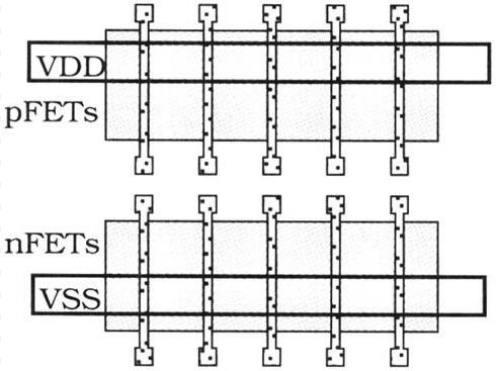
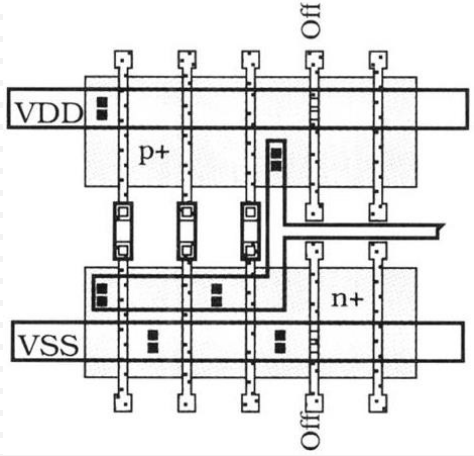


Figure 13.47 Generic NOR-based logic plane

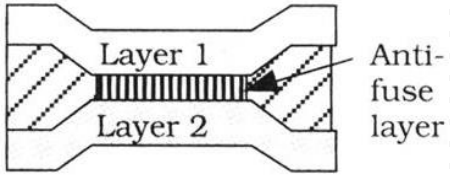
Gate Array



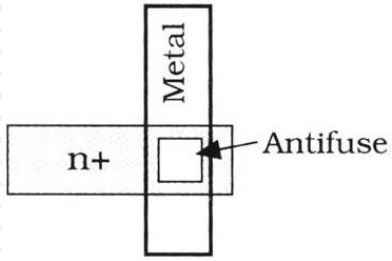
(a) Gate array based



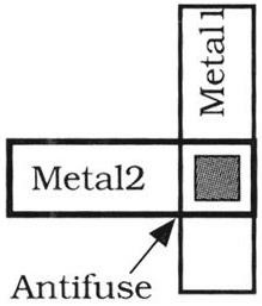
(b) NOR3 gate wiring



(a) Structure



(b) Metal-active



(c) Metal-metal

Figure 13.45 NOR-gate PLA logic

Figure 13.48 Transistor arrangement in a gate array