GENERAL VLSI SYSTEM COMPONENTS

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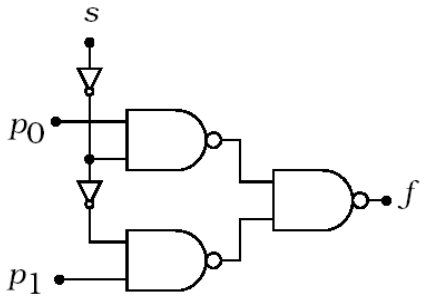
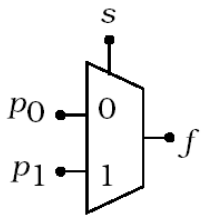
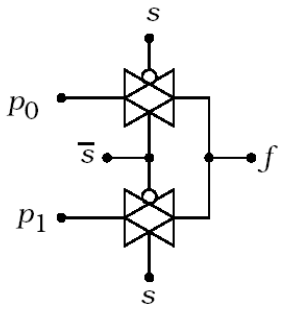
Multiplexers

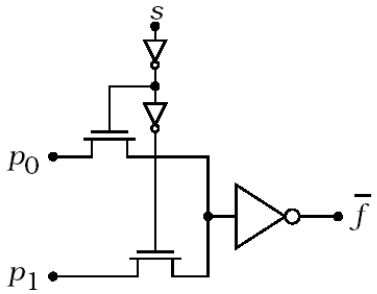




Gate-level NAND 2:1 multiplexor.

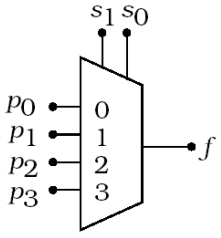


(a) TG circuit

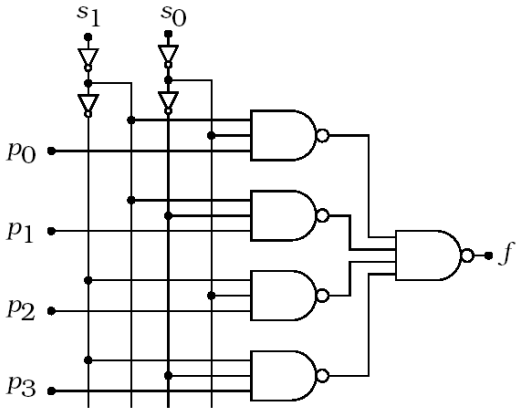


(b) Pass transistors

Multiplexor using switch logic.

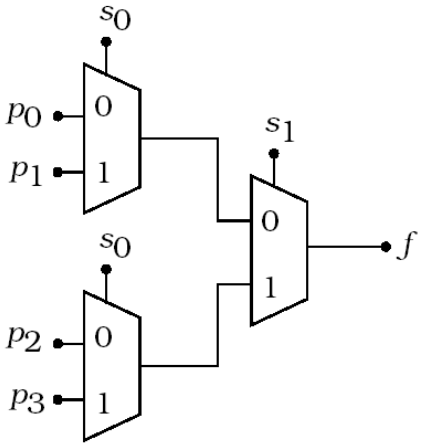


(a) Symbol



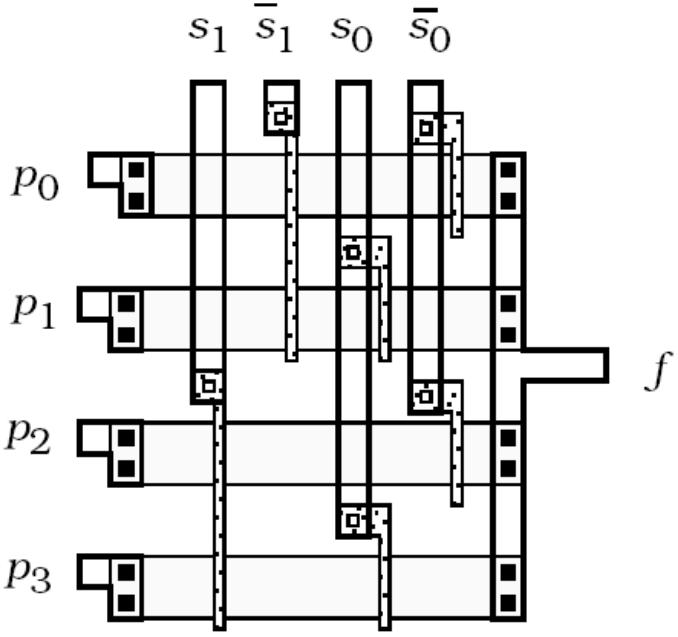
(b) Logic diagram

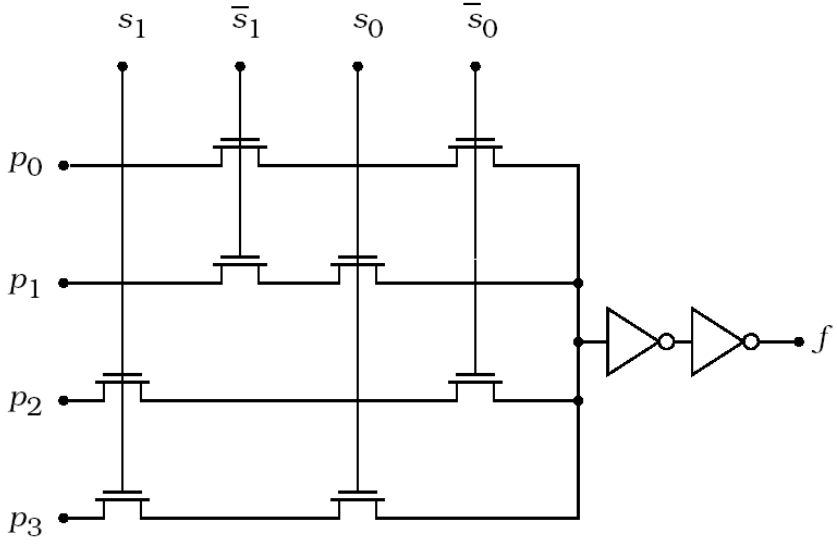
Gate-level 4:1 MUX



A 4:1 MUX using instanced 2:1 devices.

Multiplexers (2)

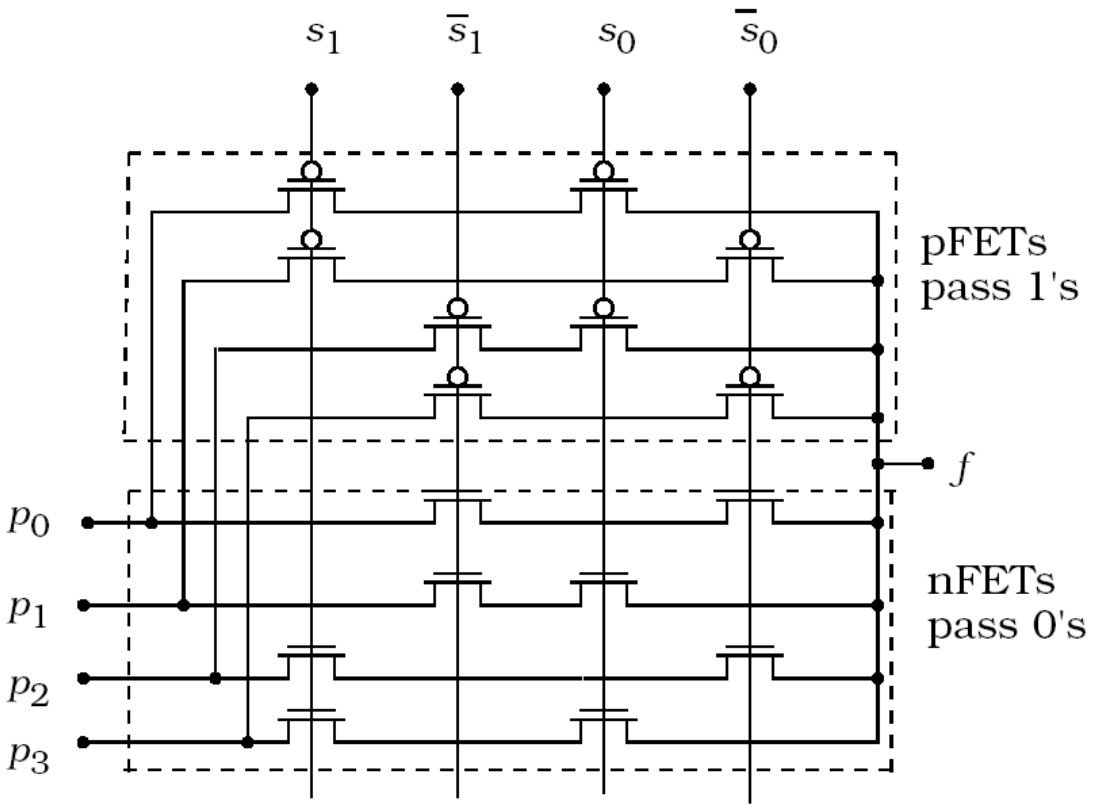




4:1 MUX using nFET pass transistors.

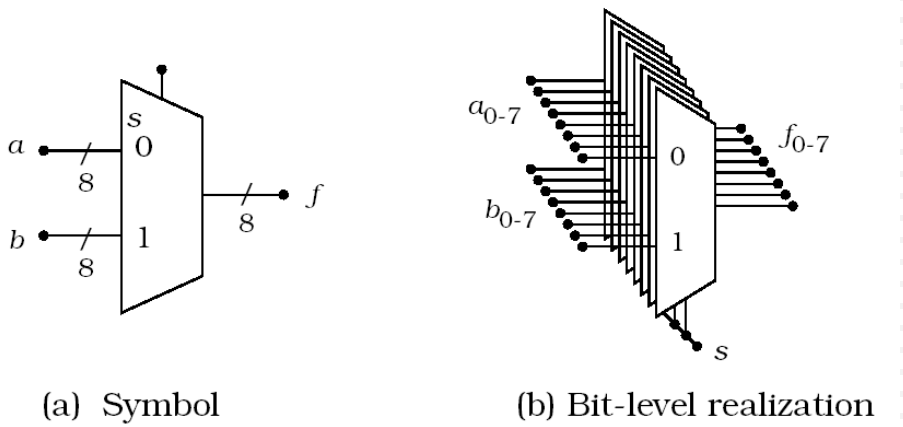
Simple 4:1 pass-FET MUX layout.

Multiplexers (3)



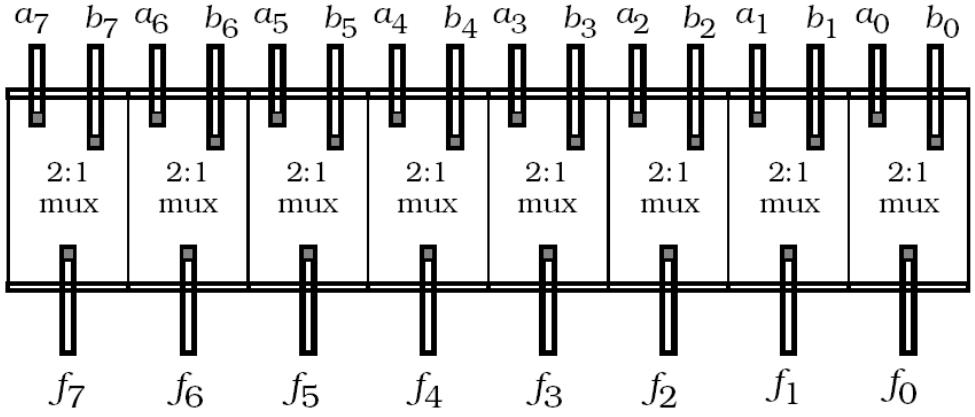
Split-array 4:1 MUX for full-rail output.

Multiplexers (4)



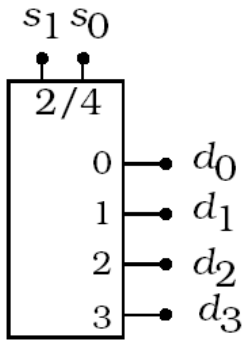
(a) Symbol (b) Bit-level realization

A vector 2:1 MUX.



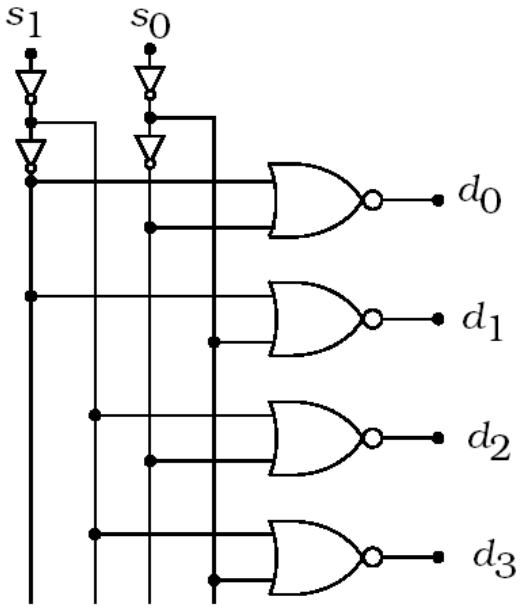
Single-bit cell tiling for an 8-bit 2:1 MUX.

Decoders



s_1	s_0	d_0	d_1	d_2	d_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

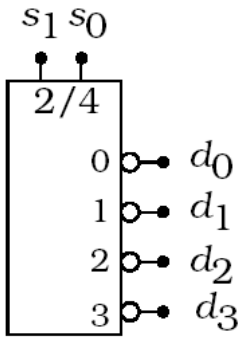
(a) Symbol and table



(b) NOR2 implementation

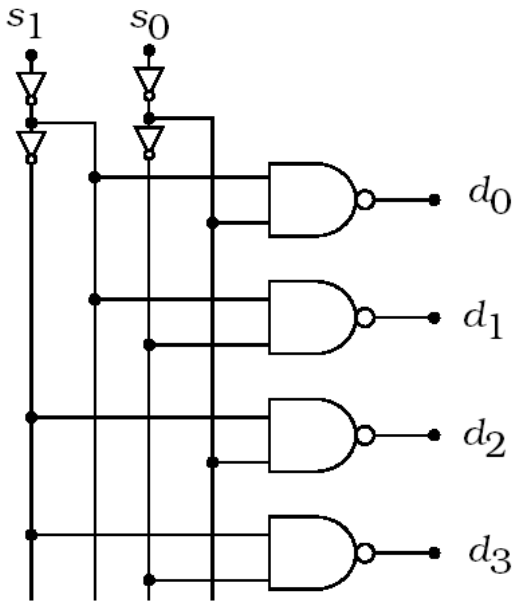
An active-high 2/4 decoder.

Decoders (2)



s_1	s_0	d_0	d_1	d_2	d_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

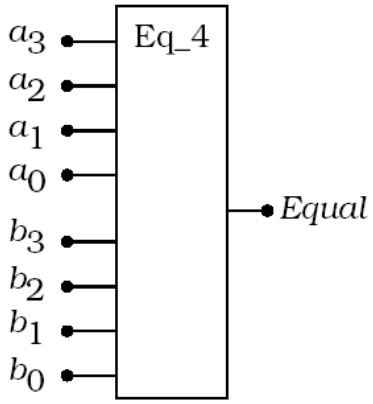
(a) Symbol and table

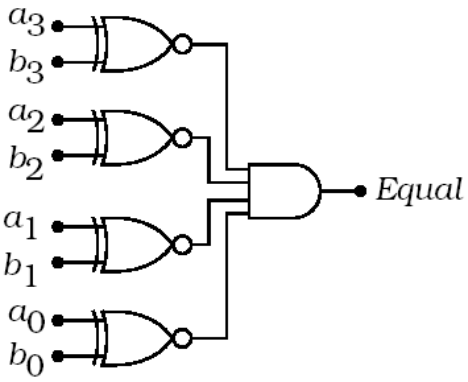


(b) NAND2 implementation

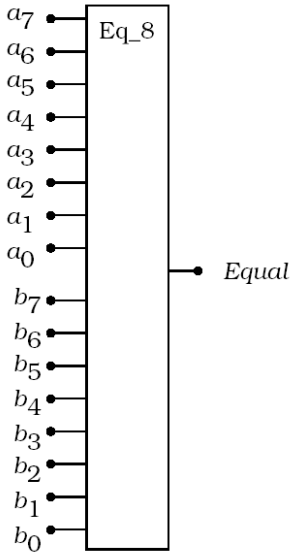
Active low 2/4 decoder.

Comparators

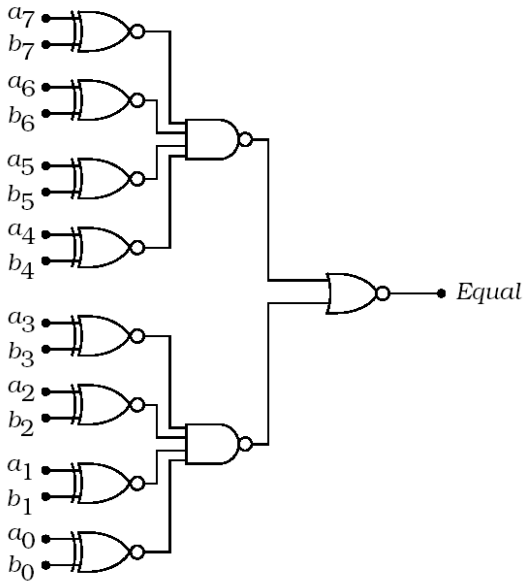




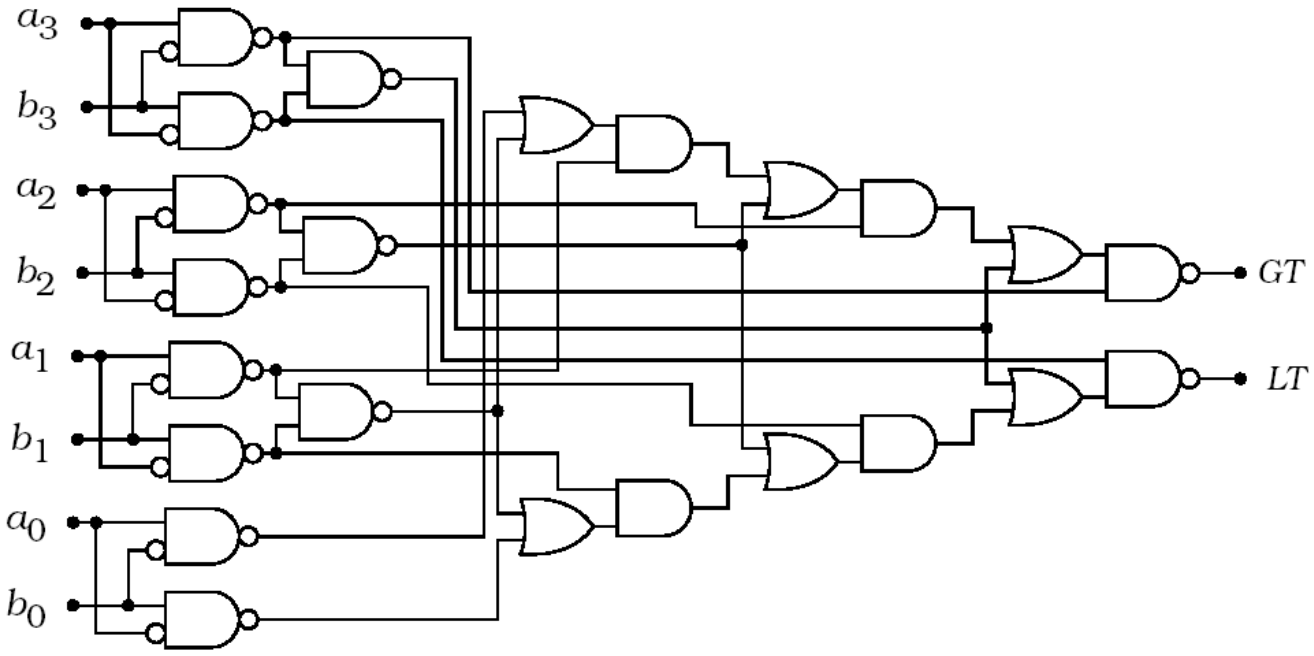
a 4-bit equality detector.



8-bit equality detector.



Comparators (2)

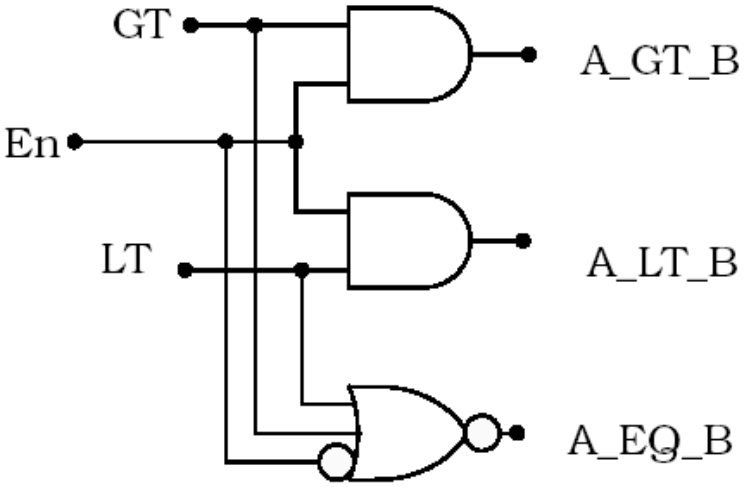


4-bit magnitude comparator logic.

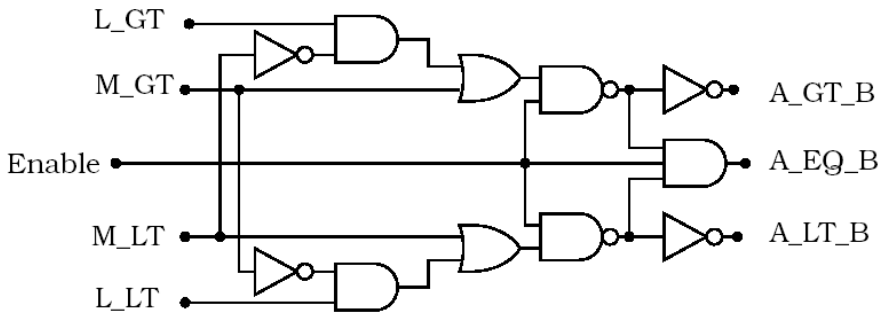
Comparator output summary.

Condition	GT	LT
$a > b$	1	0
$a < b$	0	1
$a = b$	0	0

Comparators (3)

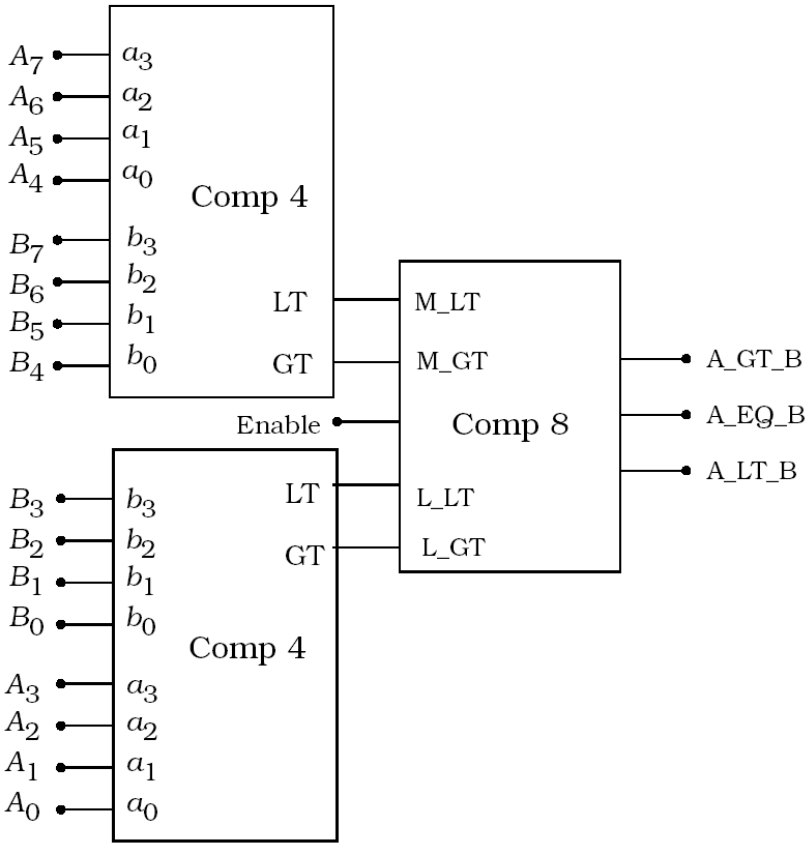


Additional logic for A_EQ_B and Enable features.



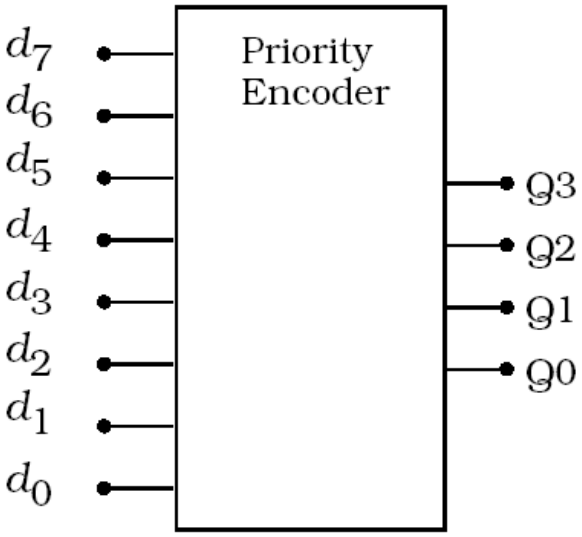
Comp 8 logic diagram.

Comparators (4)



8-bit comparator system.

Encoders



Symbol for priority encoder

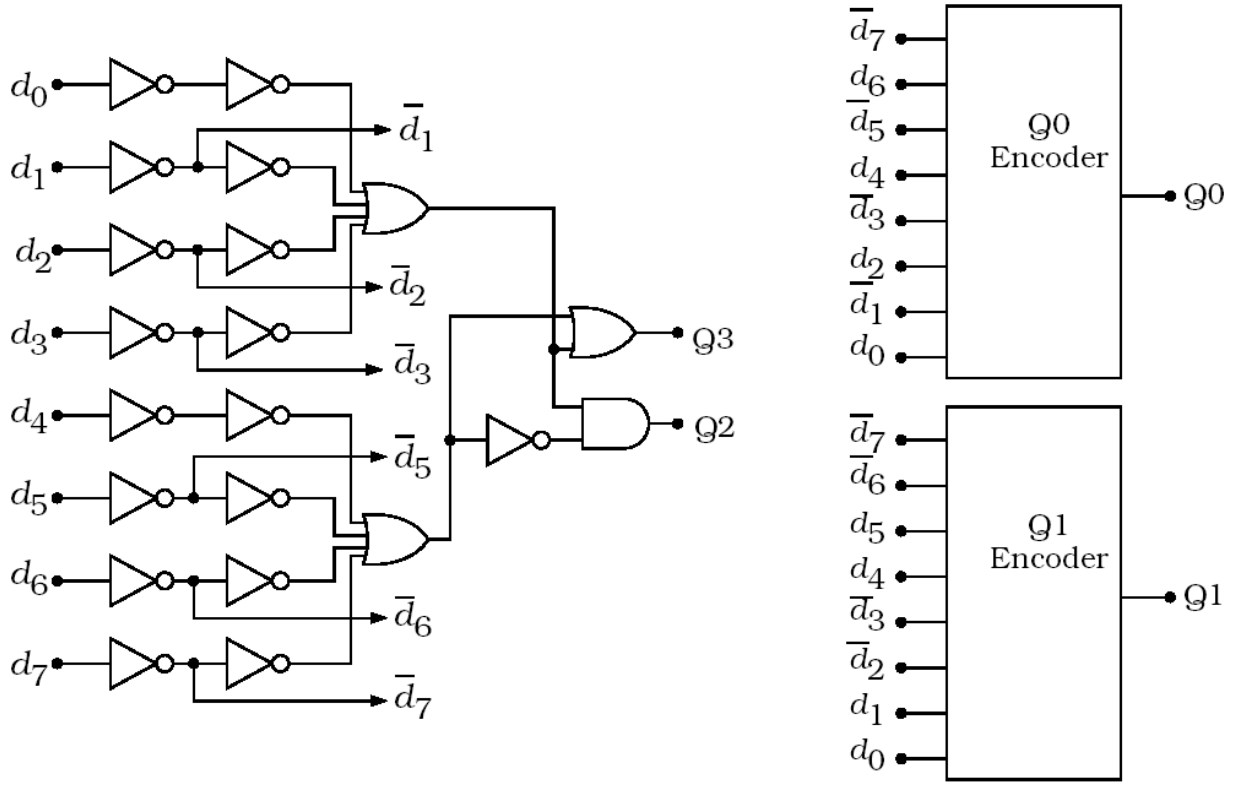
d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	1	0	0	0
0	0	0	0	0	0	1	-	1	0	0	1
0	0	0	0	0	1	-	-	1	0	1	0
0	0	0	0	1	-	-	-	1	0	1	1
0	0	0	1	-	-	-	-	1	1	0	0
0	0	1	-	-	-	-	-	1	1	0	1
0	1	-	-	-	-	-	-	1	1	1	0
1	-	-	-	-	-	-	-	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0

d_7 has highest priority
d_0 has lowest priority

$Q_3 = 1$ when $d_i = 1$ for any $i = 0, \ldots, 7$

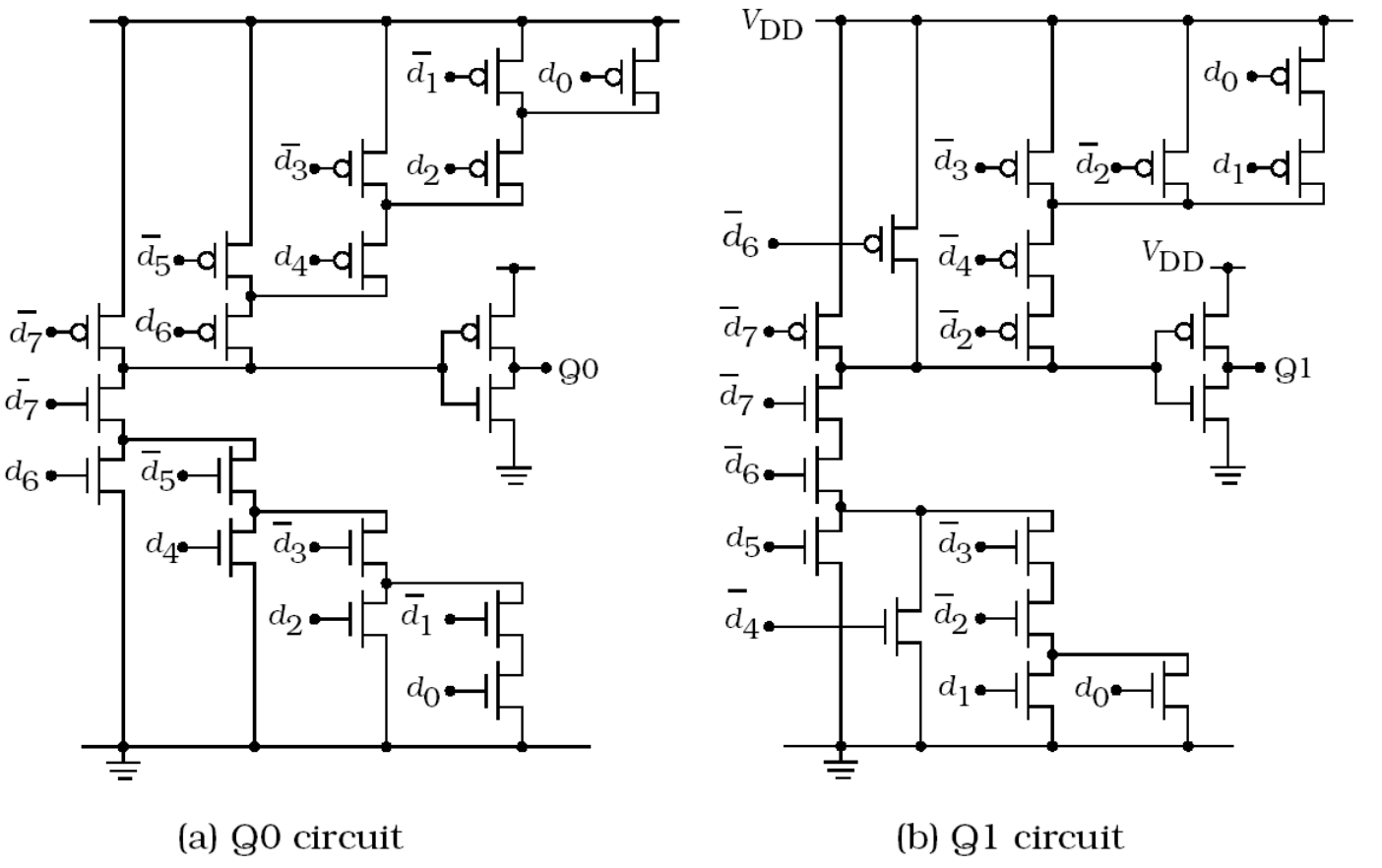
Function table for an 8-bit priority encoder.

Encoders (2)



Logic diagram for the priority encoder.

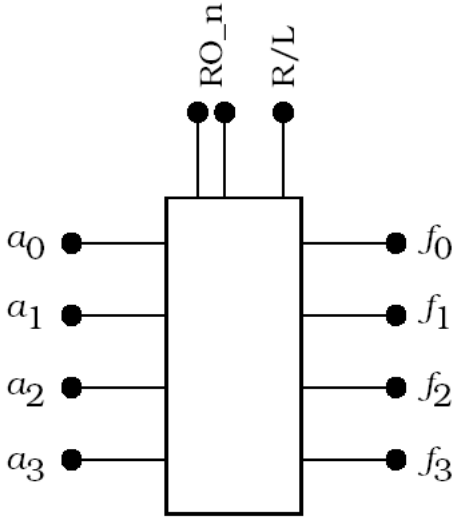
Encoders (3)



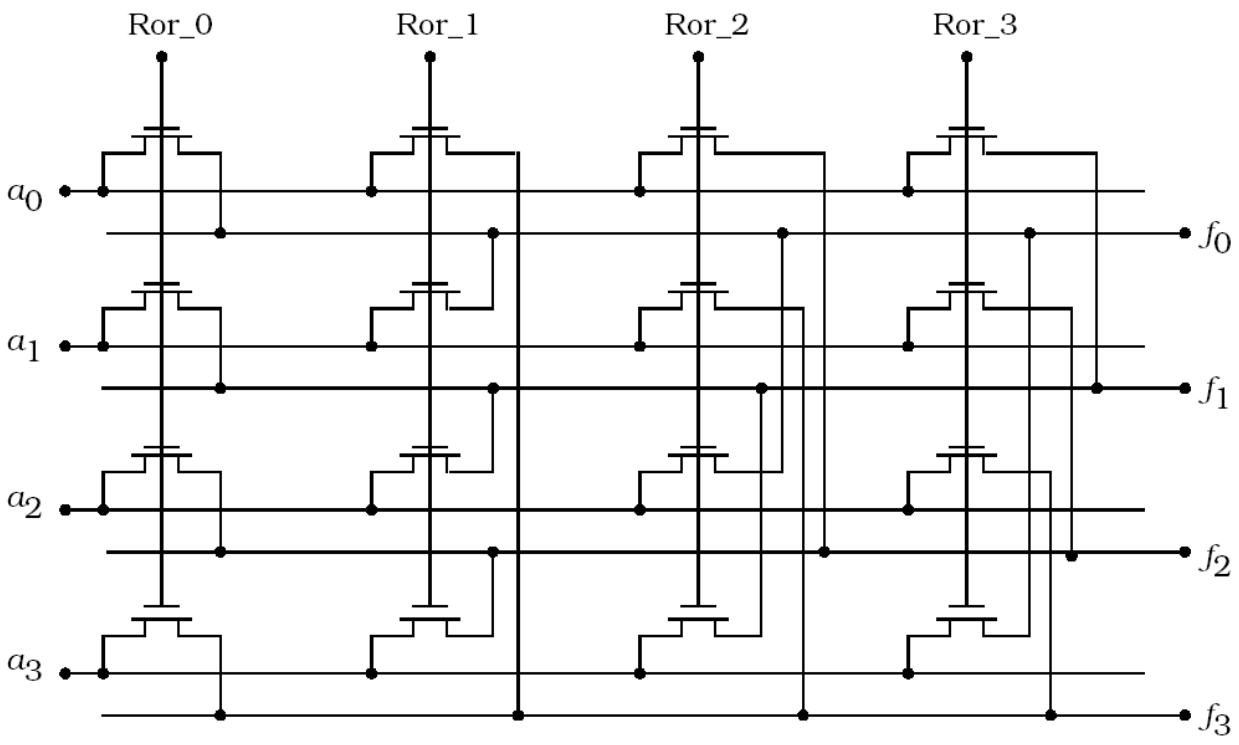
(a) Q0 circuit (b) Q1 circuit

Q0 and Q1 circuits for the 8-bit priority encoder.

Rotators and Shifters

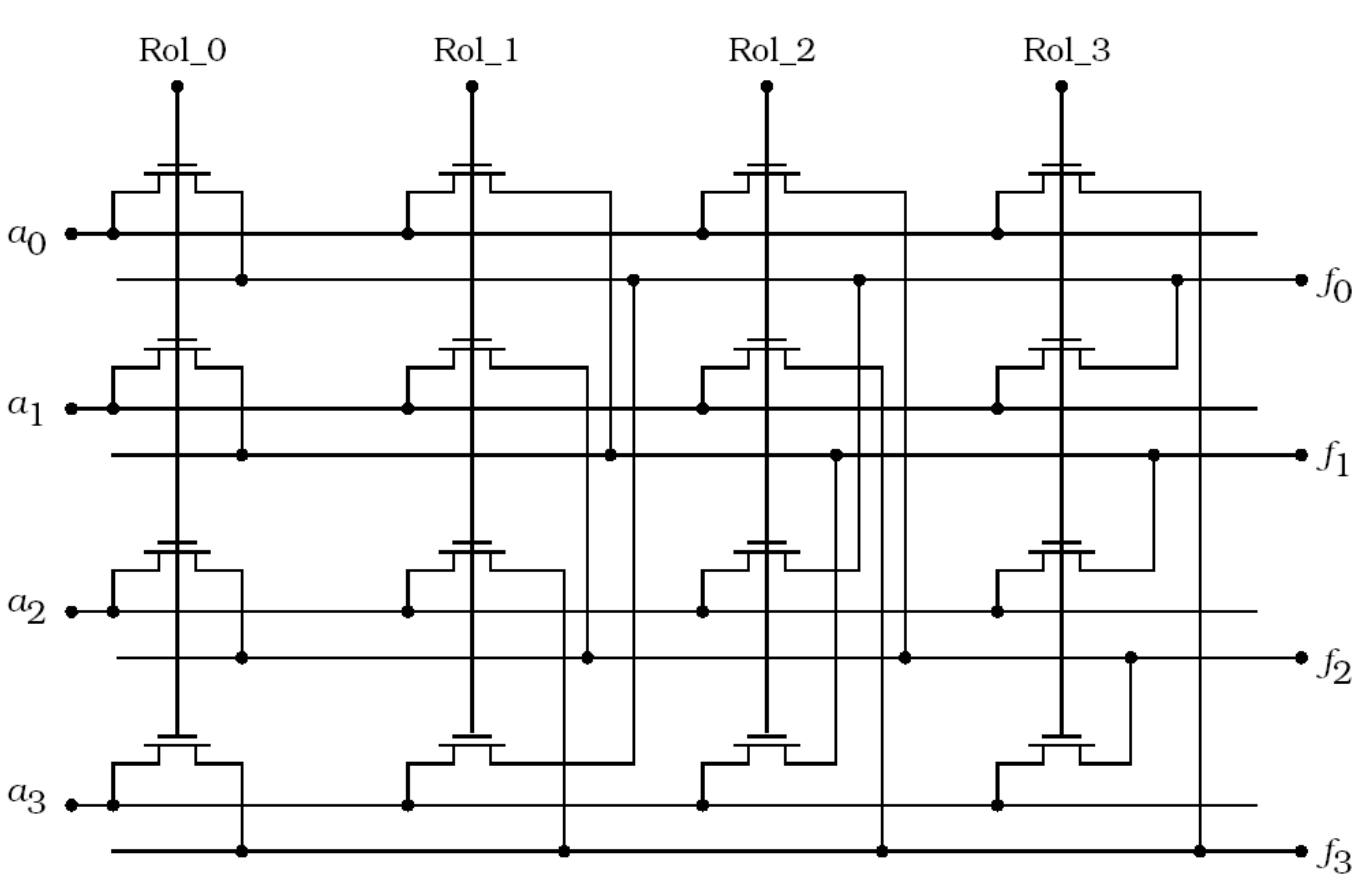


General rotator.



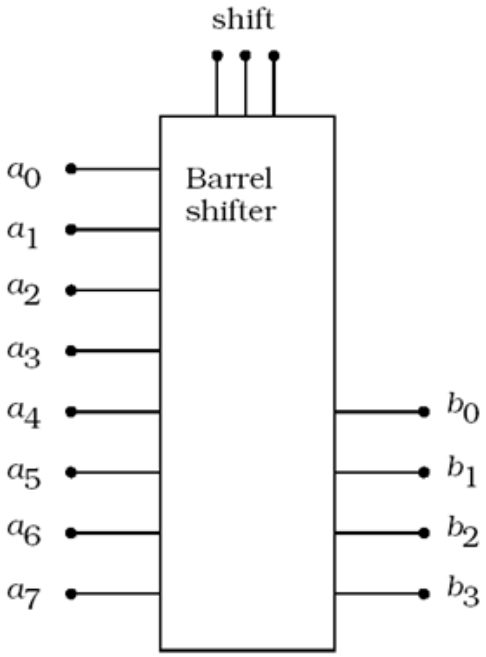
A 4-bit rotate-right network.

Rotators and Shifters (2)



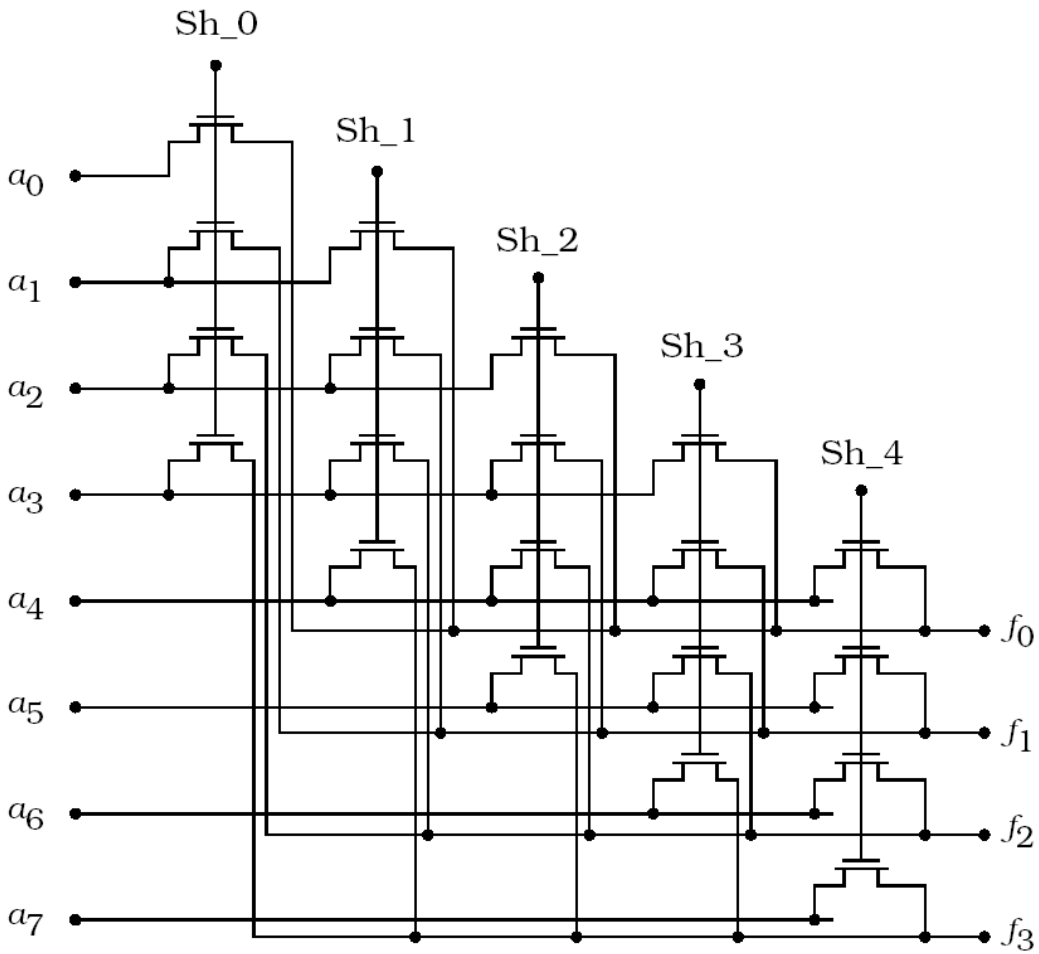
Left-rotate switching array.

Rotators and Shifters (3)



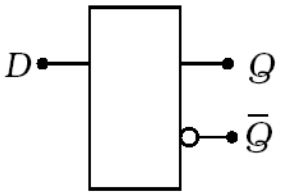
shift	$b_0 b_1 b_2 b_3$
0	$a_0 a_1 a_2 a_3$
1	$a_1 a_2 a_3 a_4$
2	$a_2 a_3 a_4 a_5$
3	$a_3 a_4 a_5 a_6$
4	$a_4 a_5 a_6 a_7$

An 8 X 4 barrel shifter.

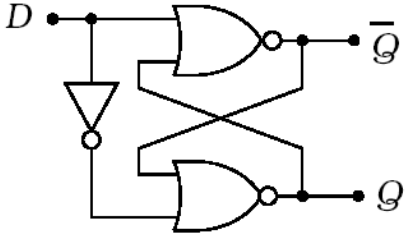


FET-array barrel shifter.

Latches and Flip-Flops

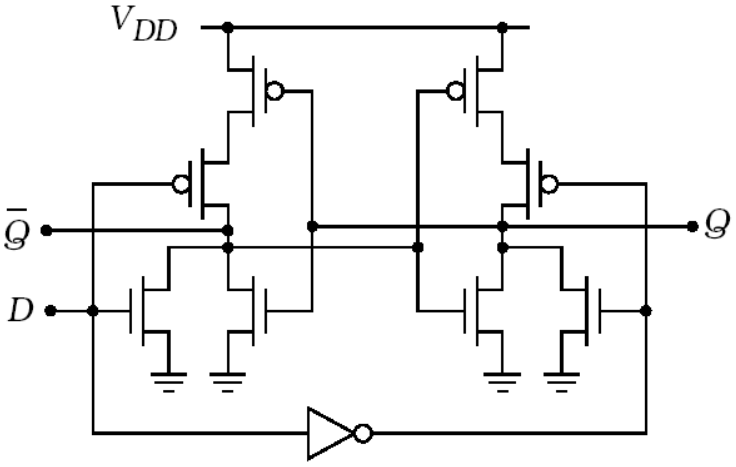


(a) Symbol

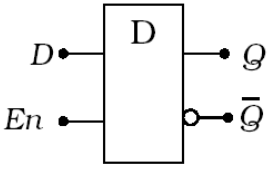


(b) Logic diagram

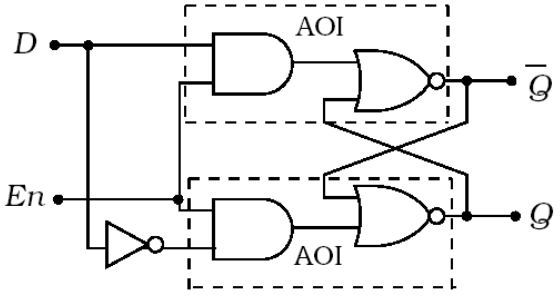
D-latch.



CMOS circuit for a D-latch.

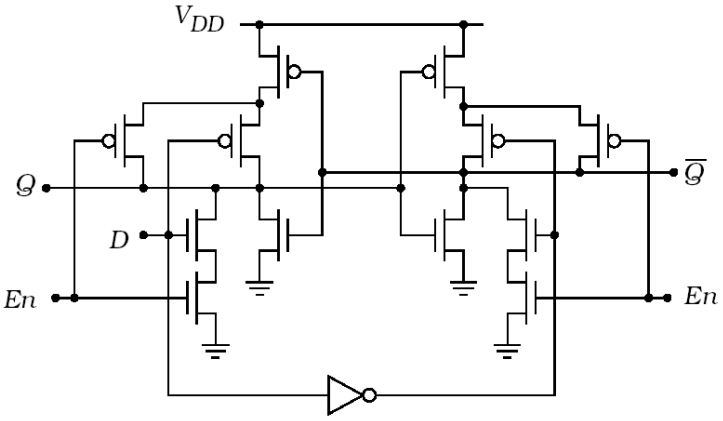


(a) Symbol



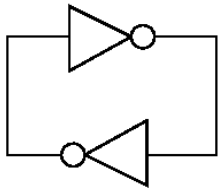
(b) Logic diagram

Gated D-latch with *Enable* control.

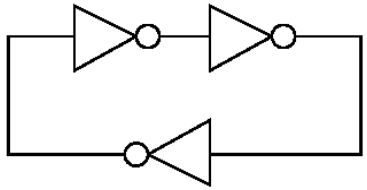


AOI CMOS gate for D-latch with *Enable*.

Latches and Flip-Flops (2)

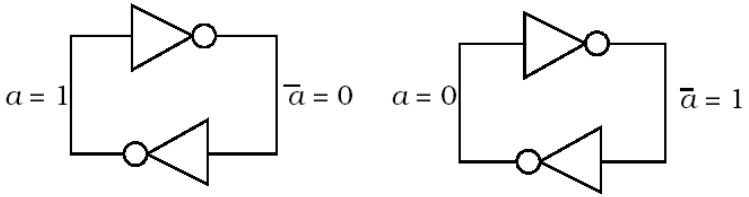


(a) Bistable circuit

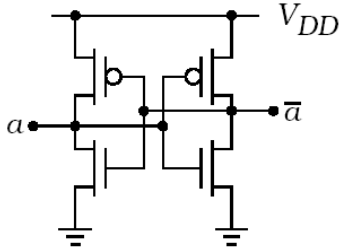


(b) Ring oscillator

Closed-loop inverter configurations.



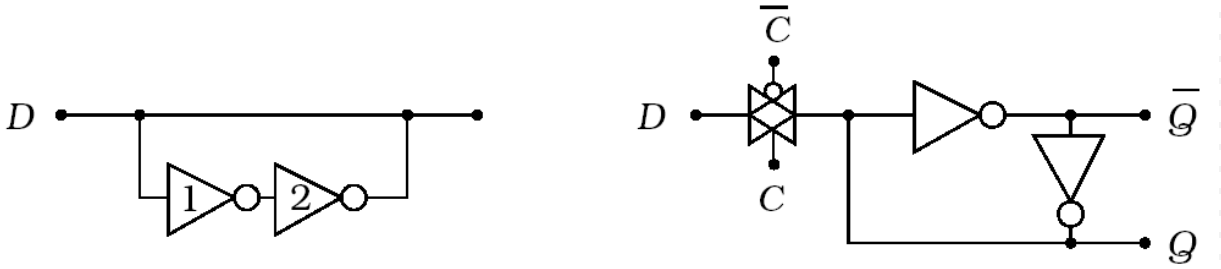
(a) Stable states



(b) CMOS circuit

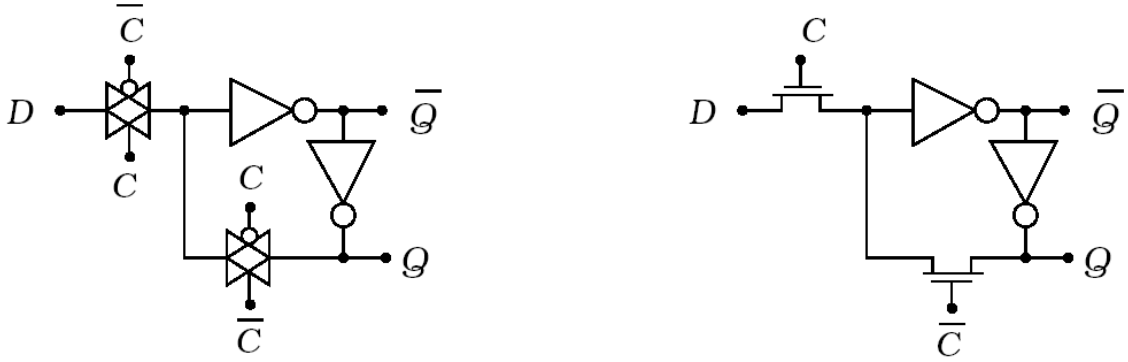
Operation of a bistable circuit.

Latches and Flip-Flops (3)



(a) Receiver circuit (b) Controlled loading

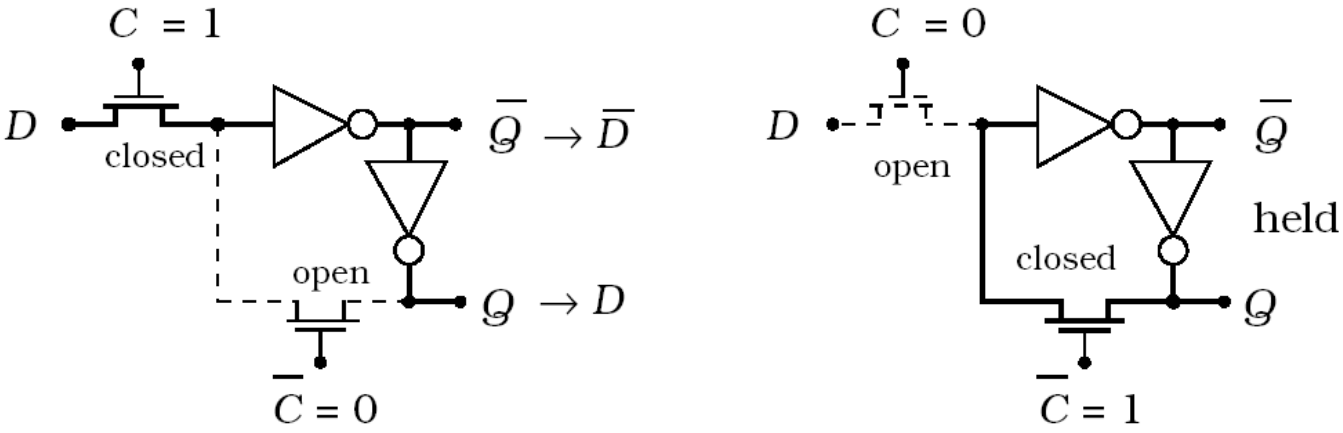
Adding an input node to the bistable circuit.



(a) CMOS TG version (b) nFET pass gates

D-latch using oppositely phased switches.

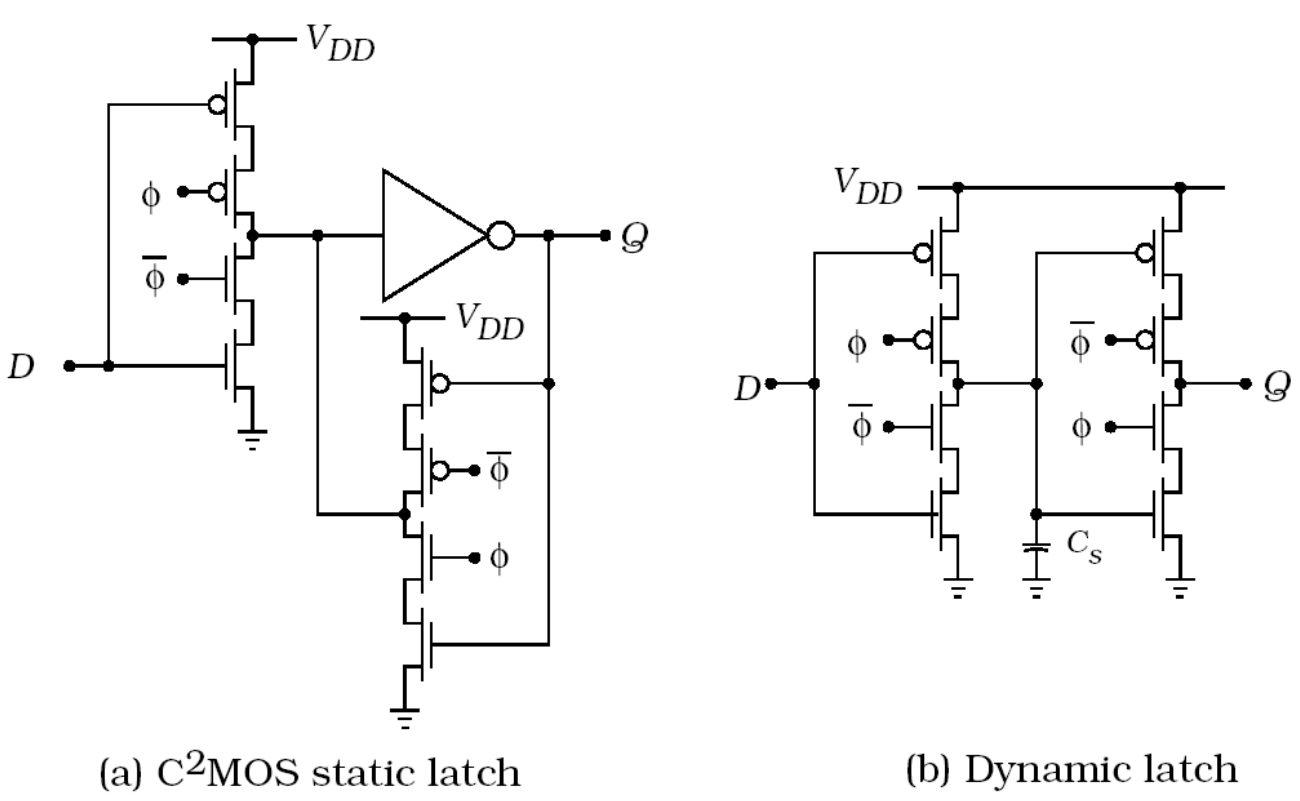
Latches and Flip-Flops (4)



(a) Load with $C = 1$ (b) Hold with $C = 0$

Operation of the D-latch.

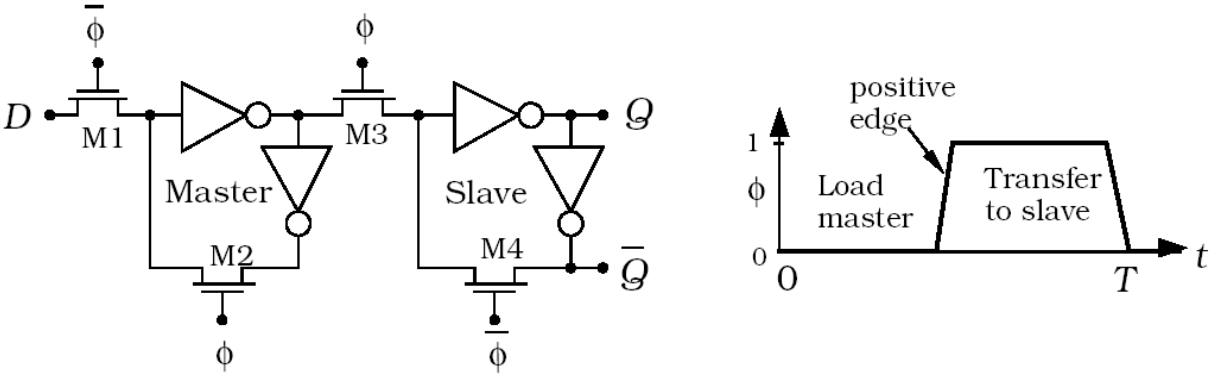
Latches and Flip-Flops (5)



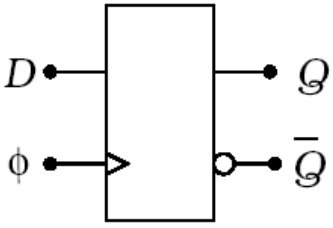
(a) C^{2}MOS static latch (b) Dynamic latch

C2MOS-based D-latch circuits.

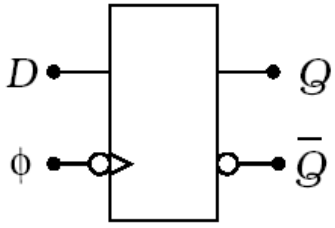
Latches and Flip-Flops (6)



Master-slave D-type flip-flop.



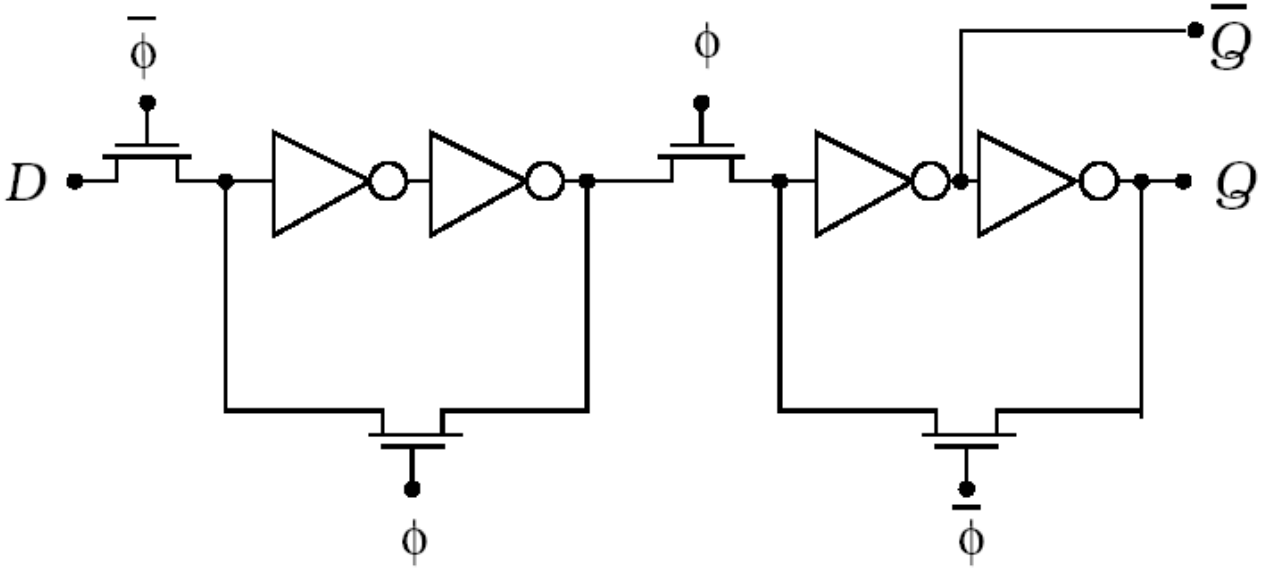
(a) Positive edge-triggered DFF



(b) Negative edge-triggered DFF

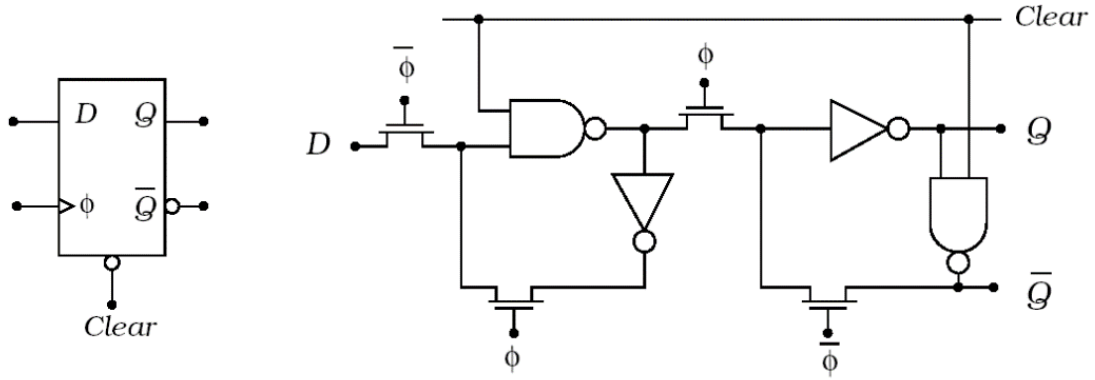
Edge-triggered DFF symbols.

Latches and Flip-Flops (7)

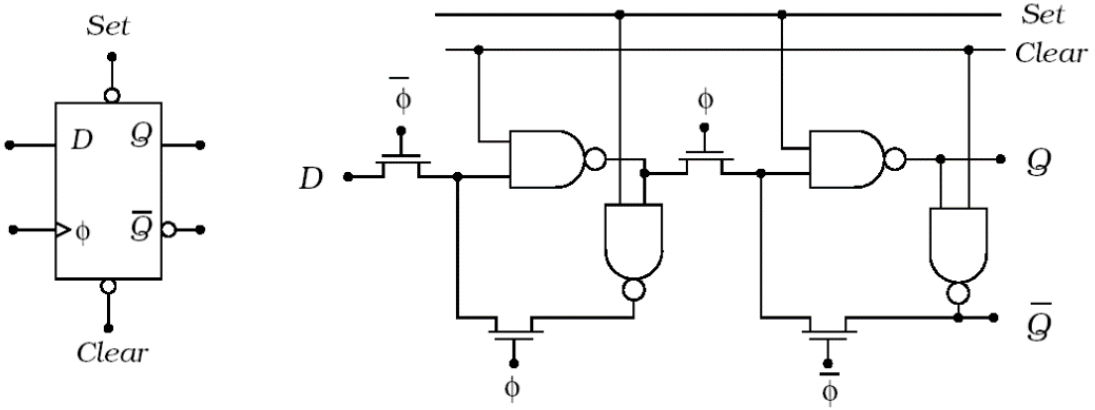


Alternate circuitry for the master-slave DFF.

Latches and Flip-Flops (8)



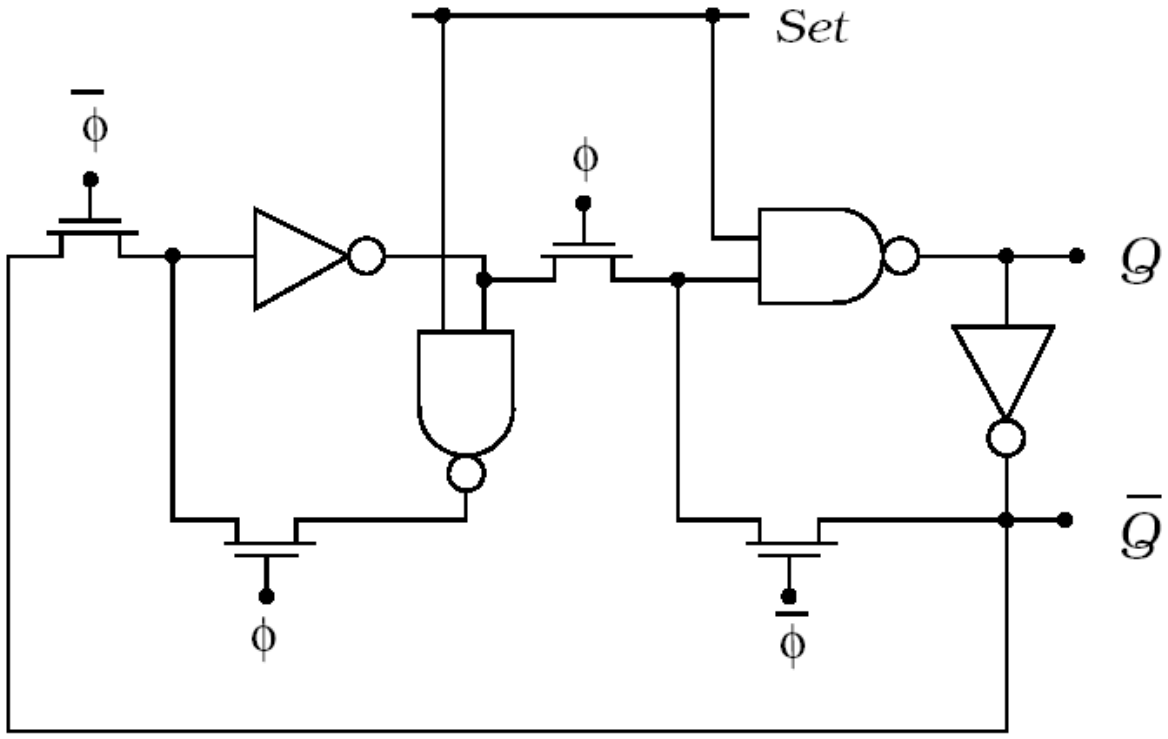
(a) DFF with direct Clear



(b) DFF with direct Clear and Set

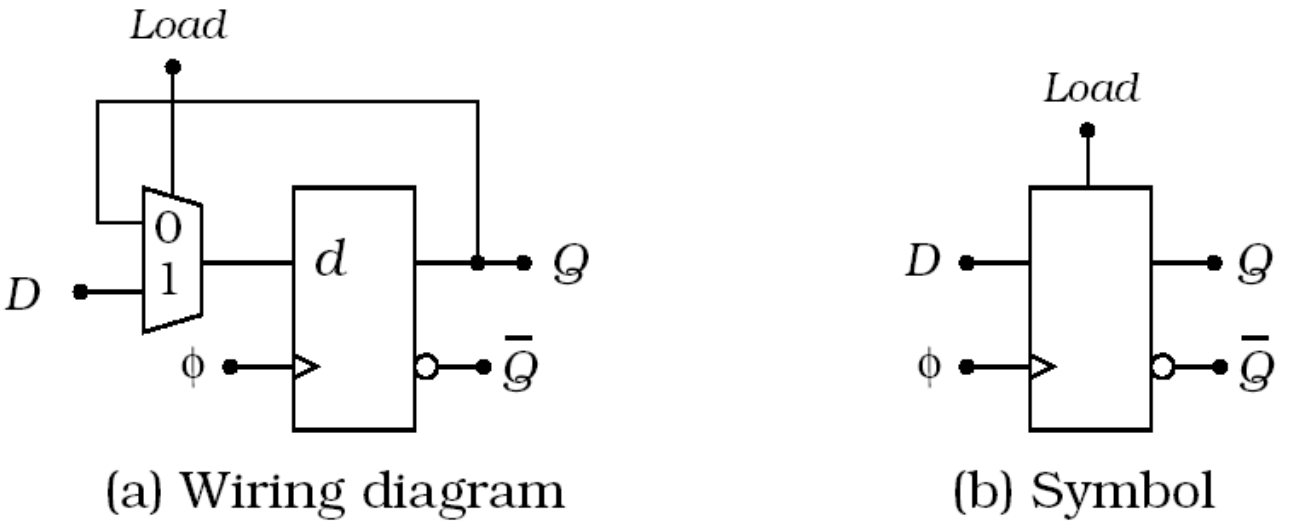
DFF circuits with assert-low Clear and Clear/Set controls.

Latches and Flip-Flops (9)



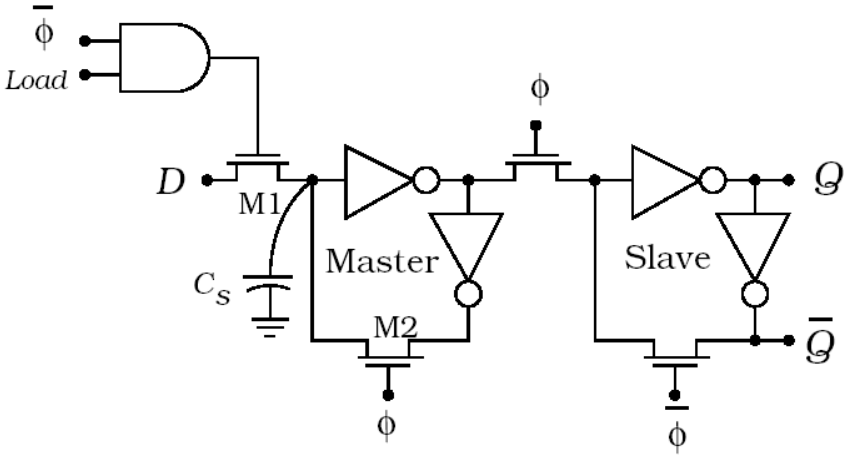
DFF modified to a TFF circuit using feedback.

Latches and Flip-Flops (10)

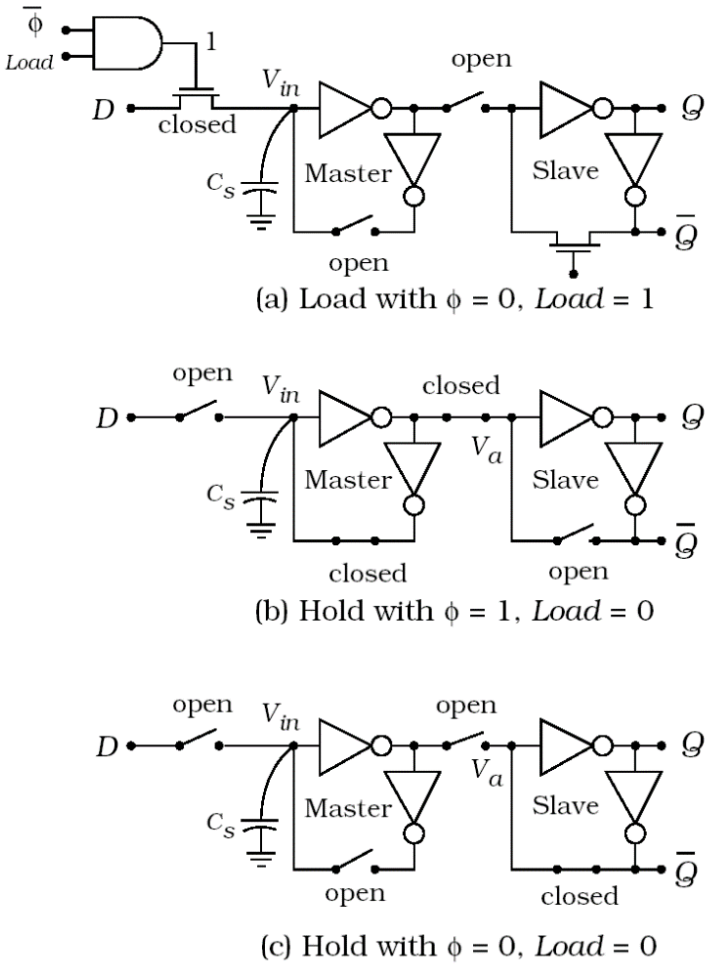


D-type flip-flop with *Load* control.

Latches and Flip-Flops (11)

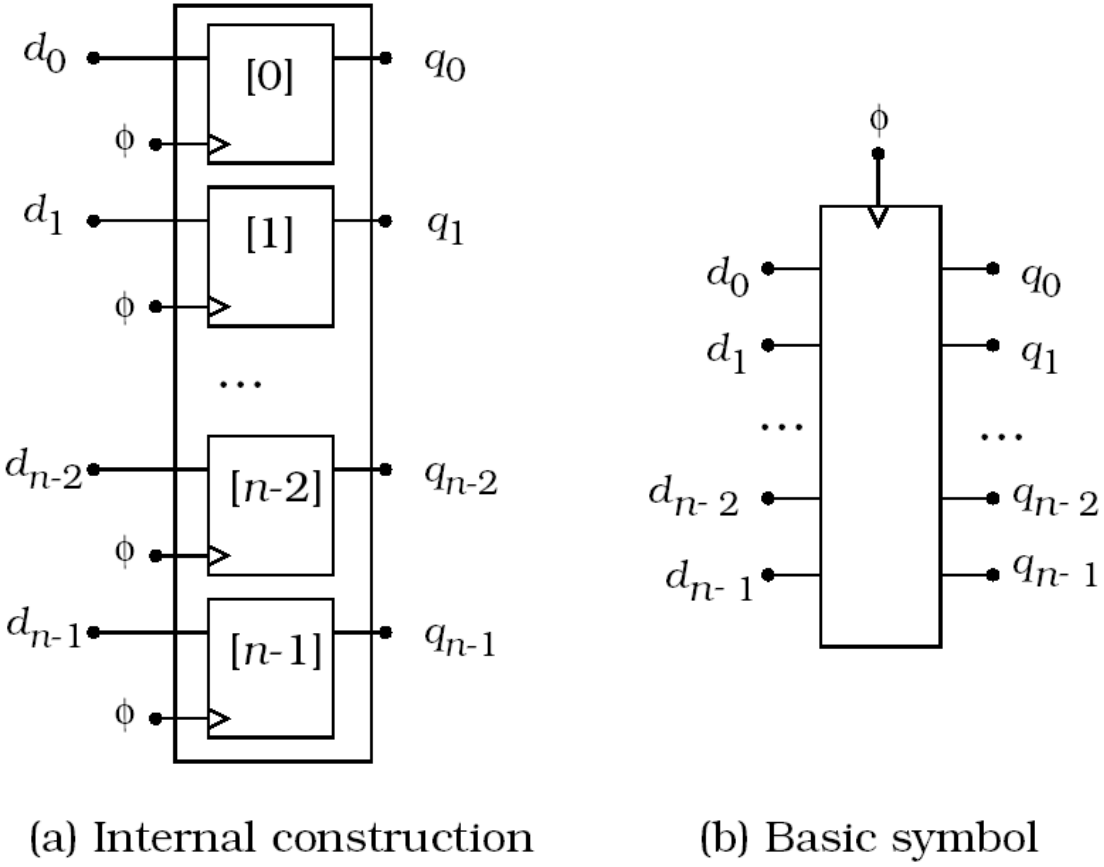


CMOS master-slave FF with Load control.



Operation of the CMOS DFF with load control.

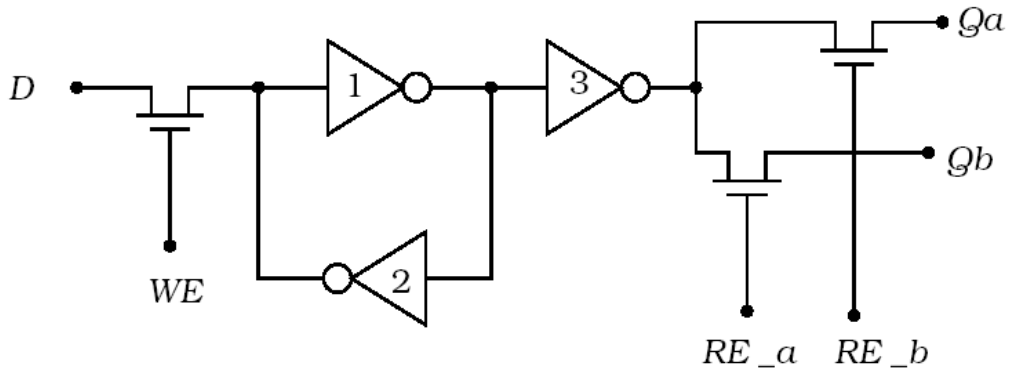
Registers



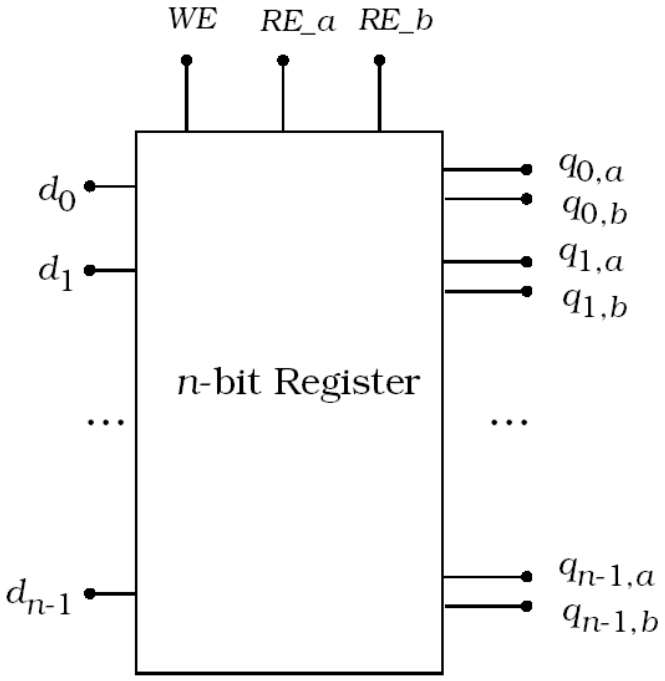
(a) Internal construction (b) Basic symbol

Construction of an *n*-bit register.

Registers (2)



One-bit static multiport register circuit.



An *n*-bit static multiport register.