ELEMENTS OF PHYSICAL DESIGN

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Outline

- Basic Concepts
- Design Rules
- Physical Design of Logic Gates
- FET Sizing and the Unit Transistor
- Cell Concepts
- Design Hierarchies

Physical Design

- What is physical design?
  - To translating logic circuits into *silicon*
  - Switch speed is critical
    - The electrical characteristics of a logic gate depend on the aspect ratios of the transistors (In Chapter 6, we will discuss it)
    - In other words, this is due to both the current flow levels and the parasitic resistance and capacitance (In Chapter 3)
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - VDD and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

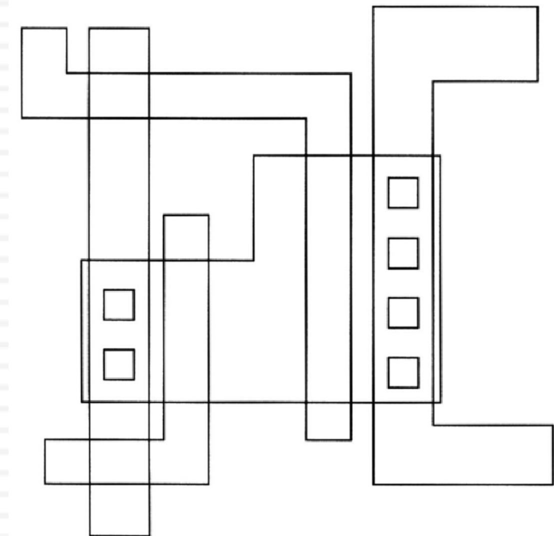
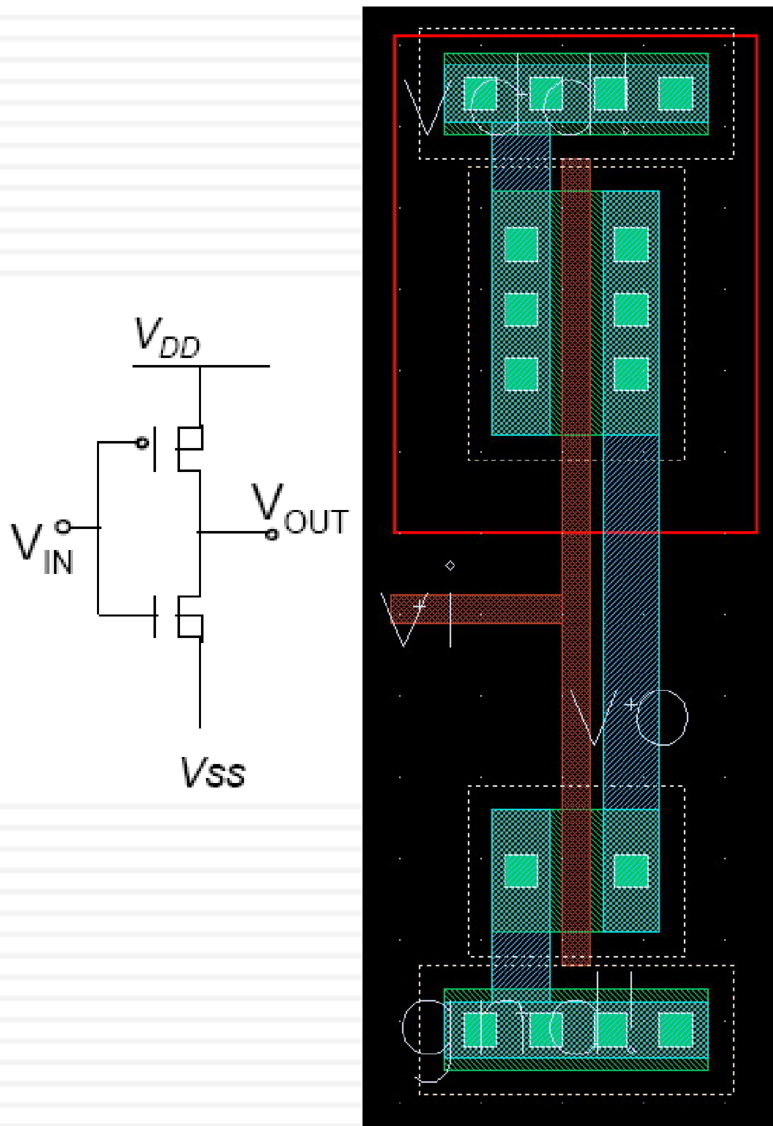
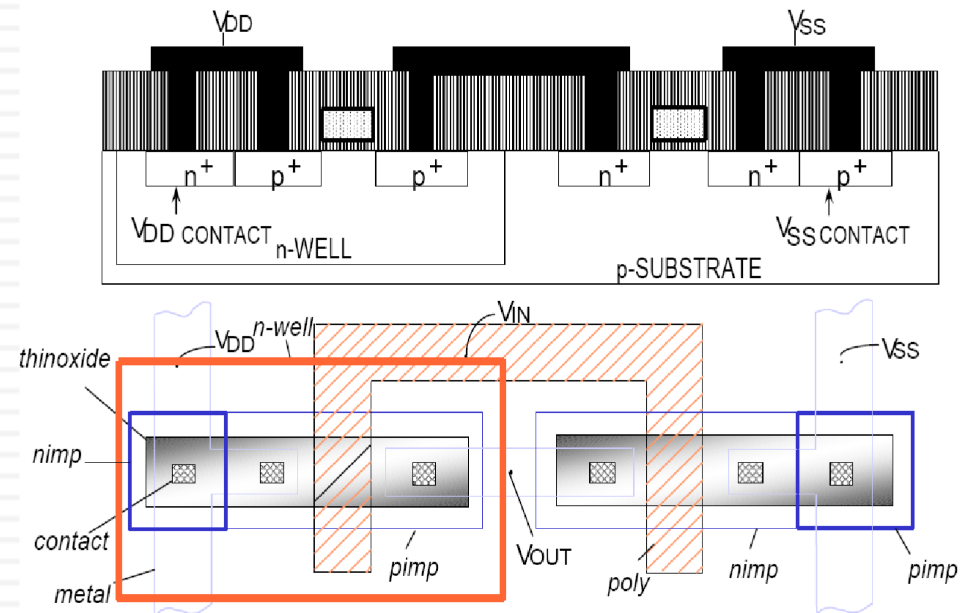


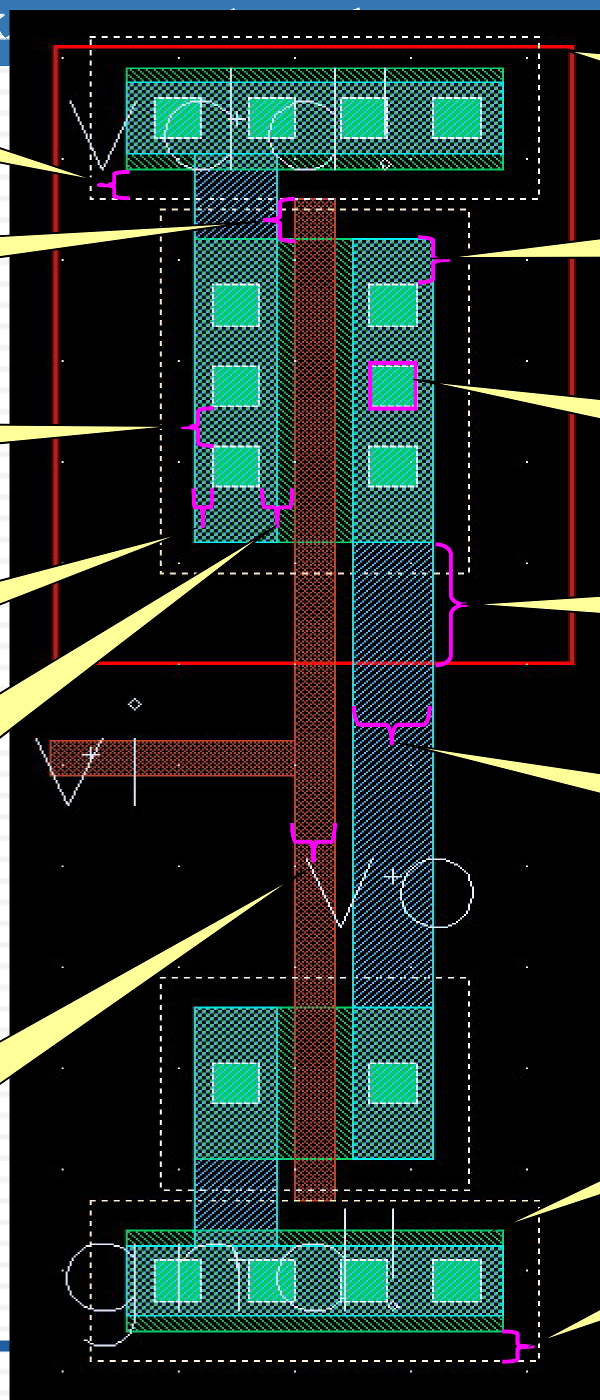
Figure 5.1 Polygons in physical design

Example: N-Well COMS Inverter





The cross-section view and layout of a CMOS(n-well) inverter



Minimum NIMP extension of N+ Diffusion 0.25 um

Minimum POLY1 extension of Diffusion 0.4 um

Minimum Contact to Contact spacing 0.4 um

Minimum Diffusion extension of Contact is 0.15 um

Minimum clearance from Contact on Diffusion region to a Poly gate 0.3 um

Minimum Poly1 width 0.35 um

Minimum N-Well width 1.7 um

Minimum Metal1 extension of Contact 0.15 um

Contact size 0.4 * 0.4 um

Minimum N-Well extension of P+ Diffusion 1.2 um

Minimum Metal1 width 0.5 um

Minimum Diffusion width 0.3 um

Minimum PIMP extension of P+ Diffusion 0.25 um

Basic Concepts

- Our study to this point shows that the topology of the transistor network establishes the logic function
- Another aspect of logic is switching speed which is crucially important to modern chip design
- The electrical characteristics of a logic gate depends on the transistor aspect ratios (W/L)
- Physical design must address both of theses areas
- We will focus on studying the basics of circuit layout in this chapter

Layout CAD Tools

- Layout Editor
  - draw multi-vertices polygons which represent physical design layers
  - Manhattan geometries, only 90° angles
  - Manhattan routing: run each interconnect layer perpendicular to each other
- Design Rules Check (DRC)
  - checks rules for each layer (size, separation, overlap)
  - must pass DRC or will fail in fabrication
- Parameter Extraction
  - create netlist of devices (tx, *R*, *C*) and connections
  - extract parasitic *R*s and *C*s, lump values at each line (R) / node (C)

Layout CAD Tools

- Layout vs. Schematic (LVS)
  - compare layout to schematic
  - check devices, connections, power routing
  - can verify device sizes also
  - ensures layout matches schematic exactly
  - passing LVS is final step in layout

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Basic Structure of nWell

nWell technology

1. Start with p-type substrate
2. nWell
3. Active
4. Poly
5. pSelect
6. nSelect
7. Active contact
8. Poly contact
9. Metal1
10. Via
11. Metal2
12. Overglass

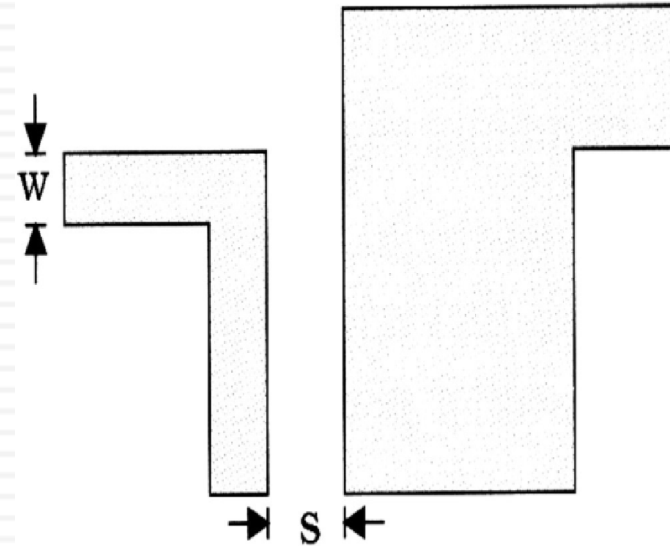


Figure 5.2 Minimum line width and space

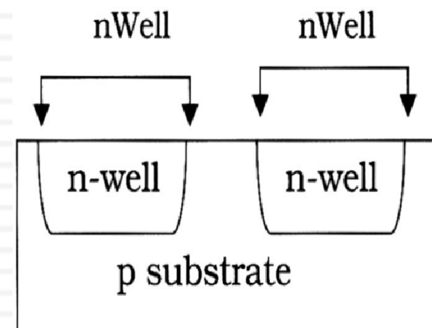
Manhattan geometries

- Where *all turns are multiples of 90°*
- If in an arbitrary manner, then must be sure what the structures are supported by the fabrication process

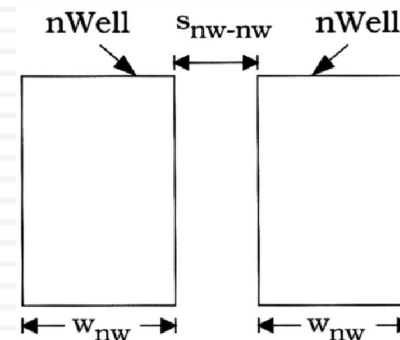
n-Wells

- An n-well is required at every location where a pFET is to be made
  - It is often possible to merge adjacent n-wells together into one
  - n-well must be connected to the power supply V_{DD} when used for pFETs

W_{nw} = minimum width of an n-well mask feature
S_{nw-nw} = minimum edge-to-edge spacing of adjacent n-wells



(a) Cross-section

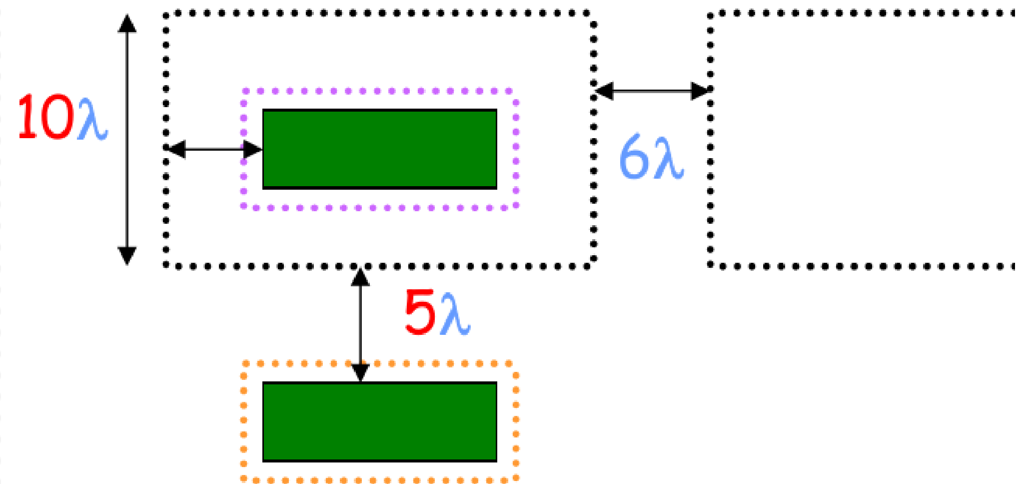


(b) Mask set

Figure 5.3 n-well structure and mask

Example

- n-well
  - required everywhere pMOS is needed
  - rules
    - minimum width
    - minimum separation to self
    - minimum separation to nMOS Active
    - minimum overlap of pMOS Active

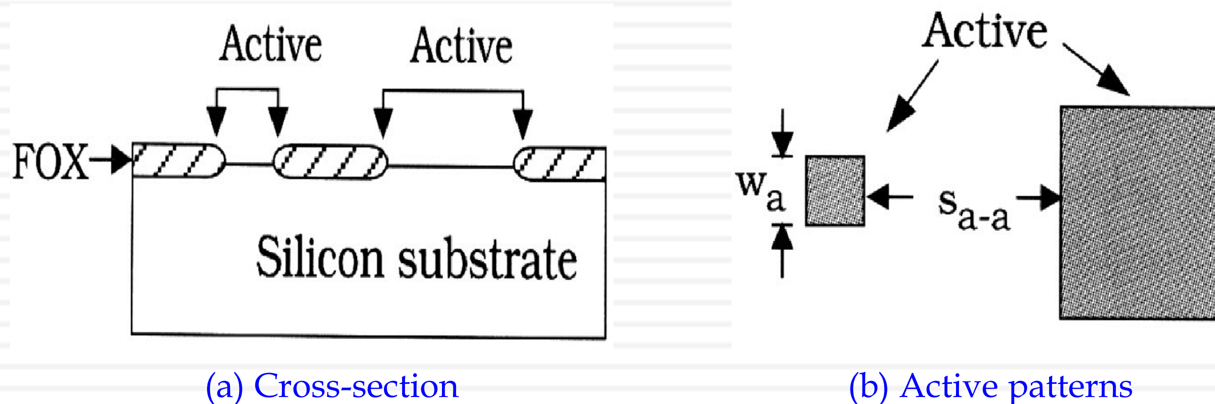


Active Areas

- Silicon devices are built on active areas of the substrate

W_a = minimum width of an Active feature
S_{a-a} = minimum edge-to-edge spacing of Active mask polygons

FOX = NOT (Active) (5.1)
FOX + Active = Surface (5.2)

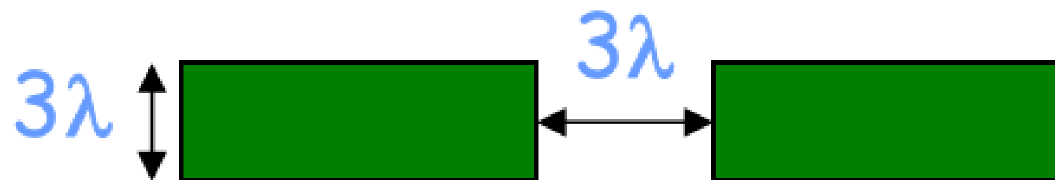


(a) Cross-section (b) Active patterns

Figure 5.4 Active area definition

Example

- Active
  - required everywhere a transistor is needed
  - any non-Active region is FOX
    - rules
      - minimum width
      - minimum separation to other Active



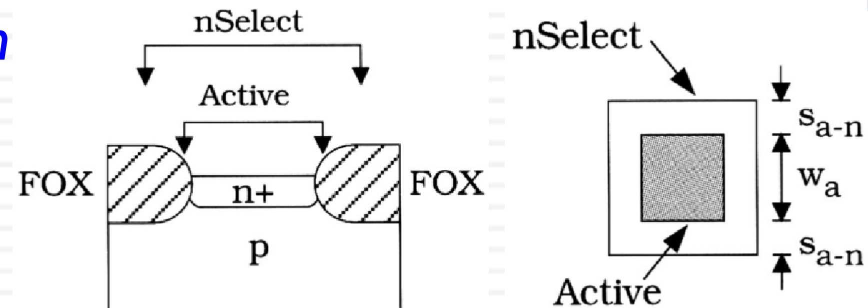
MOSIS SCMOS rules; λ=0.3μm for AMI C5N

Doped Silicon Regions

- Thermal technique called *diffusion*
  - Create n+ (ndiff, [Arsenic, As] or [Phosphorus, p]) and p+ (pdiff, [Boron, B]) regions

$$n+ = (nSelect) \cap (Active) \quad (5.3)$$

W_a = minimum width of an Active area
$S_{a\text{-}n}$ = minimum Active-to-nSelect spacing

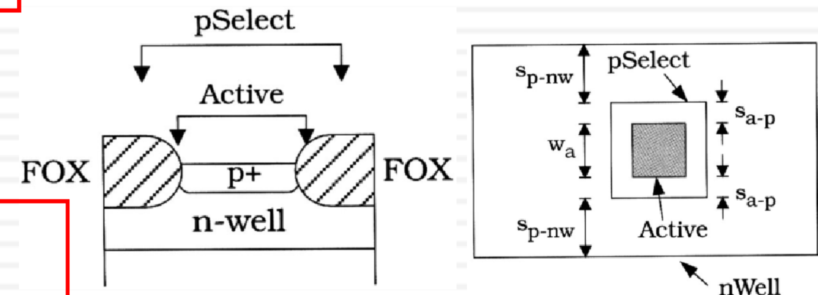


(a) Cross-section (b) Mask set

Figure 5.5 Design of a n+ regions

$$p+ = (pSelect) \cap (Active) \cap (nWell) \quad (5.4)$$

W_a = minimum width of an Active area
$S_{a\text{-}p}$ = minimum Active-to-pSelect spacing
$S_{p\text{-}nw}$ = minimum pSelect-to-nSelect spacing

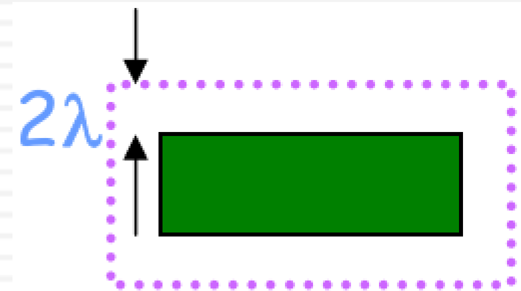


(a) Cross-section (b) Mask set

Figure 5.6 Design of a p+ regions

Example

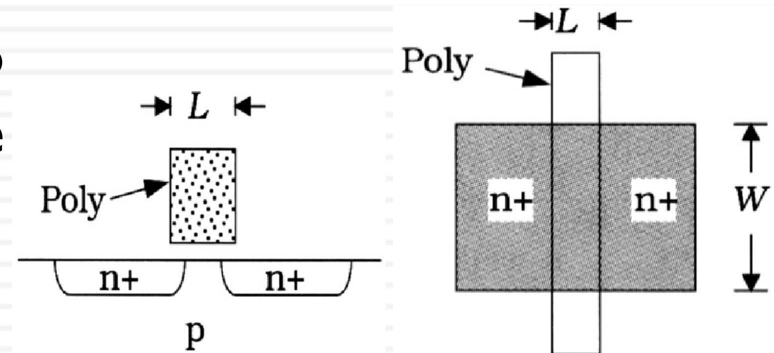
- n/p Select
  - defines regions to be doped n+ and p+
  - tx S/D = Active AND Select NOT Poly
  - tx gate = Active AND Select AND Poly
  - rules
    - minimum overlap of Active
      - same for pMOS and nMOS
    - several more complex rules available



MOSFETs (1/2)

- Physically, the poly line is deposited before the ion implant, and acts to block dopants from entering the silicon
- nFETs

W_p = minimum poly width
$S_{p\text{-}p}$ = minimum poly-to-poly spacing
$L = W_p$ = minimum width (length) of a Poly line
d_{po} = minimum extension of Poly beyond Active



(a) Cross-section (b) Layout view

Figure 5.7 nFET structure

$$nFET = (nSelect) \cap (Active) \cap (Poly) \quad (5.5)$$
$$n+ = (nSelect) \cap (Active) \cap (NOT\ [Poly]) \quad (5.6)$$

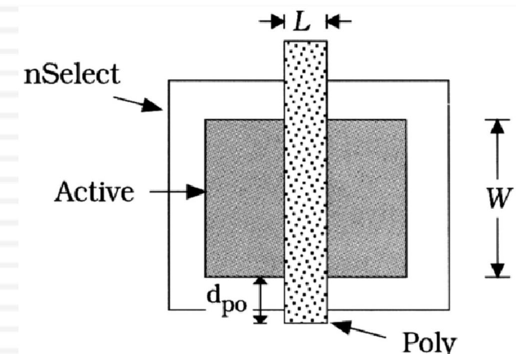


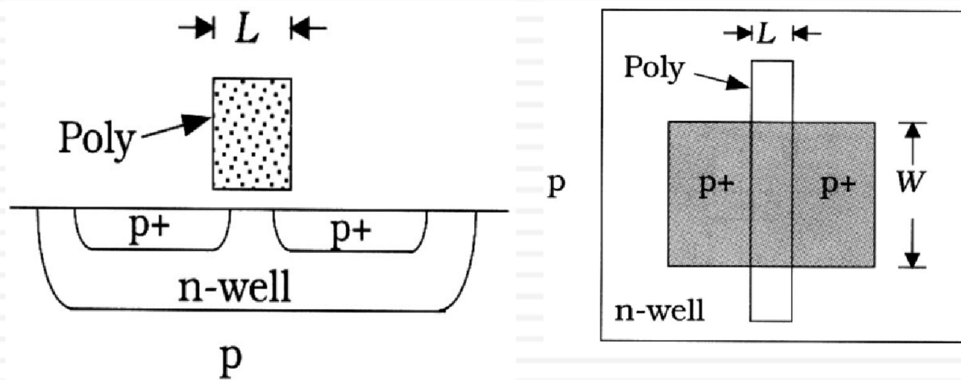
Figure 5.8 Masks for the nFET

MOSFETs (2/2)

- pFETs

pFET = (pSelect)∩(Active) ∩(Poly) ∩(nWell) (5.7)

p+ = (pSelect)∩(Active)∩(nWell)∩(NOT [Poly]) (5.8)



(a) Cross-section (b) Layout view

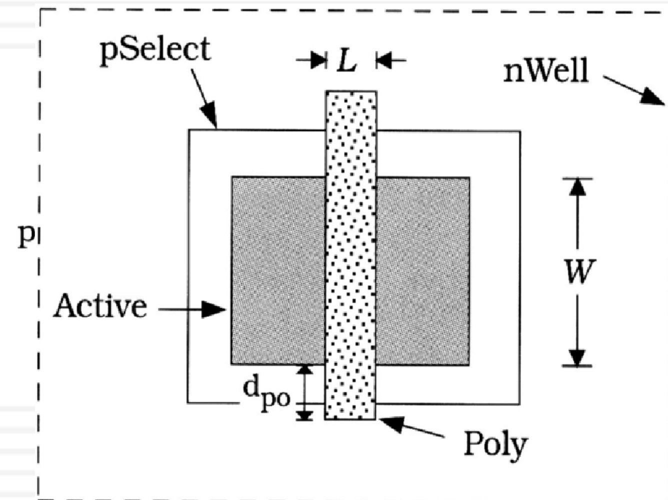
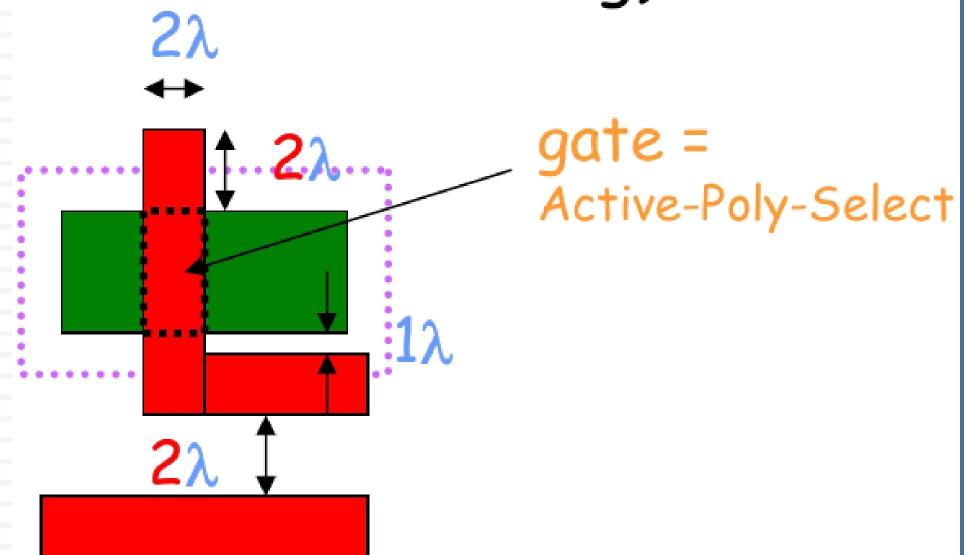


Figure 5.9 pFET structure

Figure 5.10 Masks for the pFET

Example

- Poly
  - high resistance conductor (can be used for short routing)
  - primarily used for tx gates
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of gate
    - minimum space to Active



Drawn and Effective in MOSFETs

- Draw and Effective Values in MOSFETs
  - The critical dimensions of a MOSFET are the channel length *L* and the channel width *W*
- The physical length is small than L due to lateral doping during the implant annealing step
  - L_{eff}: electrical or effective channel length
  - L_o: overlap distance on both sides

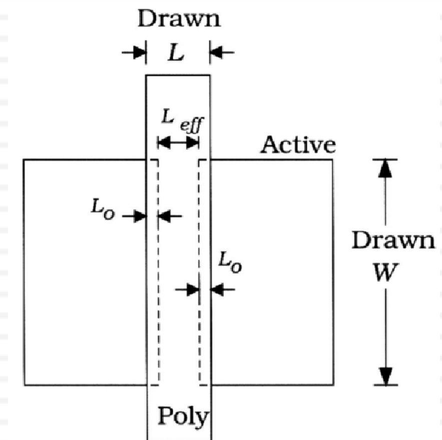
$$L_{eff} = L - 2L_o \quad (5.9)$$

$$L_{eff} = L - \Delta L \quad (5.10)$$

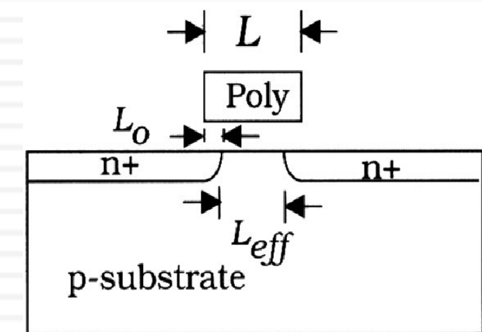
- The channel width is also small than the drawn value due to reduction of active area by the field oxide growth

$$W_{eff} = W - \Delta W \quad (5.11)$$

$$\frac{W_{eff}}{L_{eff}} \quad (5.12)$$



(a) Drawn Layout



(b) Finished view

Figure 5.11 Drawn and effective dimensions of a MOSFET

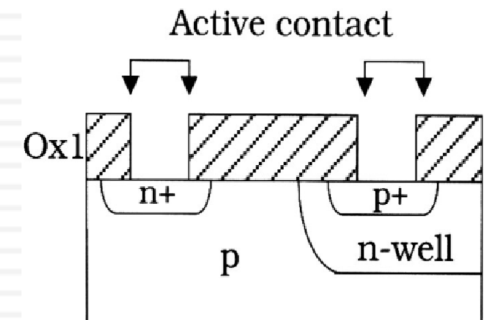
Active Contacts

- An *active contact* is a cut in the Ox1 that allows the first layer of metal1 to contact an active n+ or p+ region

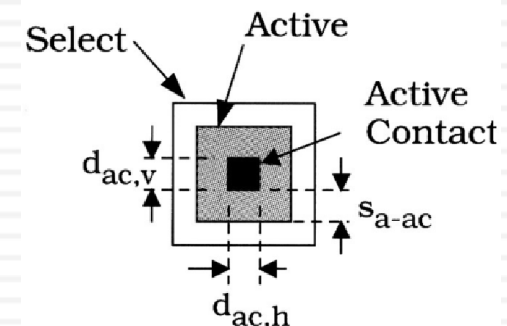
$S_{a\text{-}ac}$ = minimum spacing between Active and Active Contact
$d_{ac,\,v}$ = vertical size of the contact
$d_{ac,\,h}$ = horizontal size of the contact

- A square contact is obtained if, *however*, it is not uncommon to have aspect rations other than 1:1

$$d_{ac,\,v} = d_{ac,\,h} = d_{ac} \qquad (5.13)$$



(a) Cross-section

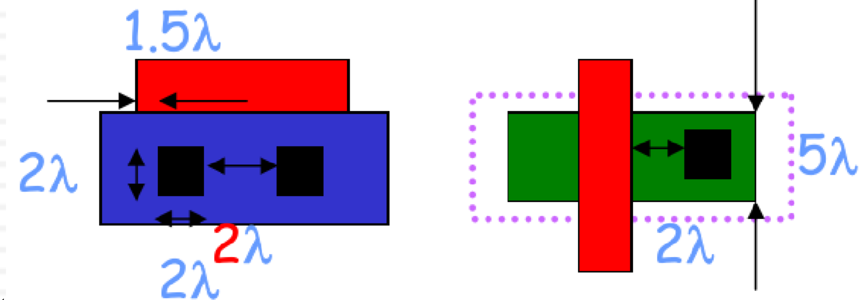


(b) General mask set

Figure 5.12 Active contact formation

Design Rules: 3

- Contacts
  - Contacts to Metal1, from Active or Poly
    - use same layer and rules for both
  - must be SQUARE and MINIMUM SIZED
  - rules
    - exact size
    - minimum overlap by Active/Poly
    - minimum space to Contact
    - minimum space to gate



Metal1 (1/3)

- Metal1 is used as interconnect for signals and power supply distribution

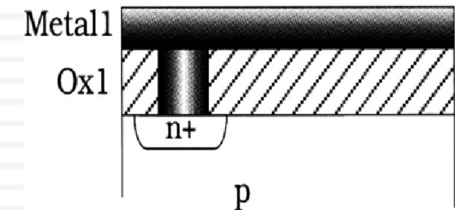
W_{m1} = minimum width of a Metal1 line
$S_{m1\text{-}ac}$ = minimum spacing from Metal1 to Active Contact

- Every contact is characterized by a resistance

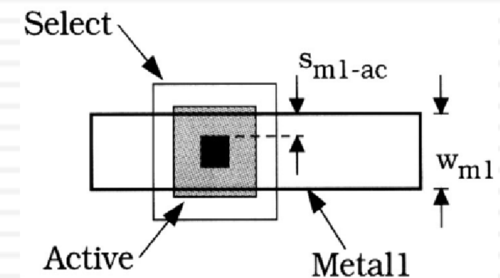
R_c = contact resistance Ω

- Since the contacts are all in parallel, the effective resistance of the Metal1-Active connection with N contacts is reduced to

$$R_{c,\,eff} = \frac{1}{N} R_c \qquad (5.14)$$



(a) Cross-section



(b) General mask set

Figure 5.13 Metal1 line with Active Contact

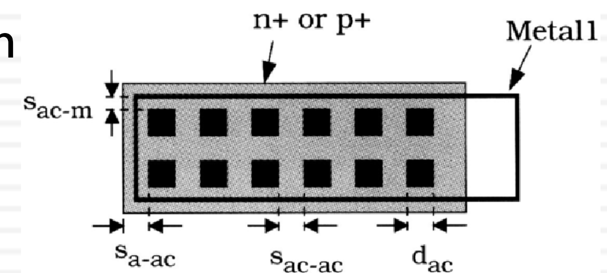
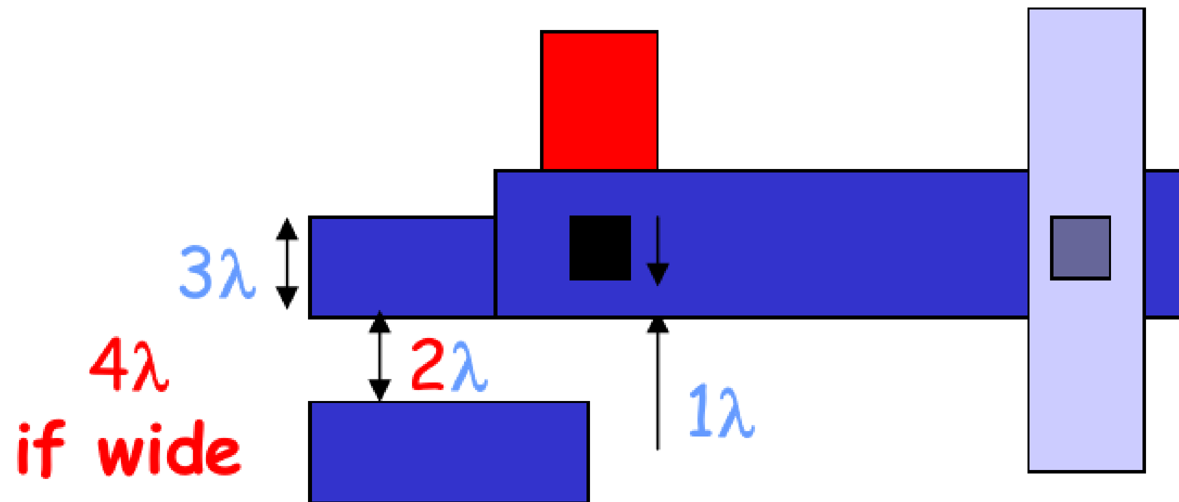


Figure 5.14 Multiple contacts

Example

- Metal I
  - low resistance conductor used for routing
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of Contact



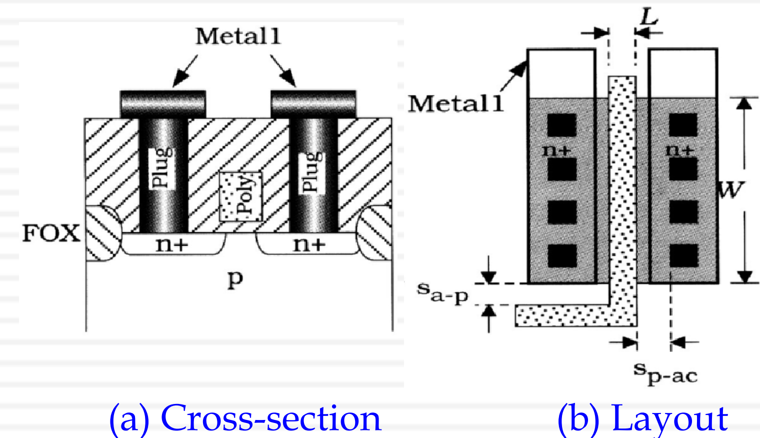
Metal1 (2/3)

- Metal1 allows access to the active regions of MOSFETs using the Active Contact oxide cut as Figure 5.15

$S_{p\text{-}ac}$ = minimum spacing from Poly to Active Contact
$S_{a\text{-}p}$ = minimum spacing from Active to Poly

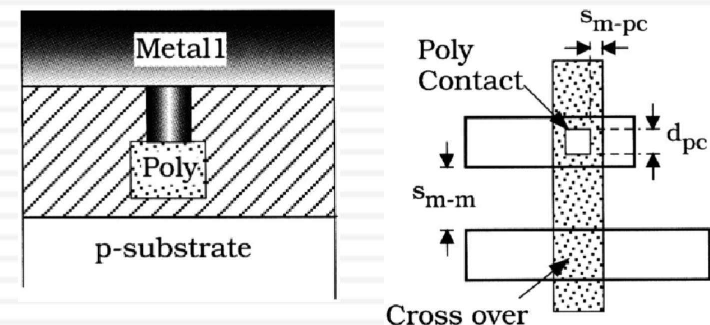
- A Poly Contact mask is used to allow electrical connections between Metal1 and the polysilicon gate as Figure 5.16

$S_{p\text{-}p}$ = minimum Poly-to-Poly spacing



(a) Cross-section (b) Layout

Figure 5.15 Drain and source FET terminals using Metal1

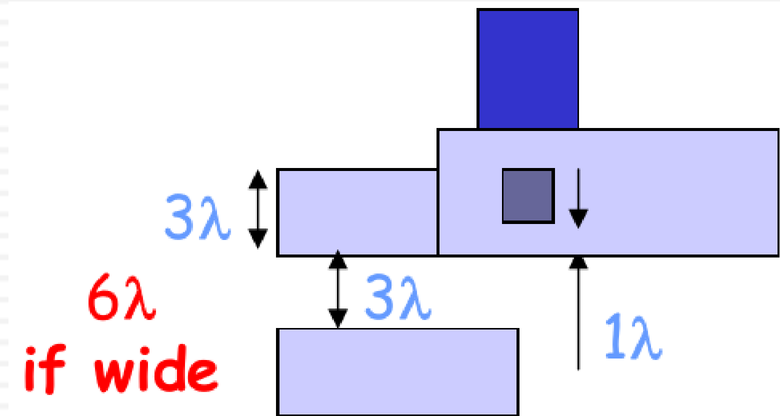


(a) Cross-section (b) Layout

Figure 5.16 Poly Contact

Example

- Vias
  - Connects Metal1 to Metal2
  - must be SQUARE and MINIMUM SIZED
  - rules
    - exact size
    - space to self
    - minimum overlap by Metal1/Metal2
    - minimum space to Contact
    - minimum space to Poly/Active edge



- Metal2
  - low resistance conductor used for routing
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of Via

Metal1 (3/3)

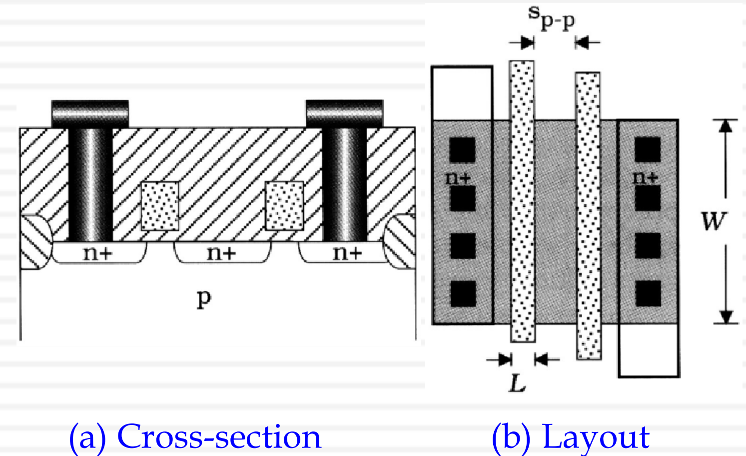
- Example: A pair of series-connected FETs sharing the central n+ region as Figure 5.17

  S_{p-p} = minimum Poly-to-Poly spacing

- Example: Parallel-connected FETs as Figure 5.18

  $S_{g-g} = d_{ac} + 2\,S_{p-ac}$ (distance between the two gates)

- Example: allow for the size of the contact itself, plus two units of poly-active spacing as Figure 5.19
  - Enforced twice S_{p-a}



(a) Cross-section (b) Layout

Figure 5.17 Series-connected FETs

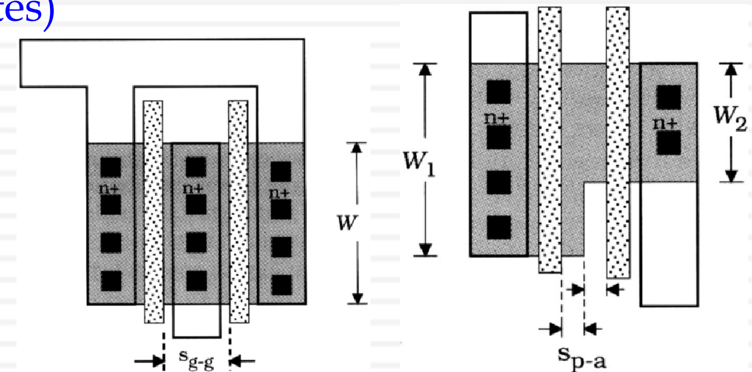


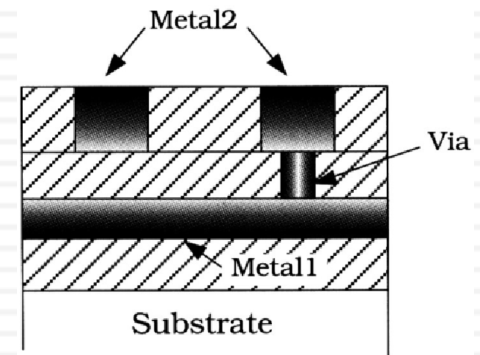
Figure 5.18 Parallel-connected nFETs

Figure 5.19 Different channel widths using the same active region

Vias and Higher Level Metals

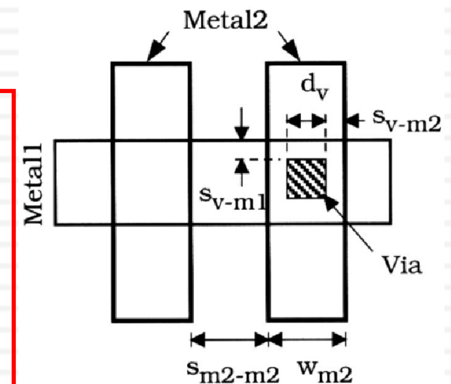
- Model CMOS processes add several additional layers of metal that can be used for signal and power distribution

Metal1 → Metal2 → Metal3 → Metal4



(a) Cross-section

d_v = dimension of a Via (may be different for vertical direction)
w_{m2} = minimum width of Metal2 feature
$s_{m2\text{-}m2}$ = minimum spacing between adjacent Metal2 features
$s_{v\text{-}m1}$ = minimum spacing between Via and Metal1 edges
$S_{v\text{-}m2}$ = minimum spacing between Via and Metal2 edges



(b) Layout

Figure 5.20 Metal1-Metal2 connection using a Via mask

Latch-up

- *Latch-up:* is a condition that can occur in a circuit fabricated in a bulk CMOS technology
  - The key to understanding latch-up is noting that the bulk technology gives a **4-layers pnpn** structure between the power supply VDD and ground
  - If VDD reaches the **breakover voltage** V_{BO}, the blocking is overwhelmed by internal electric fields

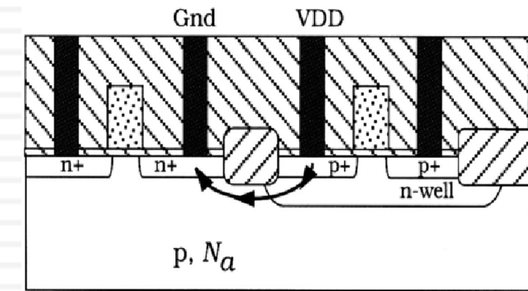
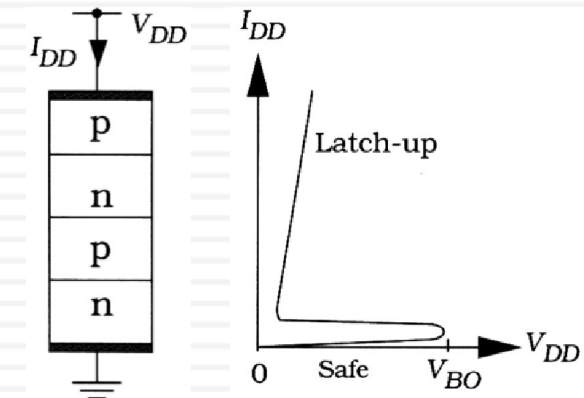


Figure 5.21 Latch-up current flow path

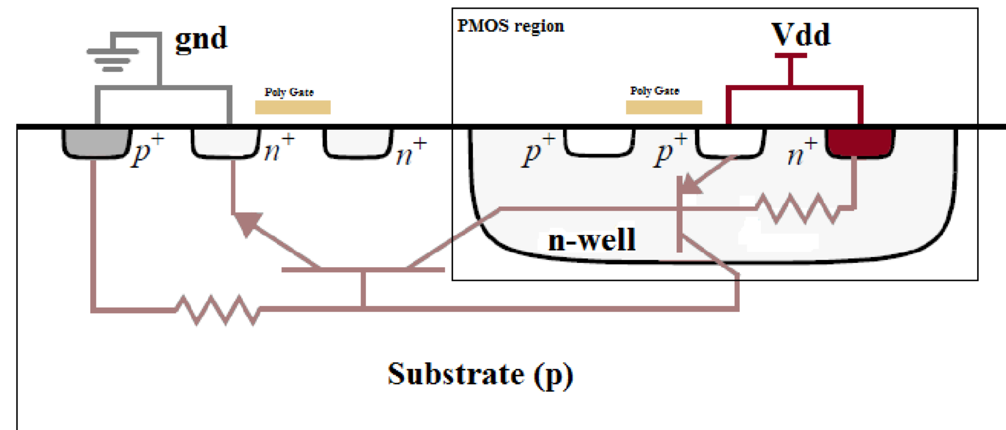


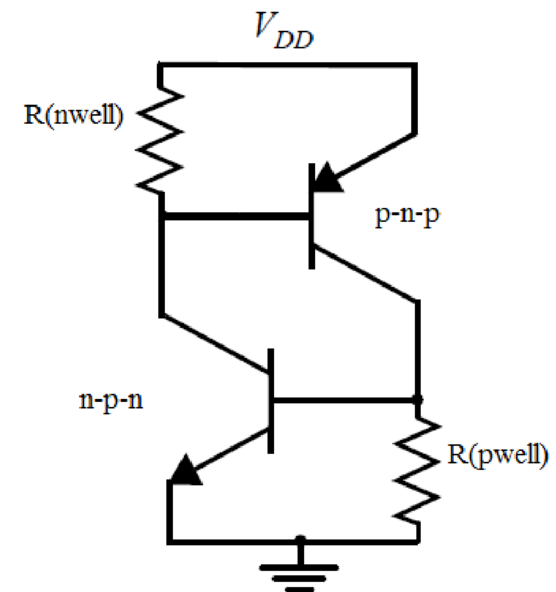
(a) Structure (b) Behavior

Figure 5.22 Characteristics of 4-layer pnpn device

Equivalent circuit of CMOS latchup

- When one of the two bipolar transistors gets forward biased (due to current flowing through the well, or substrate), it feeds the base of the other transistor
- This positive feedback increases the current until the circuit fails or burns out





Latch-up Prevention

- Latch-up avoiding method
  - to steer the current out of the "bad" path
    - Include and n-Well contact every time a pFET is connected to the power supply VDD, and
    - Include a p-substrate contact every time and nFET is connected to a ground rail
  - Silicon-on-insulator, SOI
  - Twintub: using two separate wells for FETs, an n-well for pFETs and a p-well for nFETs

Layout Editors

- n+ is formed whenever Active is surrounded by nSelect; this is also called ndiff.
- p+ is formed whenever Active is surrounded by pSelect; this is also called pdiff.
- A nFET is formed whenever Poly cuts an n+ region into two separate segments.
- A pFET is formed whenever Poly cuts an p+ region into two separate segments.
- No electrical current path exists between conducting layer (n+, p+, Poly, Metal, etc.) unless a contact cut (Active Contact, Poly Contact, or Via) is provided.

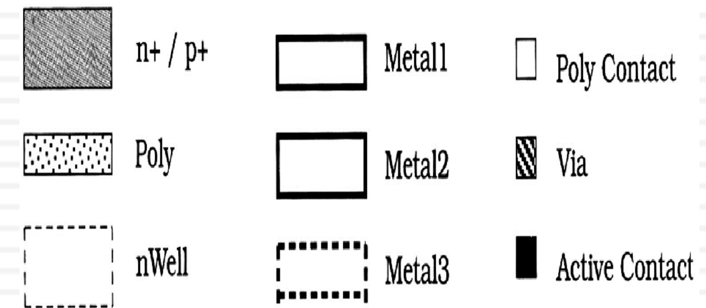
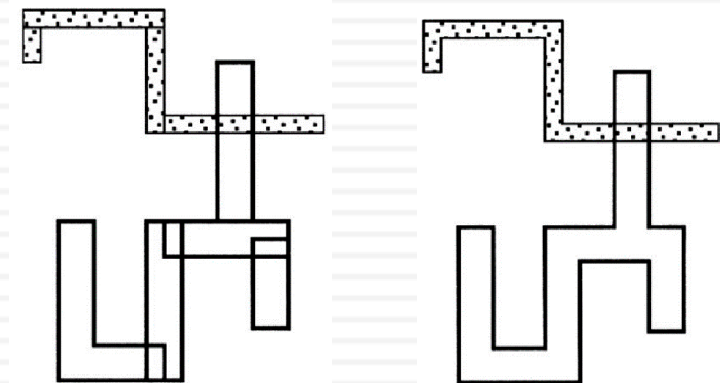


Figure 5.24 Layer key for layout drawings in this book



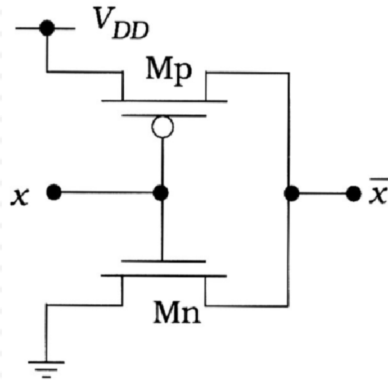
(a) Structure (b) Behavior

Figure 5.25 Drawing complex polygons using rectangles

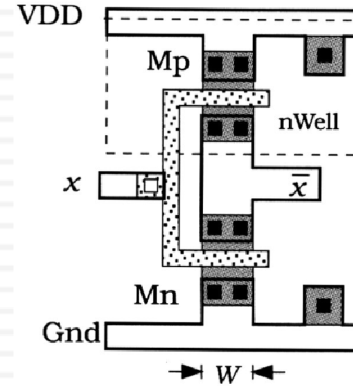
Outline

- Basic Concepts
- Design Rules
- Physical Design of Logic Gates
- FET Sizing and the Unit Transistor
- Cell Concepts
- Design Hierarchies

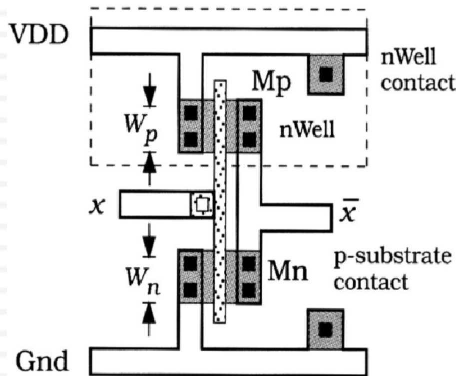
The Not Cell



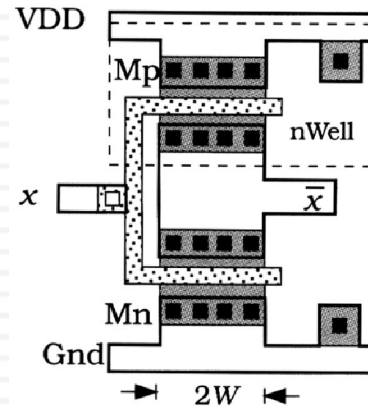
(a) Schematic



(a) Basic cell



(b) Cell layout

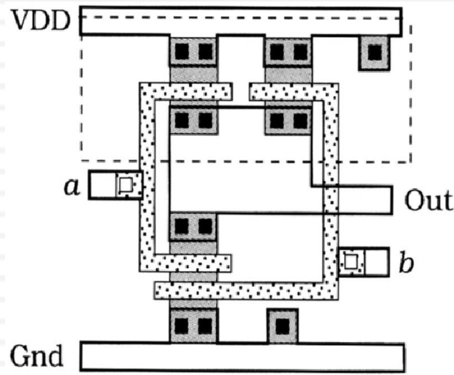


(b) 2X cell

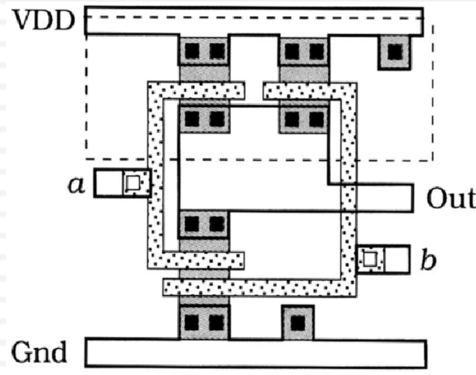
Figure 5.42 NOT gate width horizontal FETs

Figure 5.43 Not layout using vertical FETs

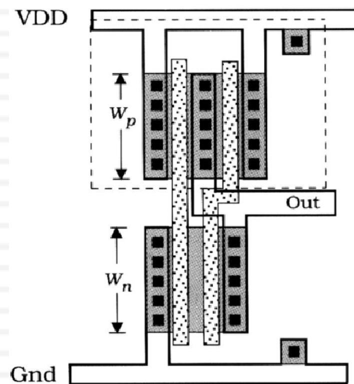
NAND2 and NOR2



(a) NAND2

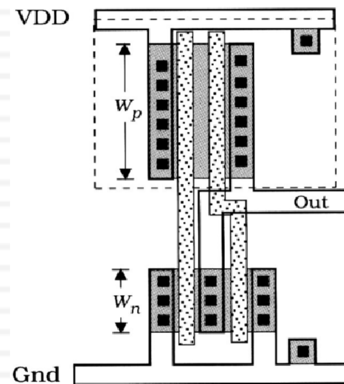


(a) NAND2



(b) NOR2

Figure 5.45 NAND2 and NOR2 layouts using vertical FETS



(b) NOR2

Figure 5.46 Alternate NAND2 and NOR2 cells

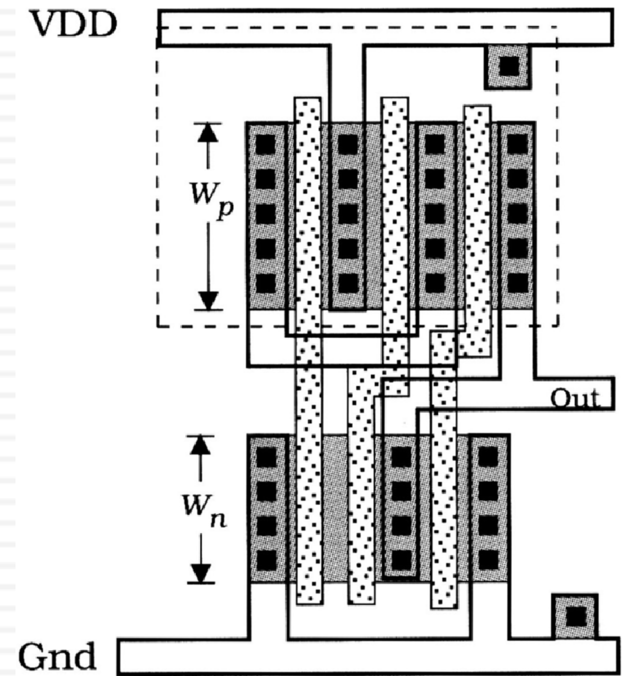
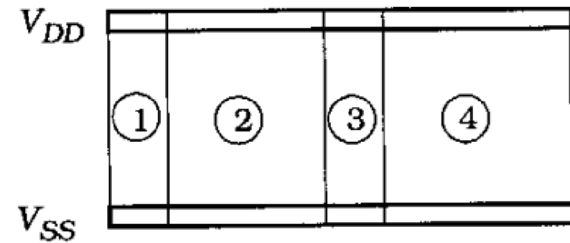


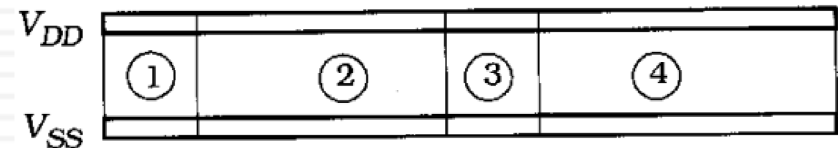
Figure 5.47 Complex logic gate example

Transistor Orientation

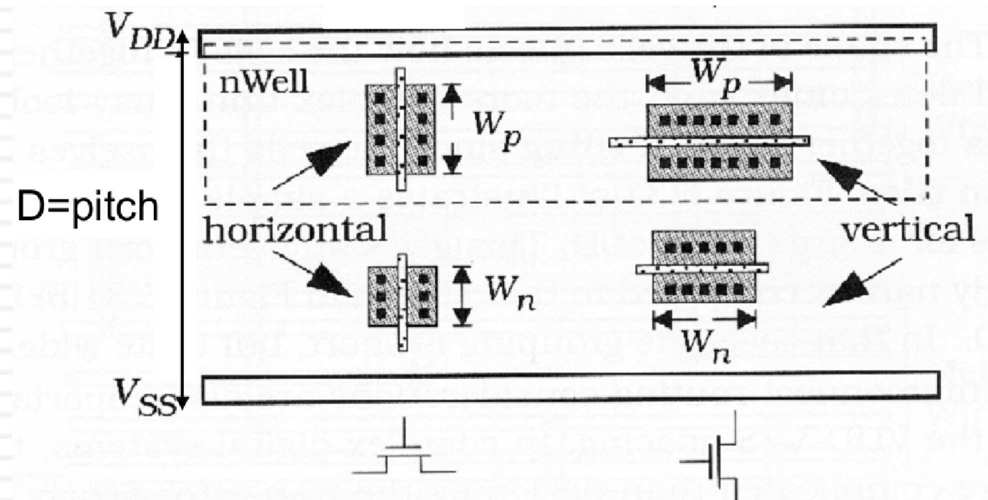
- Horizontal Tx (W run vertically)
  - can increase tx width with fixed pitch (space between power rails)
  - cells short & wide
- Vertical Tx (W runs horizontally)
  - pitch sets max tx width
  - cells taller & narrow



(a) Larger D

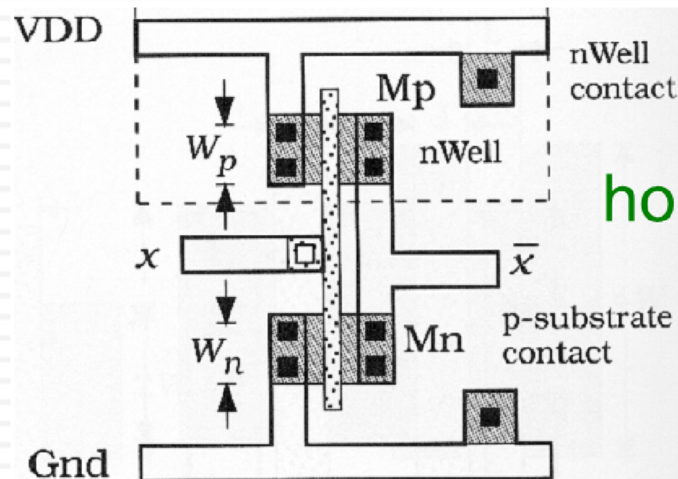


(b) Smaller D

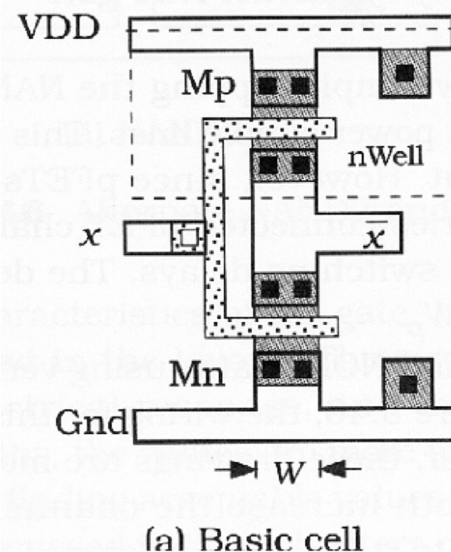


Inverter Layout Options

- Layout with Horizontal Tx
  - pitch sets max txsize
- Layout with Vertical Tx
  - allows tx size scaling without changing pitch
- Vertical Tx with 2x scaling

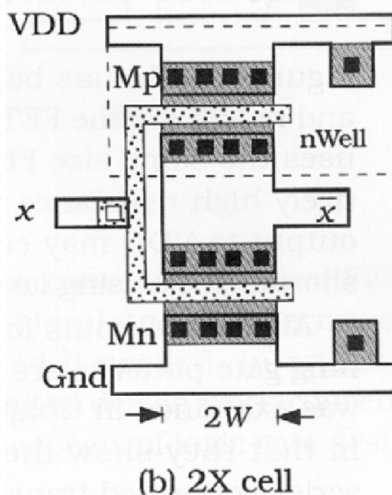


horizontal



(a) Basic cell

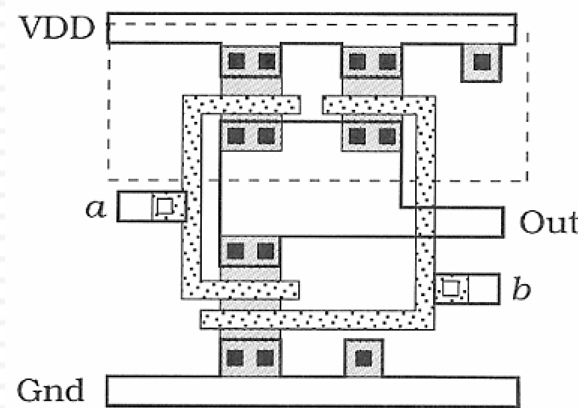
vertical



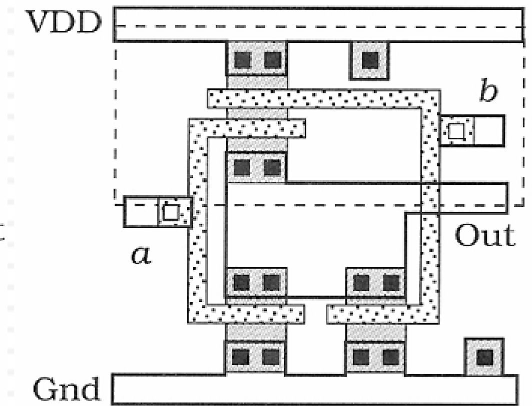
(b) 2X cell

NAND/NOR Layout Alternatives

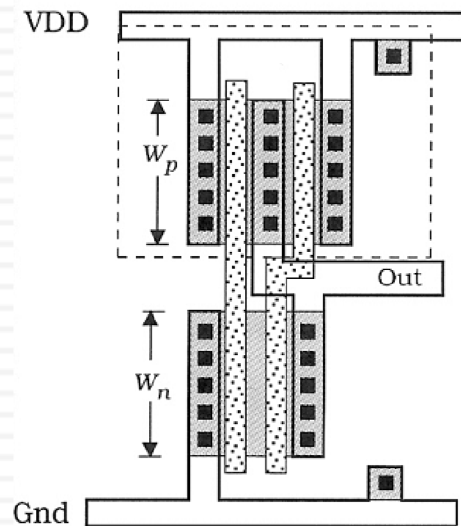
- vertical transistors
  - for smaller pitch (height) and wider cell
- large horizontal transistors
  - for larger pitch (height) and narrower cell



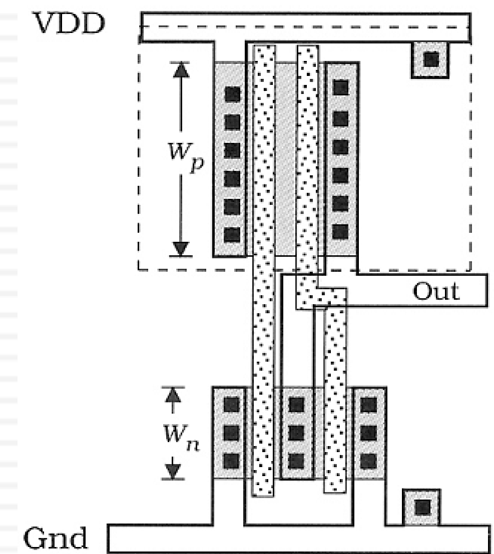
(a) NAND2 gate



(b) NOR2 gate



(a) NAND2



(b) NOR2

Outline

- Basic Concepts
- Design Rules
- Physical Design of Logic Gates
- FET Sizing and the Unit Transistor
- Cell Concepts
- Design Hierarchies

FET Sizing

- FET are specified by the aspect ratio (*W*/*L*)
  - Combine with the processing parameters to give the electrical characteristic of the transistor
  - Given the gate area by $A_G = LW$

$$C_G = C_{ox}WL \qquad (5.19)$$

  - Since
$$I_D \approx I_S$$
$$R_{chan} = R_{s,c}\left(\frac{L}{W}\right) \Rightarrow R_{chan} \propto \frac{1}{W} \qquad (5.21, 5.22)$$
$$\mu_n > \mu_p$$
  - Since
$$r = \frac{\mu_n}{\mu_p} \Rightarrow \frac{R_p}{R_n} = r \qquad (5.24, 5.25) \qquad (r = 2 \sim 3)$$

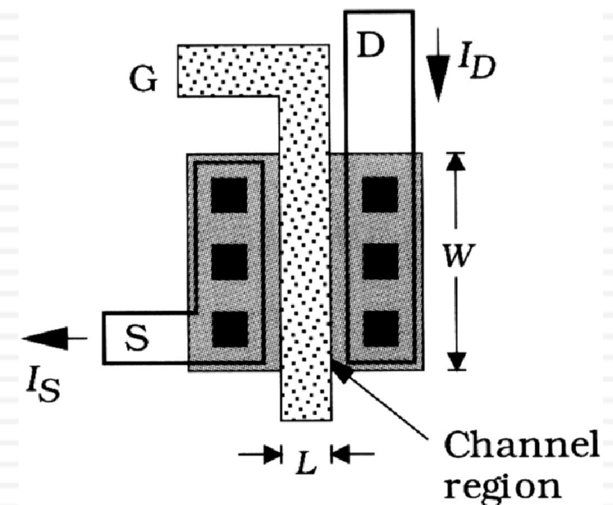


Figure 5.36 Basic geometry of a FET

$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n \qquad (5.26)$$

pFETs don't conduct as well as nFETs

$$C_{Gp} = rC_{Gn} \qquad (5.27)$$

(Since C is proportional to *W*)

Unit Transistors

- Unit transistor is the minimum-size MOSFET

$$\left(\frac{W}{L}\right)_{min} = \frac{w_a}{w_b} \quad (5.30) \quad \text{(the aspect ratio)}$$

$$C_G = C_{ox} w_a w_p \quad (5.31) \quad \text{(gate capacitance)}$$

d_c = dimension of the contact
$s_{a\text{-}ac}$ = spacing between Active and Active Contact

» As Figure 5.38, the minimum width is now

$$W = d_c + 2s_{a\text{-}ac} \quad (5.32)$$

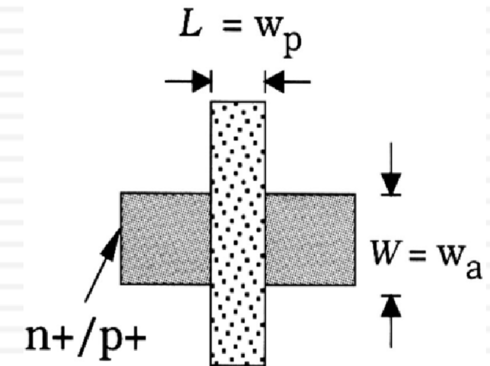
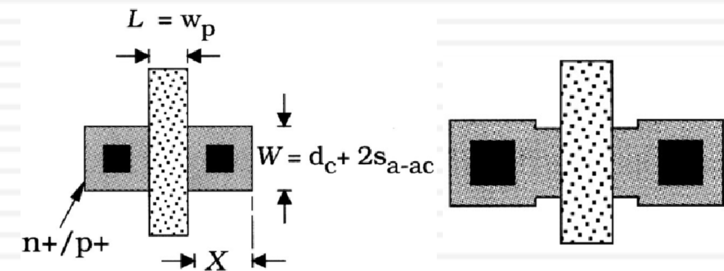


Figure 5.37 Geometry of a minimum-size FET



(a) Active contact (b) Small W_a

Figure 5.38 Minimum-size FETs with Active Contact features

Scaling Technology

- Once a unit FET has been selected, it's useful to allow it to be scaled in size
  - Reference 1X → 2X → 4X
  - However, Altering the size of the transistor changes its resistance and capacitance
- Denote R_{1X} and C_{1X} be the R and C of the 1X device

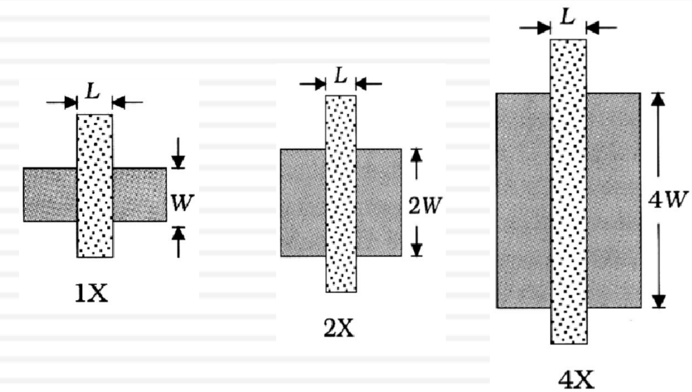


Figure 5.39 Scaling of the unit transistor

$$W_{SX} = SW_{1X}$$ (5.33) (S: Scaling factor)

$$W_{4X} = 4W_{1X}$$ (5.34) (S = 4)

$$R_{SX} = \frac{R_{1X}}{S} \quad C_{SX} = SC_{1X}$$ (5.35) (decided by FET size)

$$R_{2X} = \frac{R_{1X}}{2} \quad C_{2X} = 2C_{1X}$$ (5.36) (S = 2)

$$2(R_{1X}/2) = R_{1X}$$ (5.37) (Figure 5.40)

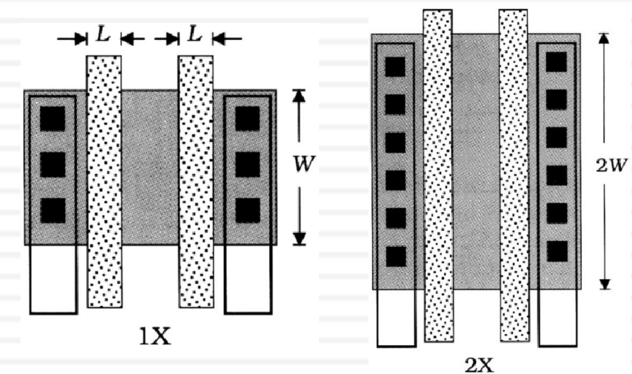


Figure 5.40 Scaling of series-connected FET chain

Gate Design for Transient Performance

$$\beta = k'\left(\frac{W}{L}\right)$$ (Inverter reference starting) $$\frac{1}{\beta_n(V_{DD}-V_{Tn})} = \frac{2}{\beta_N(V_{DD}-V_{Tn})}$$

$$R_p = \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)}, \quad R_n = \frac{1}{\beta_n(V_{DD}-V_{Tn})} \qquad \beta_N = 2\beta_n$$

$$\beta_n = \beta_p \qquad \left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n$$

$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n \qquad \beta_N = \beta_n$$ (NOR2 vs Inverter)

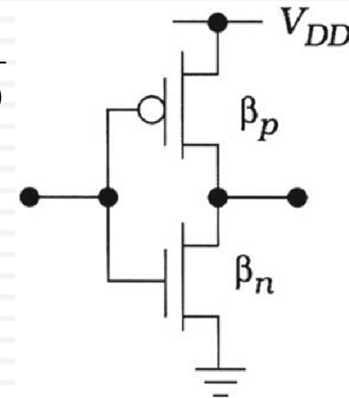
$$\text{where } r = \frac{k_n'}{k_p'} \qquad \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)} = \frac{2}{\beta_P(V_{DD}-|V_{Tp}|)}$$

$$\beta_P = \beta_p$$ (NAND2 vs Inverter) $$\beta_P = 2\beta_p$$

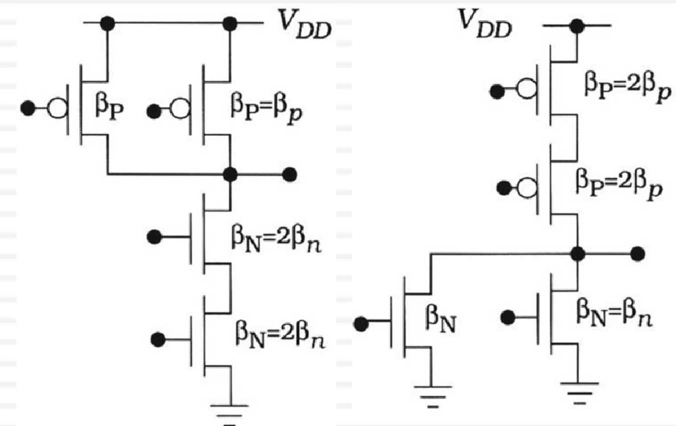
$$R = R_N + R_N \qquad \left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_p$$

$$\text{where } R_N = \frac{1}{\beta_N(V_{DD}-V_{Tn})}$$

$$R = R_n = 2R_N$$



(a) Inverter



(b) NAND2 (c) NOR2

Figure 7.34 Relative FET sizing

Gate Design for Transient Performance (2)

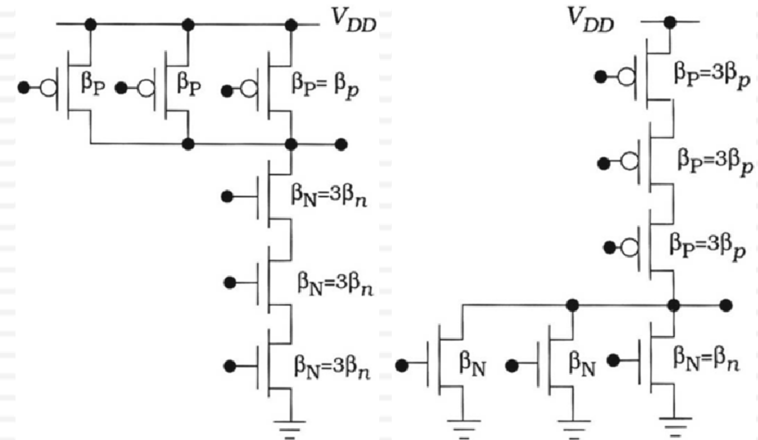
- Extend to large chains as Figure 7.35

$$\beta_N = 3\beta_n,\ \beta_P = \beta_p \quad (7.177)$$

$$\left(\frac{W}{L}\right)_N = 3\left(\frac{W}{L}\right)_n,\ \left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_p \quad (7.178)$$

$$\beta_N = \beta_n,\ \beta_P = 3\beta_p \quad (7.179)$$

$$\left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_n,\ \left(\frac{W}{L}\right)_P = 3\left(\frac{W}{L}\right)_p \quad (7.180)$$



(a) NAND3 (b) NOR3

Figure 7.35 Sizing for 3-input gates

- Example

$$f = \overline{(a \cdot b + c \cdot d) \cdot x} \quad (7.181)$$

$$\beta_N = 3\beta_n = \beta_{N1} \quad (7.182)$$

$$\beta_P = 2\beta_p \quad (7.183)$$

$$\beta_{P1} = \beta_p \quad (7.184)$$

$$\beta_{P1} = \beta_P = 2\beta_P \quad (7.185)$$

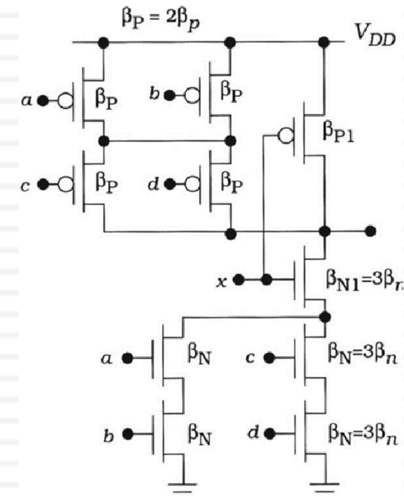


Figure 7.36 Sizing of a complex logic gate

Outline

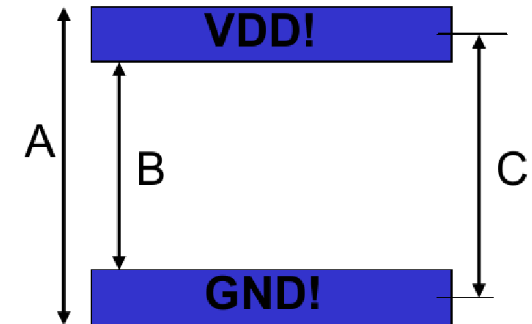
- Basic Concepts
- Design Rules
- Physical Design of Logic Gates
- FET Sizing and the Unit Transistor
- Cell Concepts
- Design Hierarchies

The Cell Concept

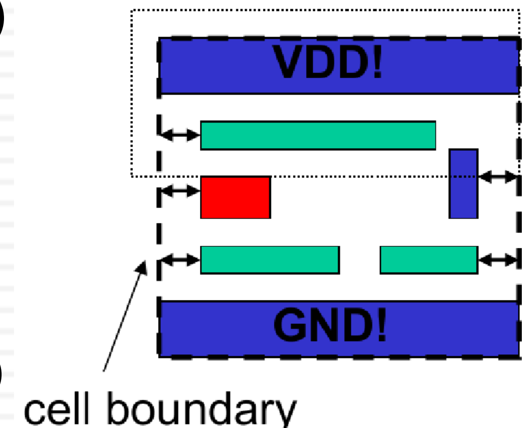
- Each physical design file is called a "cell"
- "Primitive" cells, polygon-level
  - create "cell library" of basic functions
- Expanding library with more complex cells
  - primitive library cells added as to higher level cells to create more complex logic functions
  - the instantiated (added) cell is called an "instance"

Layout Cell Definitions

- Cell Pitch = Height of standard cells
  - measured between VDD & GND rails
    - A: top of VDD to bottom of GND (we will use this)
    - B: interior size, without power rails
    - C: middle of GND to middle of VDD



- Cell Boundary
  - max extension of any layer (except nwell)
    - set boundary so that cells can be placed side-by-side without any rule violations
    - extend power rails 1.5λ(or 2λto be safe) beyond any active/poly/metal layers
    - extend n-well to cell boundary (or beyond) to avoid breaks in n-well



Cell Layout Guidelines

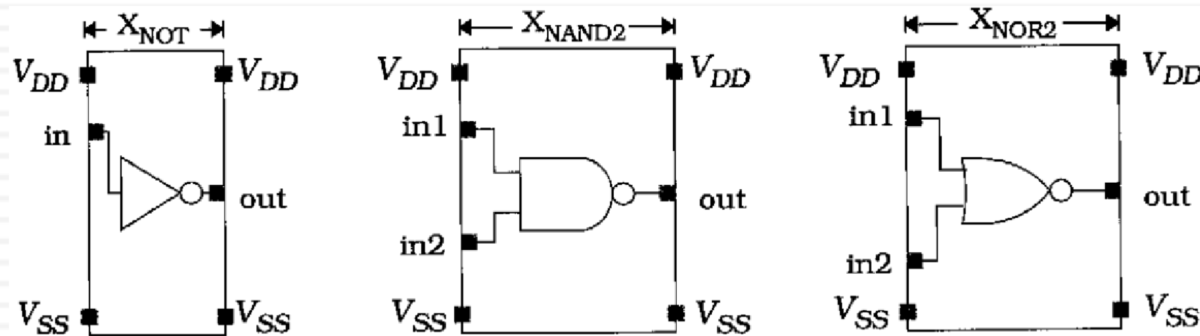
- Internal Routing
  - use lowest routing layer possible, typically poly and metal1
  - keep all possible routing inside power rails
  - keep interconnects as short as possible
- Bulk (substrate/well) Contacts
  - must have many contacts to p-substrate and n-well (at least 1 for each connection to power/ground rails)
  - consider how signals will be routed in/out of the cells (don't block access to I/O signals with substrate/well contacts)

Cell Layout Guidelines (2)

- S/D Area Minimization
  - minimize S/D junction areas to keep capacitance low
- I/O Pads
  - Placement: must be able to route I/O signals out of cell
  - Pad Layer: metal1 for smaller cells, metal2 acceptable in larger cells
- Cell Boundary
  - extend VDD and GND rail at least 1.5λ beyond internal features
  - extend n-well to cell boundary to avoid breaks in higher level cell

Cell View and Cell Ports

- Cell View
  - see only I/O ports (including power), typically in Metal1
  - can't see internal layer polygons of the primitive



Cell-level view of INV, NAND, and NOR primitives

- Ports
  - all signals that connect to higher level cells
  - physical locations of the layout cell, typically in Metal1or Metal2
- Metal1 vs Metal2 ports
  - best to keep ports in Metal1 for primitives
  - always try to use only the lowest level metals you can

Cell-based Design

- Cell-based: once a set are defined, they may be used to create more complex networks

- A function using unit gate of Figure 5.26

$$f = \overline{a} \cdot b \qquad (5.16)$$

$$\Rightarrow 2X_{NOT} + X_{NAND} \qquad (5.17)$$

- In this case, a new complex cell F1 will become to the new unit component, and this block without decomposing it into the primitive cells

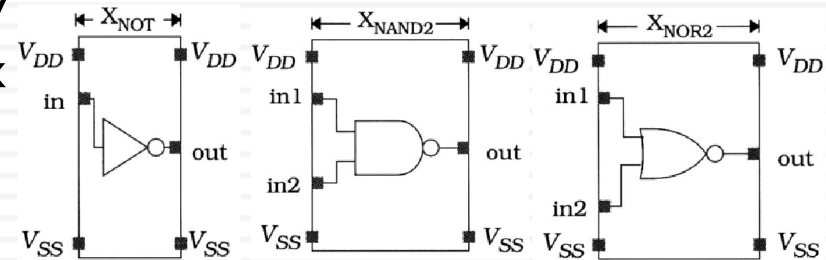
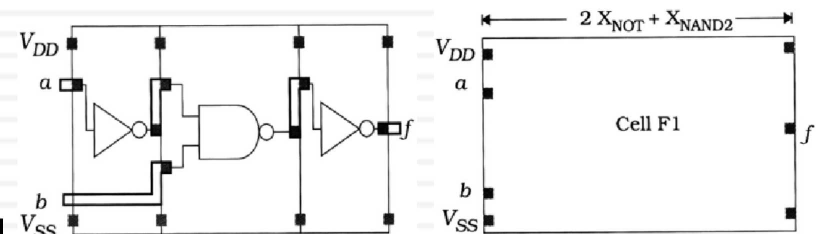


Figure 5.26 Logic gates as basic cells



(a) Primitive (b) New complex cell

Figure 5.27 Creation of a new cell using basic units

Cell-based:VDD & VSS Placement

- Power supply lines placement
  - Both are shown on the Metal1

$D_{m1\text{-}m1}$ = Edge-to-Edge distance between VDD and VSS

  - Pitch

$P_{m1\text{-}m1}$ = Distance between the middle of the VDD and VSS lines

  - The two are related by, where WDD is the width of the power supply lines

$$P_{m1\text{-}m1} = D_{m1\text{-}m1} + W_{DD} \quad (5.18)$$

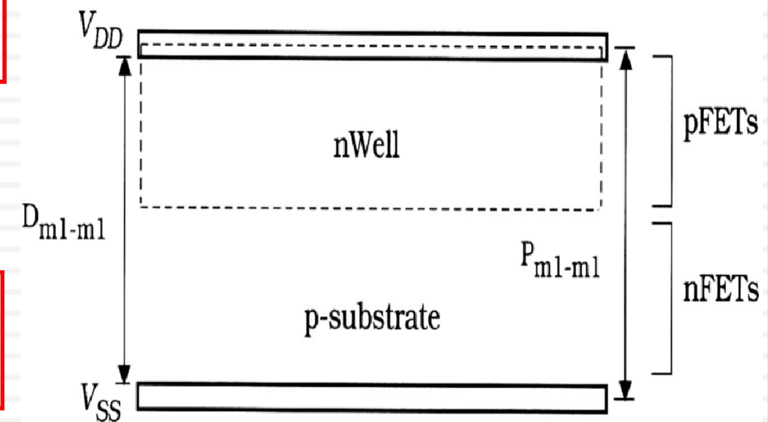
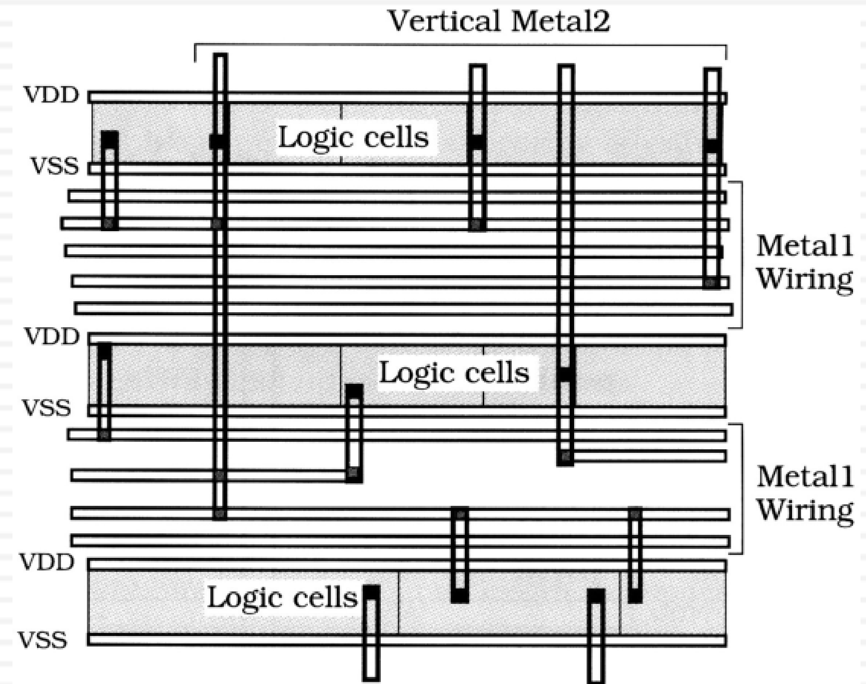


Figure 5.28 VDD and VSS power supply lines

Cell-based: FET Placement

- Tiling Placement
  - Arrays of parallel metal1are used for interconnect
  - Both Metal1 and Metal2 are used for routing which gives more flexibility
  - Metal1 arrays consume significant area leading to a decreased chip density



Weinberger Image Placement

- A high-density technique is to alternate VDD and VSS power lines
  - "Inverted logic cells" are defined to be flipped in relation to the rows of "Logic cells"
  - High-density placement rate
- Major drawback: must use Metal2 or higher metal layer to achieve this approach

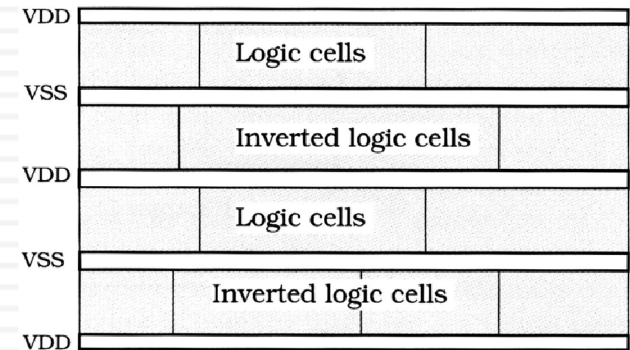


Figure 5.33 Weinberger image array

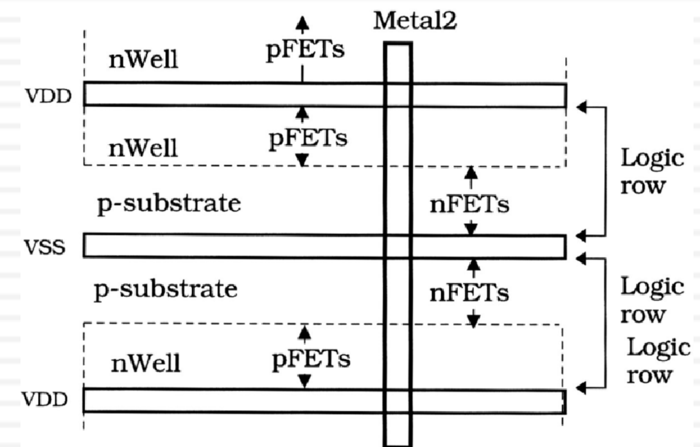


Figure 5.34 FET placement in a Weinberger array

Outline

- Basic Concepts
- Design Rules
- Physical Design of Logic Gates
- FET Sizing and the Unit Transistor
- Cell Concepts
- Design Hierarchies

Design Hierarchies

- Top-down hierarchy design
- Bottom-up hierarchy design

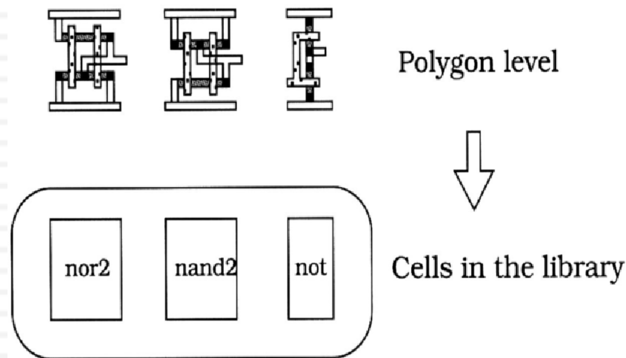


Figure 5.48 Primitive polygon-level library entries

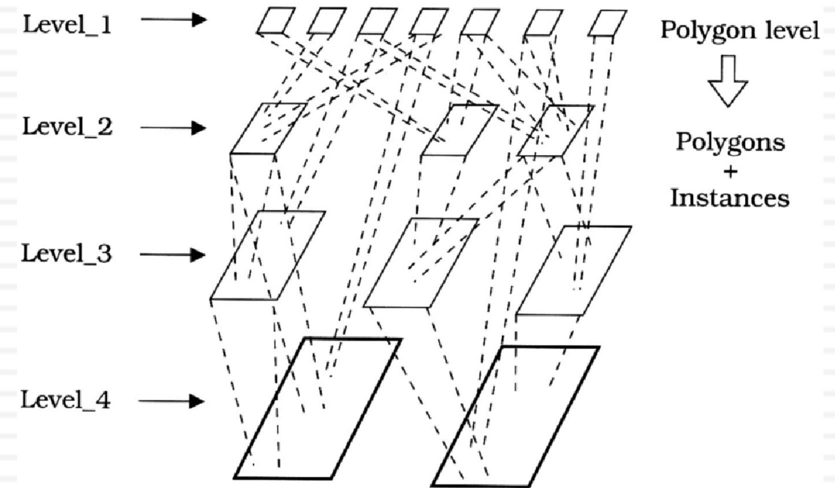


Figure 5.50 Cell hierarchy

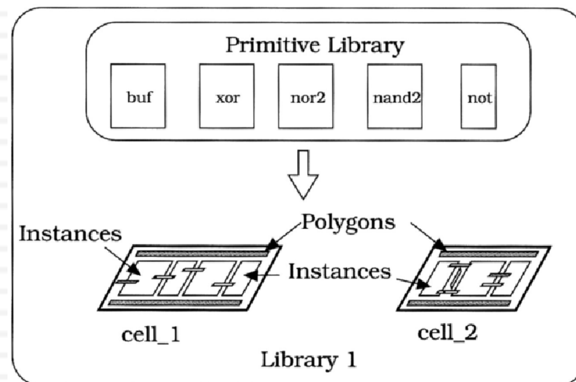


Figure 5.49 Expanding the library with more complex cells

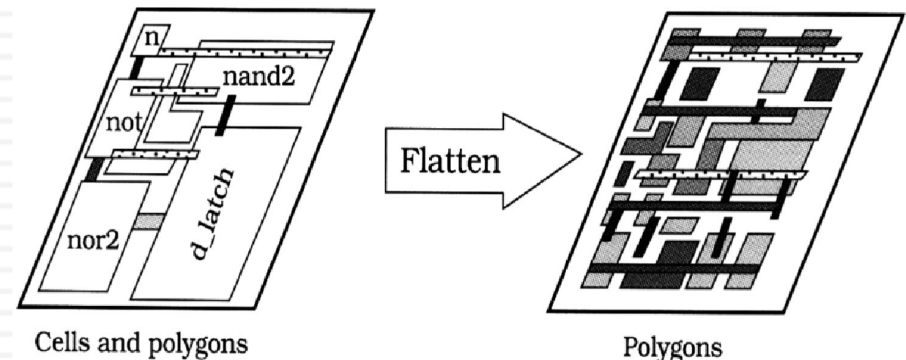
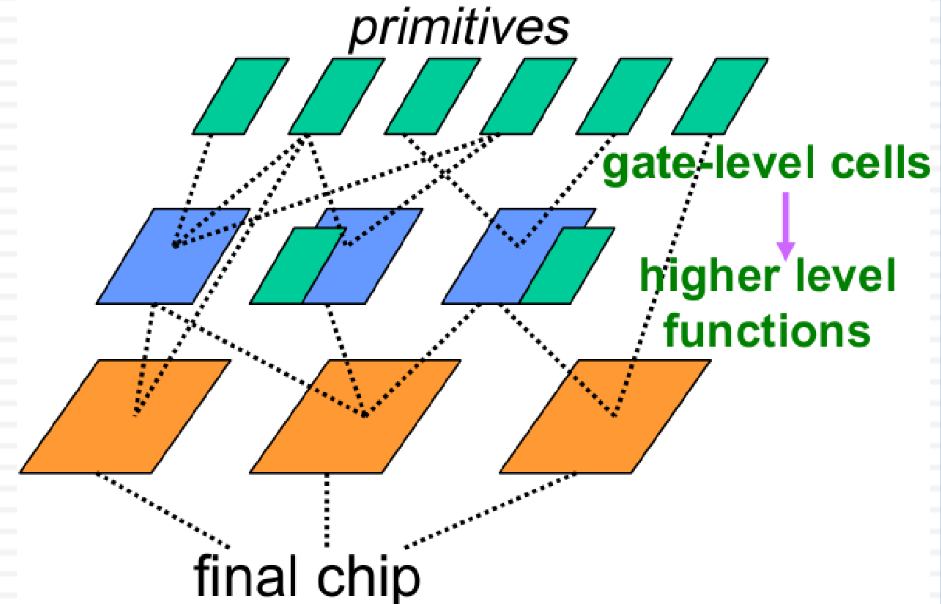


Figure 5.51 Effect of the flatten operation

Hierarchical Design

- Start with Primitives
  - basic transistor-level gates/functions
  - optimize performance and layout
  - layout with polygons
- Build larger cells from primitives
  - layout with instances of primitives
  - polygons for transistors and routing
- Build even larger cells
  - layout with instances of lower level cells
  - polygons only for signal routing
- Repeat for necessary levels of hierarchy until Final Chip

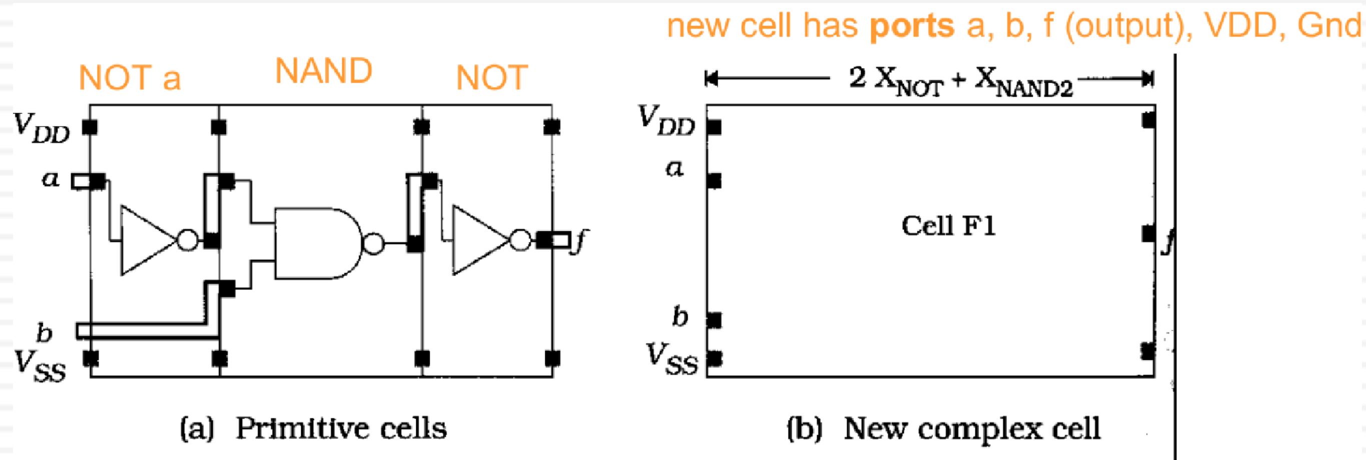


- Advantages of Hierarchical Design:
  - allow layout optimization within each cell
  - eases layout effort at higher level
    - higher level layout deal with interconnects rather than tx layout

Primitives must be done using custom techniques, but higher level layout can use automated (place-and-route) CAD tools

Hierarchical Design Concepts

- Building Functions from Primitives
  - instantiate one or more lower-level cells to from higher-level function
  - Example: f = $a\,\overline{b}$



(a) Primitive cells

(b) New complex cell

Hierarchical Design Concepts (2)

- Final Chip
  - flatten all cells to create one level of polygons
  - allows masks to be made for each layout layer
  - removes hierarchy

IMPORTANT:

Don't flatten your cells! There are other ways to peak (see) lower level cells instantiated within a higher level cell