PHYSICAL STRUCTURE OF CMOS INTEGRATED CIRCUITS

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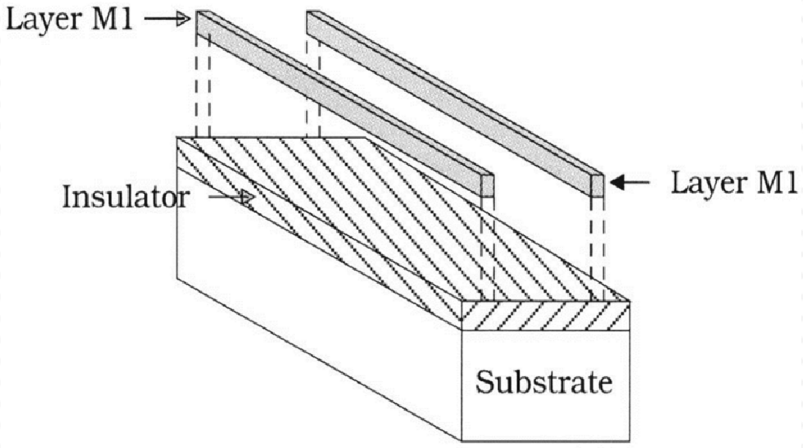
Outline

- Integrated Circuit Layers
- MOSFETs
- CMOS Layers
- Designing FET Arrays

Integrated Circuit Layers

- CMOS integrated circuits are electronic switching networks that are created on small area of a silicon wafer using a complex set of physical and chemical processes
- Integrated circuits are a stack of patterned layers
  - Metals, good conduction, used for interconnects
  - Insulators (silicon dioxide), block conduction
  - Semiconductors(silicon), conducts under certain conditions
- Stacked layers form 3-dimensional structures

Figure 3.1 Two separate material layers



Three-dimensional Structure

- Combining the top and side views of an IC allows us to visualize the three-dimensional structure
  - The side view illustrates the order of the stacking
  - Insulating layers separate the two metal layers so that they are electrically distinct
  - The patterning of each layer is shown by a top view perspective
- The stacking order is established in the manufacturing process, and can not be altered by the VLSI designer

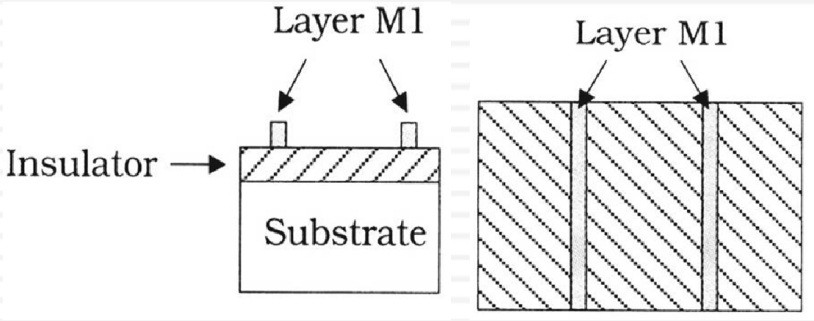


Figure 3.2 Layers after the stacking process is completed

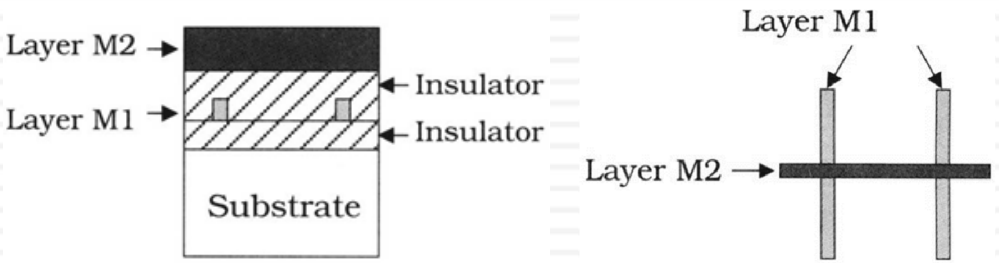


Figure 3.3 Addition of another insulator and a second metal layer

Interconnect Resistance and Capacitance

- Logic gates communicate with each other by signal flow paths from one point to another
  - Using patterned metal lines
  - Current flow is governed by the physical characteristics of the material and the dimensions of the line
  - *Ohm's law*

$$V = IR \qquad (3.1)$$

  - *Line resistance* R_{line}: a parasitic (unwanted) electrical element that cannot be avoided

$$A = wt \qquad (3.2)$$

$$R_{line} = \frac{l}{\sigma A} \qquad (3.3) \qquad (\sigma \text{:conductivity})$$

$$Since \quad \rho = \frac{1}{\sigma} \qquad (3.4) \qquad (\rho \text{ :resistivity})$$

$$\Rightarrow R_{line} = \rho \frac{l}{A} \qquad (3.5)$$

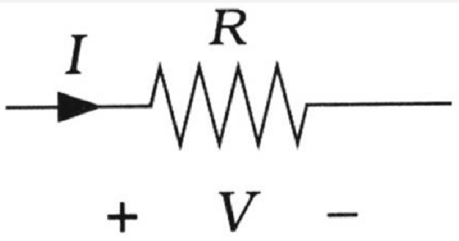


Figure 3.4 Symbol for a linear resistor

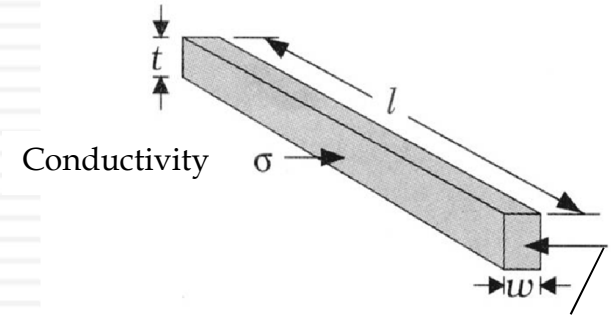


Figure 3.5 Geometry of a conducting line

Sheet Resistance Model

- Sheet resistance R_s, rewriting $R_{line} = \rho \frac{l}{A}$

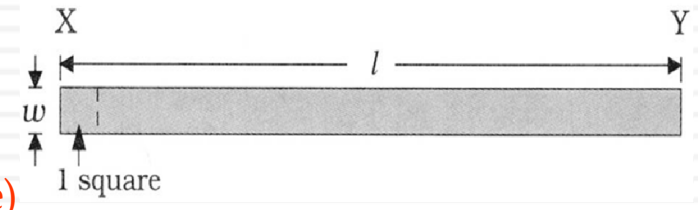
$$\Rightarrow R_{line} = \left(\frac{1}{\sigma t}\right)\left(\frac{l}{w}\right) \quad (3.6)$$

$$R_s = \frac{1}{\sigma t} = \frac{\rho}{t} \quad (3.7) \quad \text{(sheet resistance)}$$

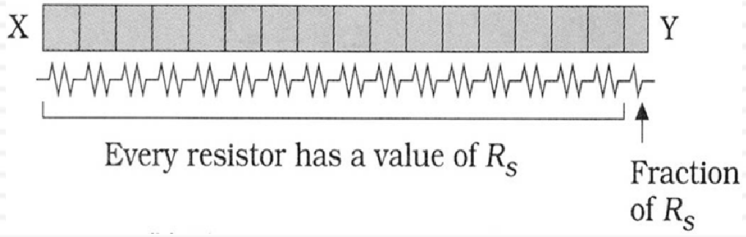
$$\Rightarrow R_{line} = R_s\left(\frac{w}{w}\right) = R_s \quad (3.8)$$

$$\Rightarrow R_{line} = R_s n \quad (3.9)$$

$$where \quad n = \frac{1}{w} \quad (3.10)$$



(a) Top-view geometry

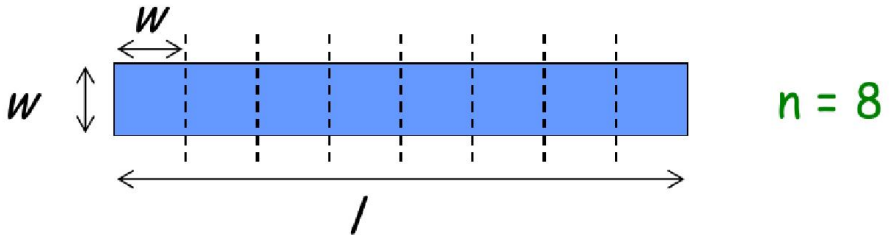


(b) Sheet resistance contributions

Figure 3.6 Top-view geometry of a patterned line

- We can determine how many 'squares' of the layer are present from the top view of layout,
- Example

  $R = 8*R_s$



Capacitor

- Interconnect lines also exhibit the property of capacitance
  - In electronics, the element that stores charge is called *capacitor*

$$Q = CV \quad (3.11)$$

  - Since electric current is defined by the time derivative $I = (dQ/dt)$, differentiating gives the *I-V* equation

$$I = C\frac{dV}{dt} \quad (3.12)$$

  - Capacitance exists between any two conducting bodies that are electrically separated
    - For the interconnect line, the conductor is isolated from the substrate by an insulating layer of silicon dioxide glass
    - So, the capacitance depends on the geometry of the line

$$C_{line} = \frac{\varepsilon_{ox} wl}{T_{ox}} \quad (3.13) \quad \text{(parallel-plate formula)}$$

Where ε_{ox} is the permittivity of the insulating oxide F / cm

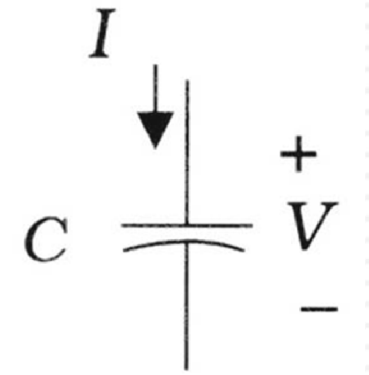


Figure 3.7 Circuit symbol for a capacitor

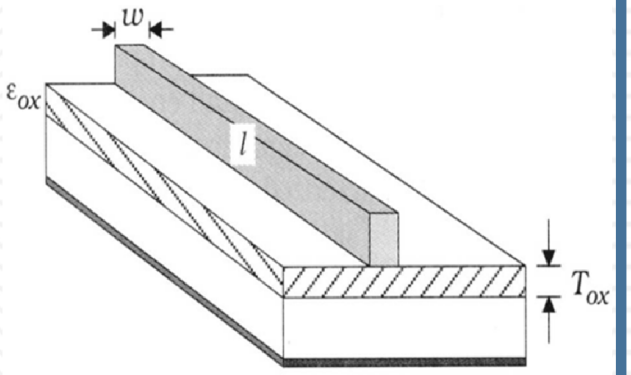


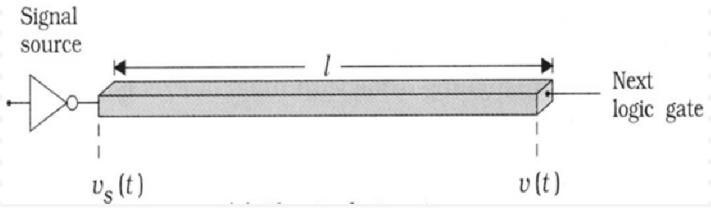
Figure 3.8 Geometry for calculating the line capacitance

Delay: RC Time Constant

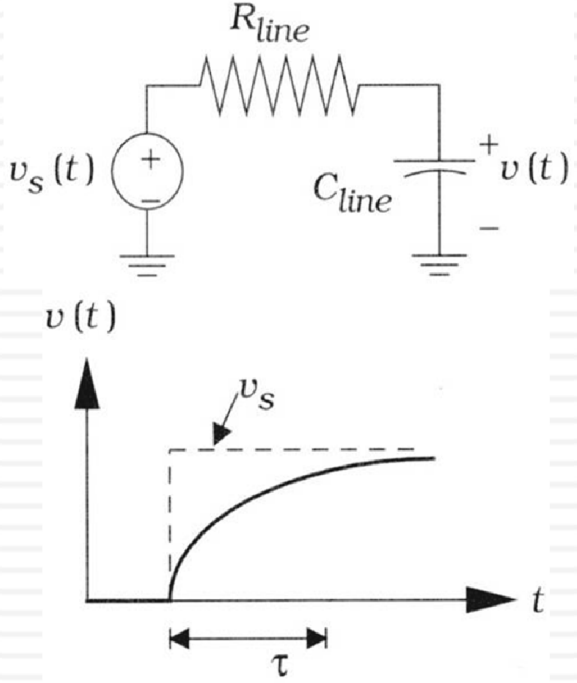
- The interconnect line exhibits both parasitic resistance R_{line} [Ω] and capacitance C_{line} [F]
  - Forming the product of these two quantities gives

$$\tau = R_{line}C_{line}\ [s] \qquad (3.14)$$

- In high speed digital circuits, signals on an interconnect line are delayed by τ , which places a limiting factor on the speed of the network
  - VLSI processing are directed toward minimizing both R_{line} and C_{line}
  - Circuit designers are then faced with creating the fastest switching network within the limits of delay



(a) Physical structure



(b) Circuit model

Figure 3.9 Time delay due to the interconnect time constant

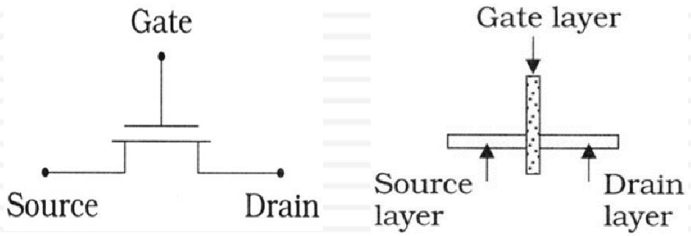
Outline

- An Overview CMOS Fabrication
- Integrated Circuit Layers
- MOSFETs
- CMOS Layers
- Designing FET Arrays

MOSFETs

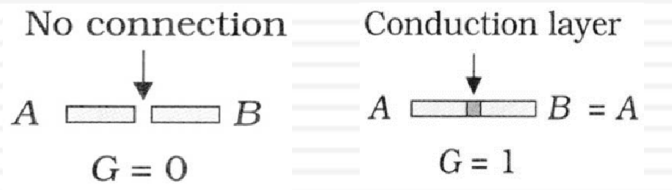
- MOSFET is a small area set of two basic patterned layers that together act like a controlled switch
  - The voltage applied to the gate determines the electrical current flow between the source and drain terminals
- Assuming that the drain and source are formed on the same layer, then this behavior can be used to deduce that

The gate signal G is responsible for the absence or presence of the conducting region between the drain and source region



(a) nFET symbol (b) pFET symbol

Figure 3.10 nFET circuit symbol and layer equivalents

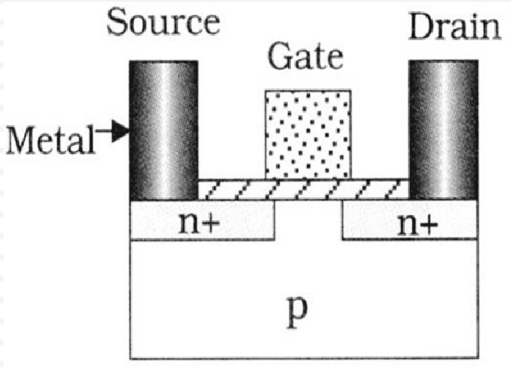


(a) Open switch (b) Closed Switch

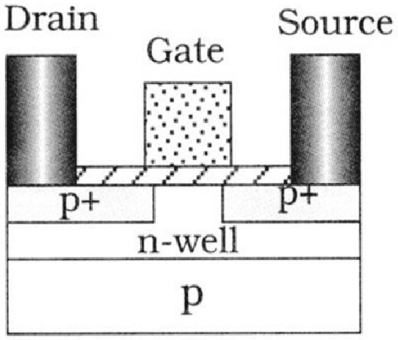
Figure 3.11 Simplified operational view of an nFET

nFET and pFET

- The polarity of a FET (*n* or *p*) is determined by the polarity of the drain and source regions
- *nFET*: the drain and source regions are labeled as "n+" to indicate that they are **heavily doped** as Figure 3.16 (a) showing
- *pFET*: the source and drain regions are p+ sections that are embedded in an n-type "well" layer as Figure 3.16 (b) showing
- All pn junction are used to prevent current flow between adjacent layers



(a) nFET cross-section

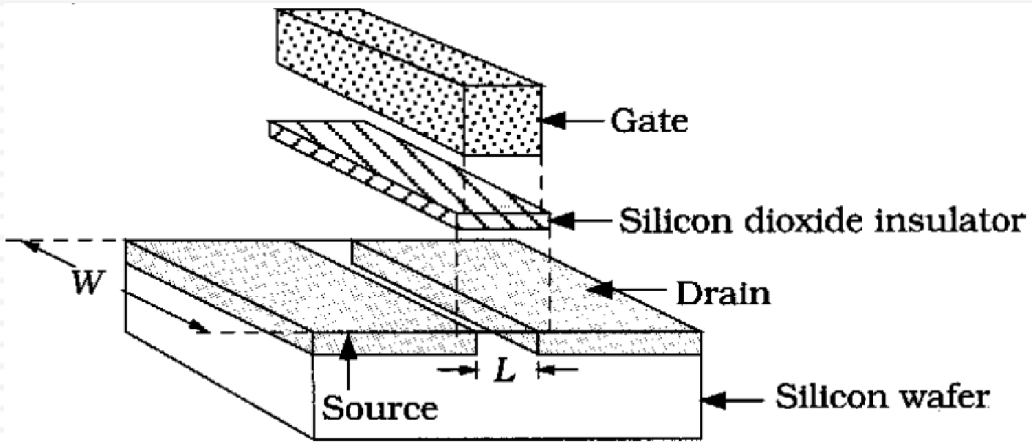


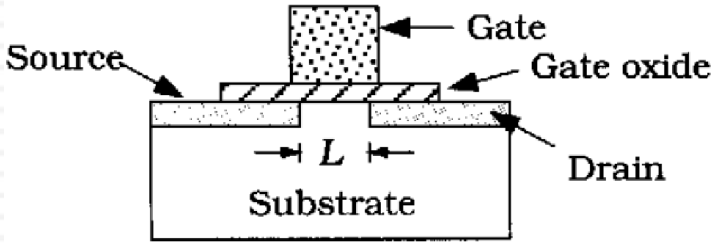
(b) pFET cross-section

Figure 3.16 nFET and pFET layers

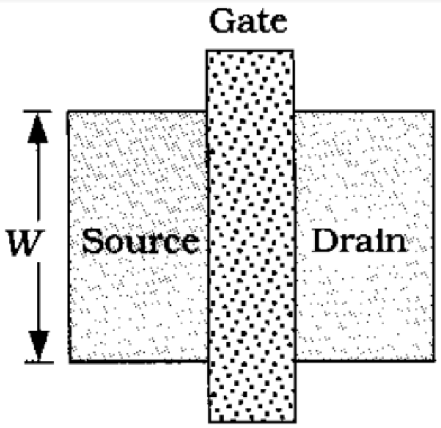
MOSFET Device Dimensions

- Physical dimensions of a MOSFET
  - L = channel length
  - W = channel width
  - *W/L* = aspect ratio
- Side and Top views





(a) Side view



(b) Top view

Outline

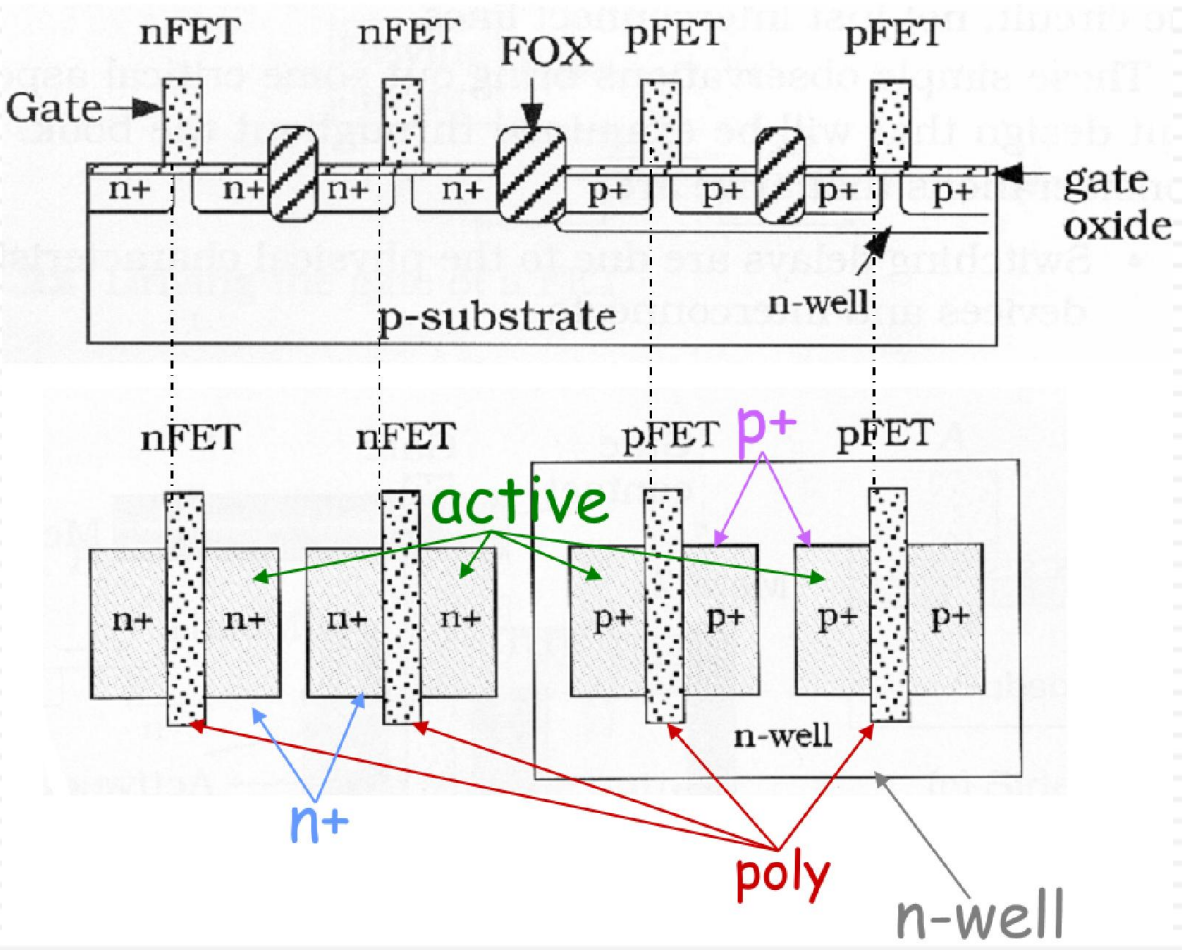
- Integrated Circuit Layers
- MOSFETs
- CMOS Layers
- Designing FET Arrays

n-well Process

- CMOS fabrication process: In simplest terms, this refers to the sequence of steps that we use to take a bare "wafer" of silicon to the finished form of an electronic integrated circuit
- The n-well process starts with a p-type substrate (wafer) that is used as a base layer
- nFETs can be fabricated directly in the p-type substrate
- N-well regions are needed to accommodate p-type substrate

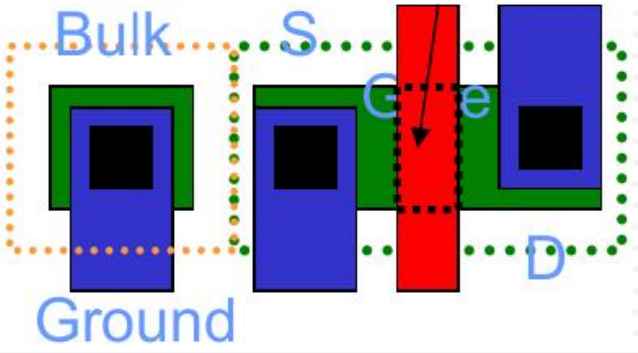
Lower CMOS Layers

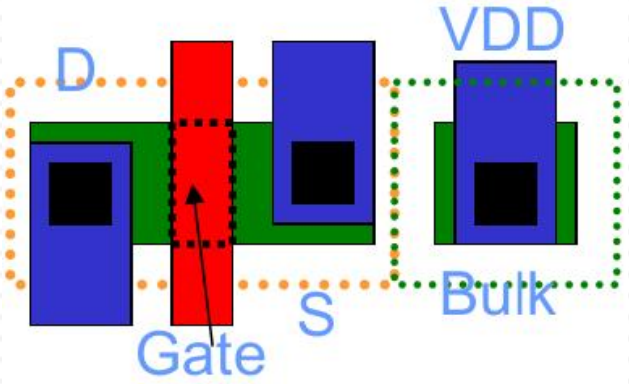
- Visible Features
  - p-substrate
  - n-well
  - n+ S/D regions
  - p+ S/D regions
  - gate oxide
  - poly silicon gate
- Mask Layers
  - n-well
  - active(S/D regions)
  - active = not FOX
  - n+ doping
  - p+ doping
  - poly patterning
- gate oxide aligned to gate poly, no oxide mask



Physical Realization of 4-Terminal MOSFETs

- nMOS Layout
  - gate is intersection of Active, Poly, and n Select
  - S/D formed by Active with Contact to Metal1
  - bulk connection formed by p+ tap to substrate
- pMOS Layout
  - gate is intersection of Active, Poly, and p Select
  - S/D formed by Active with Contact to Metal1
  - bulk connection formed by n+ tap to n Well
- nActive should always be covered by nSelect
- pActive should always be covered by pSelect
- nActive and pActive are the same mask layer (active) (help to differentiate nMOS/pMOS)





Upper CMOS Layers

- Cover lower layers with oxide insulator, Ox1
- Contacts through oxide, Ox1
  - metal1 contacts to poly and active
- Layers: (Metal, Insulator Ox2, Via contacts, Metal 2, Repeat insulator/via/metal)
- Full Device Illustration
  - active
  - poly gate
  - contacts (active & gate)
  - metal1
  - Via
  - metal2

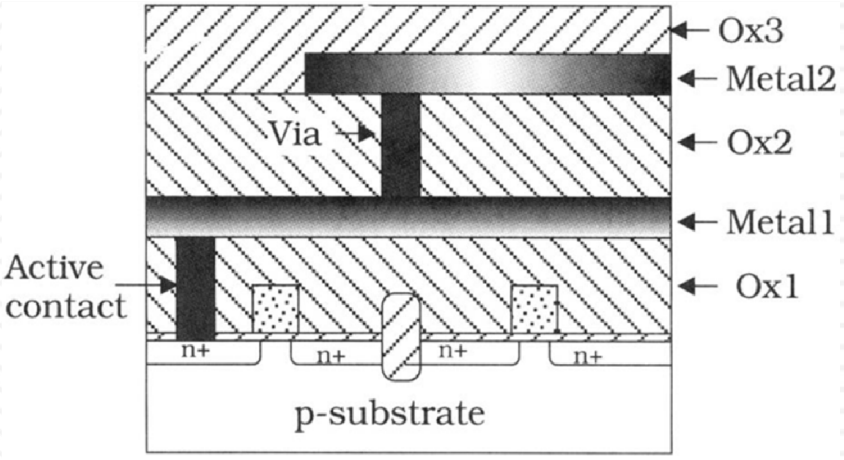


Figure 3.25 Metal interconnect layers

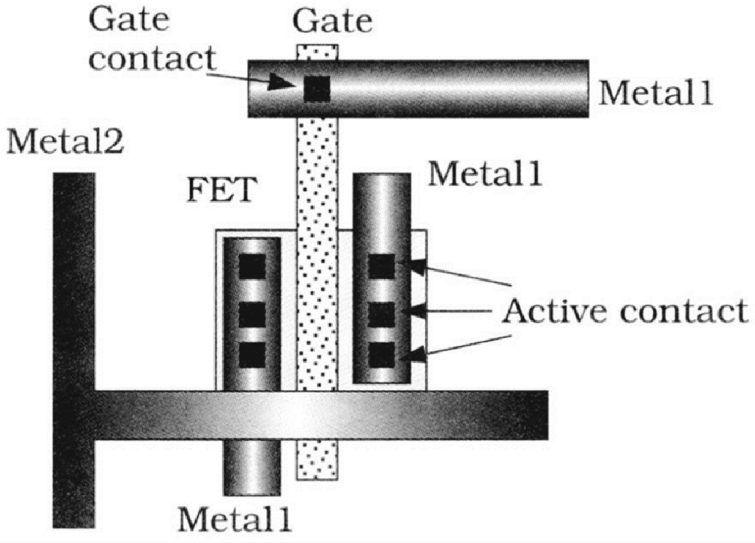
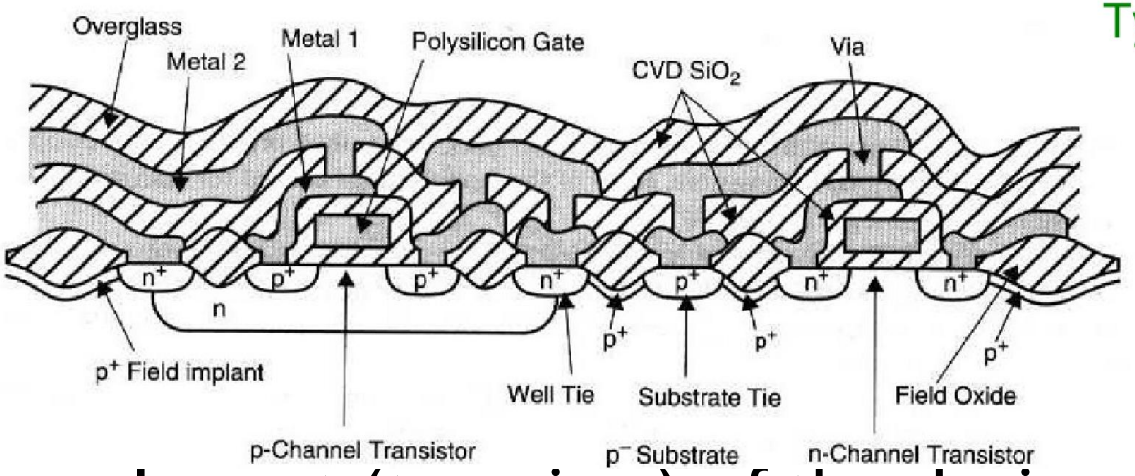
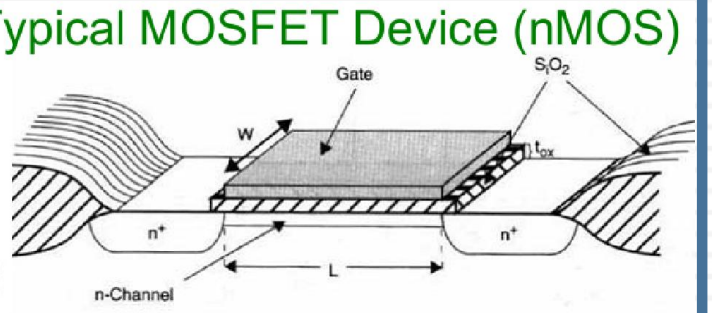


Figure 3.26 Interconnect layout example

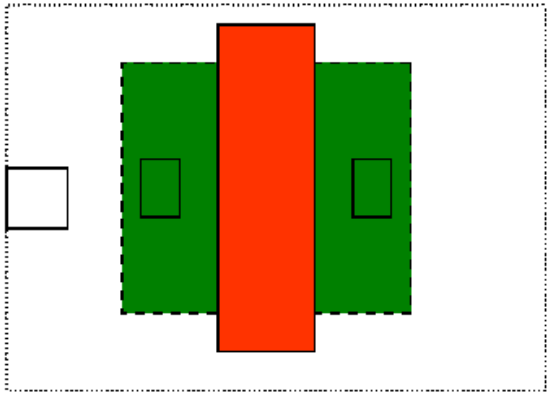
CMOS Cross Section View

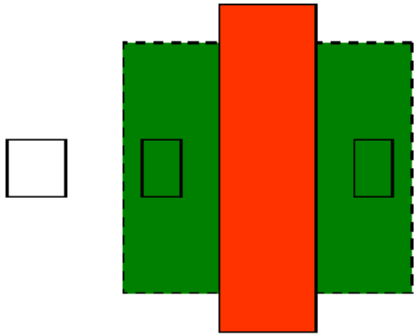
- Cross section of a 2 metal, 1 poly CMOS process





- Layout (top view) of the devices above (partial, simplified)





Outline

- Integrated Circuit Layers
- MOSFETs
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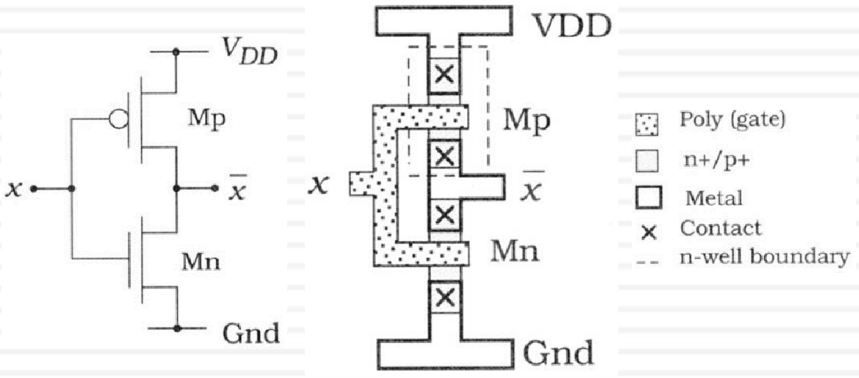
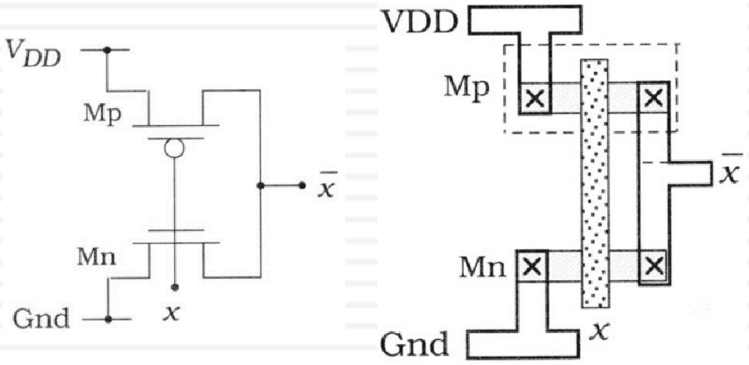
Basic Gates Design

- Design notes
  - Both the power supply (VDD) and ground (GND) are routed using the Metal layer
  - n+ and p+ regions are denoted using the same fill pattern. The difference is that pFETs are embedded within an n-well boundary
  - Contacts are needed from Metal to n+ or p+ since they are at different levels in the structure



(a) Circuit (b) Layer Patterning

Figure 3.31 Translating a NOT gate circuit to silicon

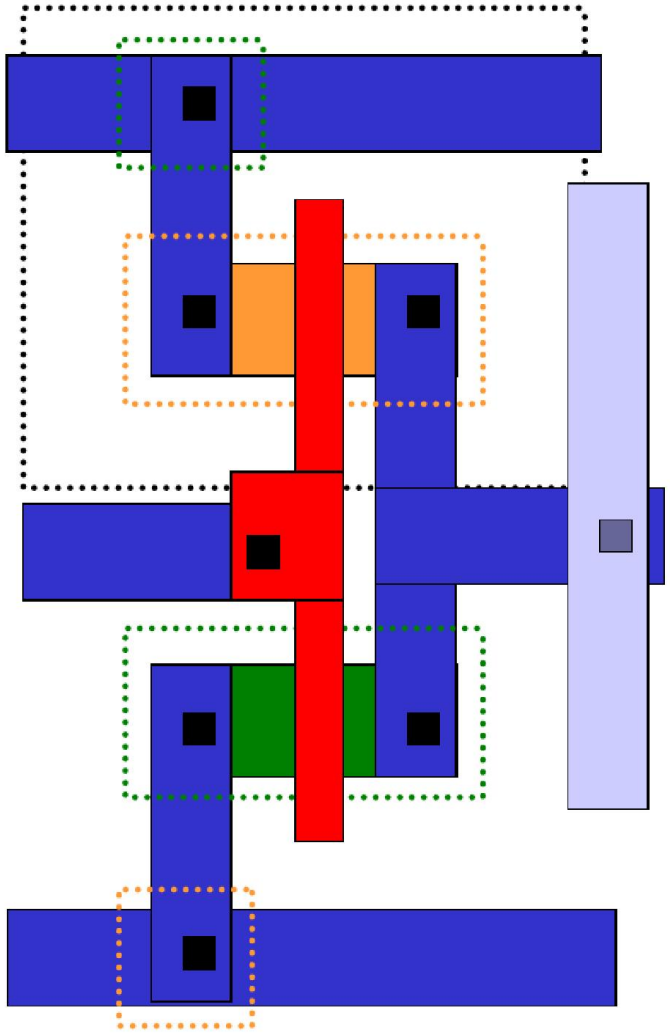


(a) Circuit (b) Layer Patterning

Figure 3.32 Alternate layout for a NOT gate

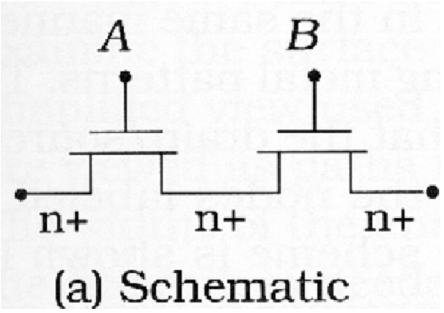
CMOS Inverter Layout

- Mask layers for 1 poly, 2 metal, n-well CMOS process
  - Background: p-substrate
  - nWell
  - Active (nactive and pactive)
  - Poly
  - pSelect
  - nSelect
  - Active **Contact**
  - Poly **Contact**
  - Metal1
  - Via
  - Metal2
  - Overglass

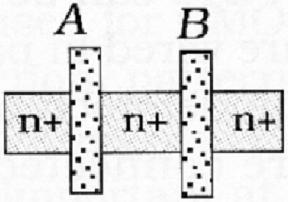


Series MOSFET Layout

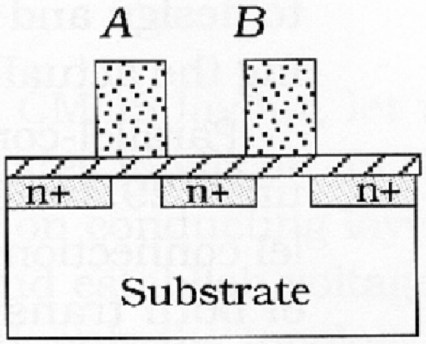
- Series txs (2 txs share a S/D junction)



(a) Schematic

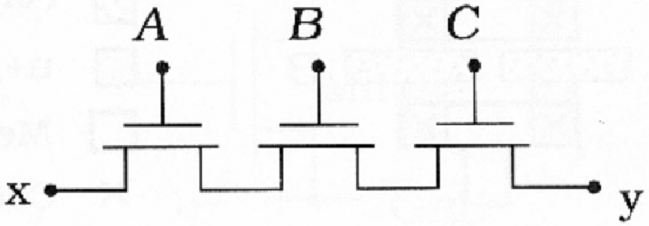


(b) Surface pattern

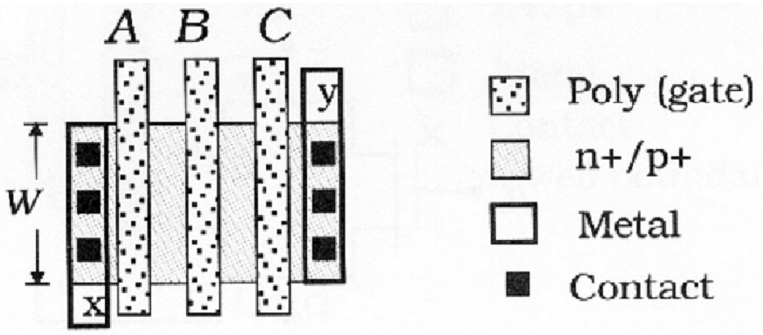


(c) Side view

- Multiple series transistors (draw gates side-by-side)



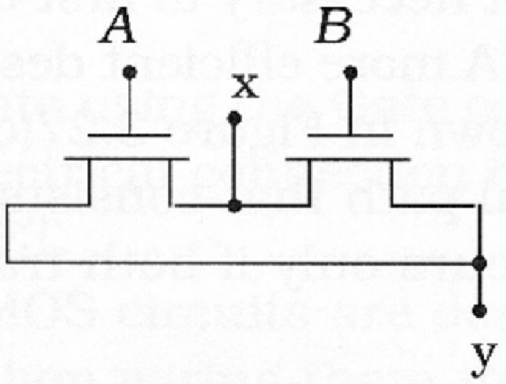
(a) Schematic



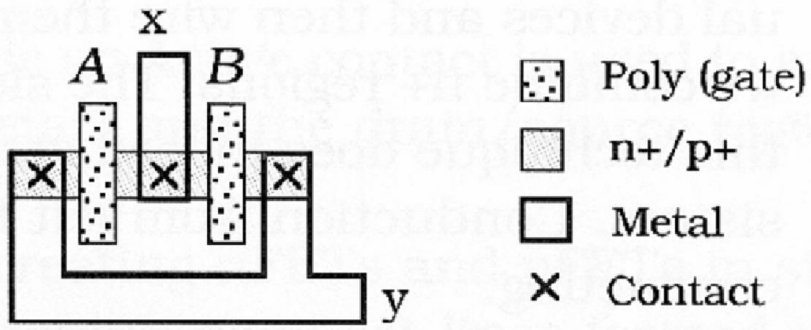
(b) Surface pattern

Parallel MOSFET Layout

- Parallel txs
  - one shared S/D junction with contact
  - short other S/D using interconnect layer (metal1)

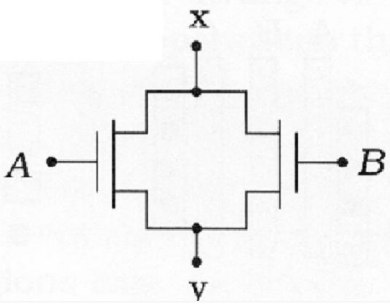


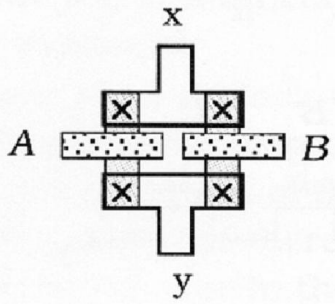
(a) Schematic



(b) Surface pattern

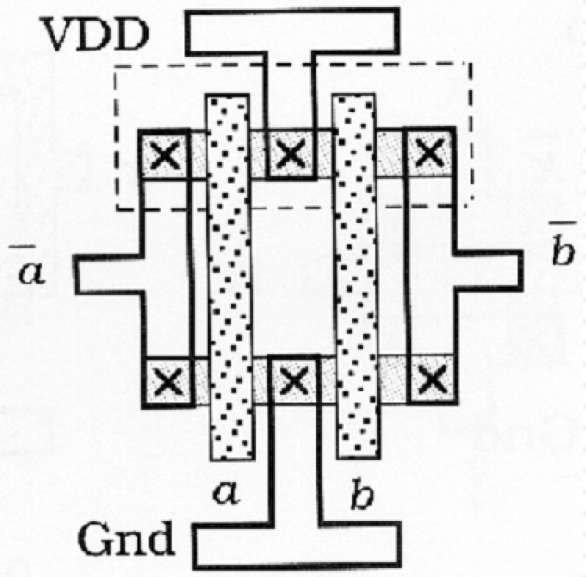
- Alternate layout strategy
  - horizontal gates





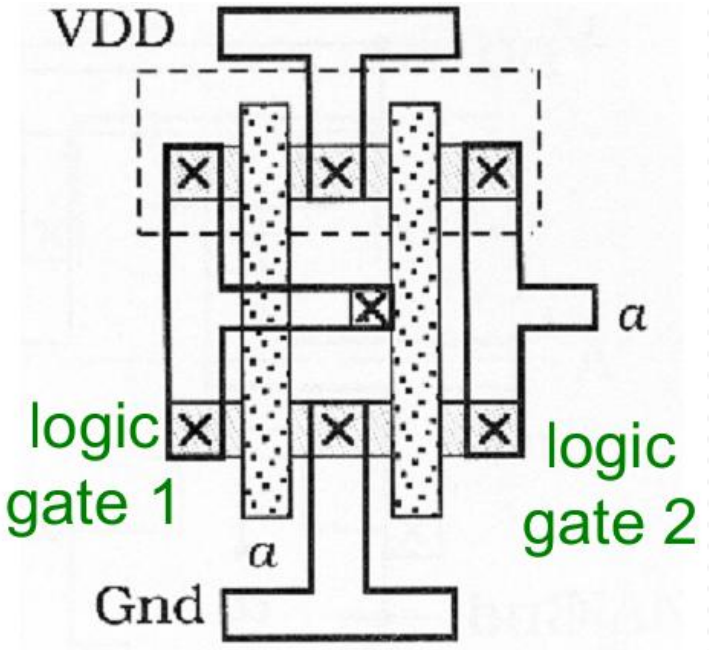
Multi Functional Cells

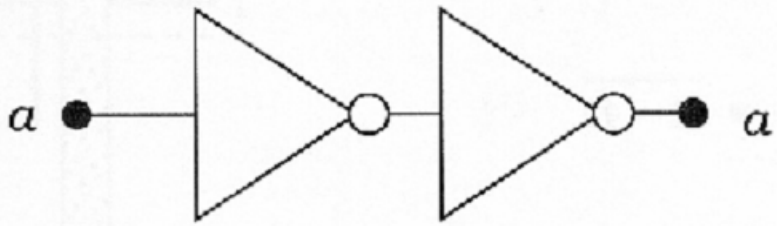
- Sharing power supply rail connections
  - independent gate inputs and outputs
  - shared power supply nodes
  - logic function?



Multi Functional Cells (2)

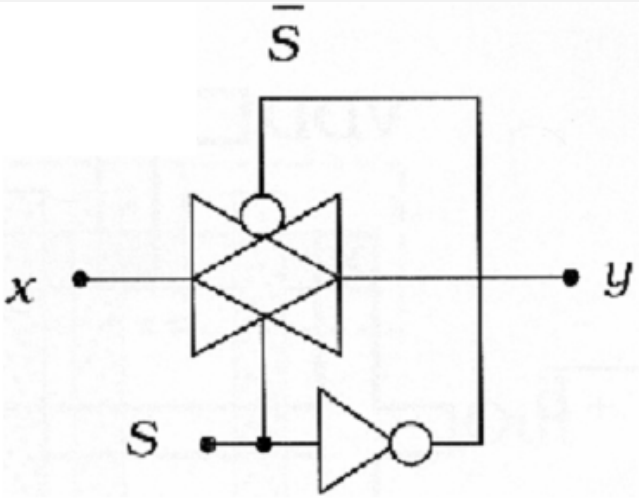
- Cascaded Gates
  - output of gate 1 = input of gate
  - g1 output metal connected (via contact) to g2 gate poly
  - shared power supply node
  - function?
  - non-inverting buffer





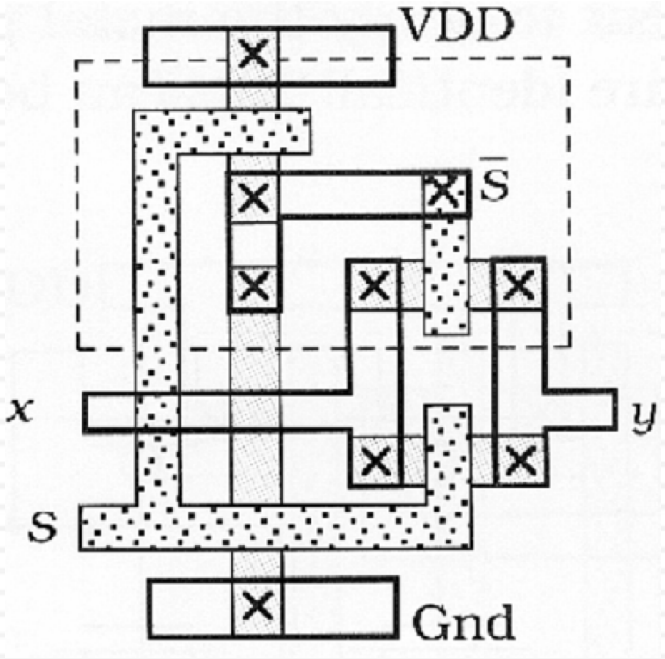
Complex Intra-Cell Routing

- Transmission gate with built-in select inverter
  - one TG gate driven by *s* at inverter input
  - one TG gate driven by $\bar{s}$ at inverter output
  - complicates poly routing inside the cell
  - figures uses n+ to route signal under metal 1
    - not great choice due to higher S/D junction capacitance



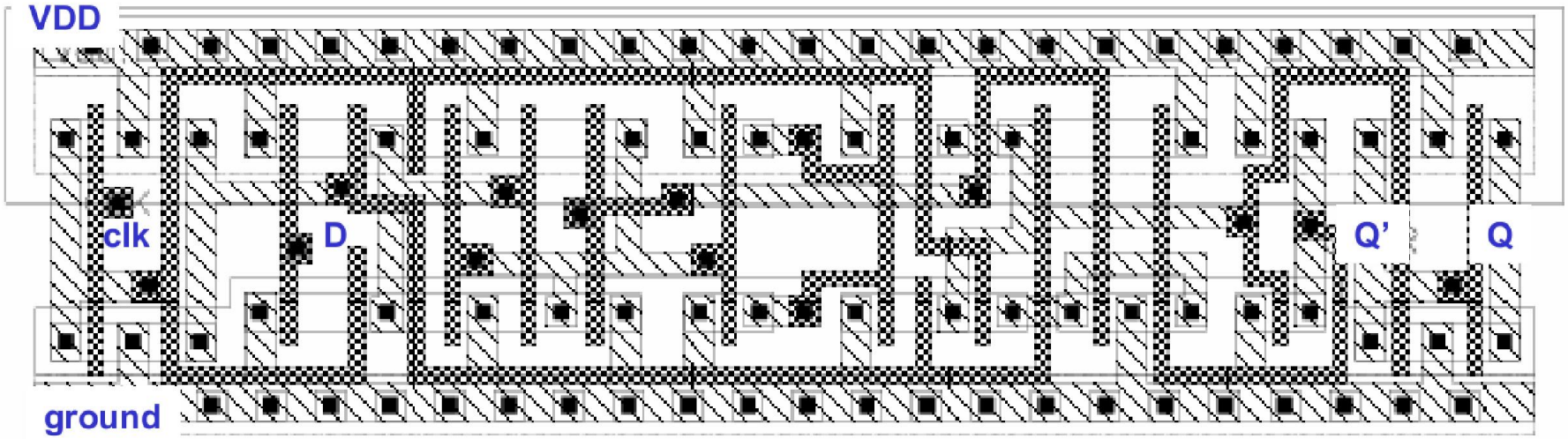
Complex Intra-Cell Routing (2)

- Routing rules
  - poly can cross all layers except
    - poly (can't cross itself)
    - active (n+/p+), this forms a transistor
  - metal can cross all layers except
    - metal (can't cross itself)



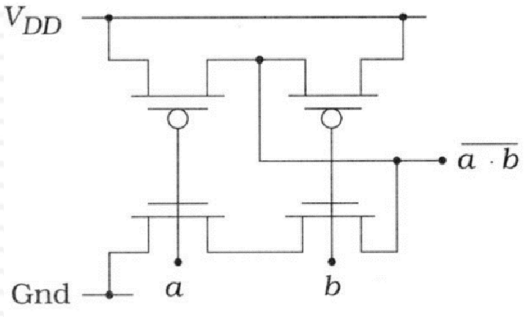
Example: Layout of Complex Cell

- D-type Flip Flop with Reset

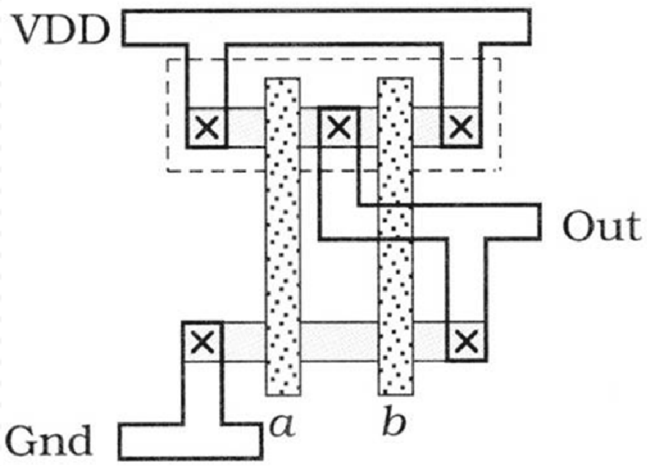


- Features
  - same pitch as inv, nand, nor, xor cells
  - complex intra-cell poly routing
  - passing under, above and between transistors
  - most I/O ports accessible via M1 or poly (M2 required for D)

NAND / NOR Gates

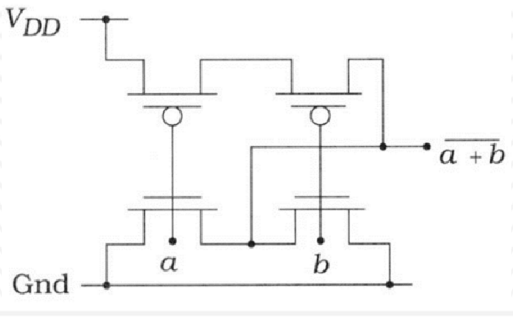


(a) Circuit

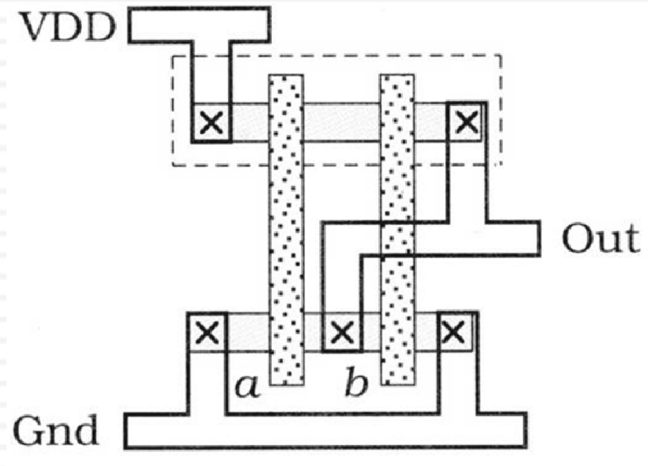


(b) Layout

Figure 3.36 NAND2 gate design



(a) Circuit



(b) Layout

Figure 3.37 NOR2 gate design

NAND-NOR Layout comparison

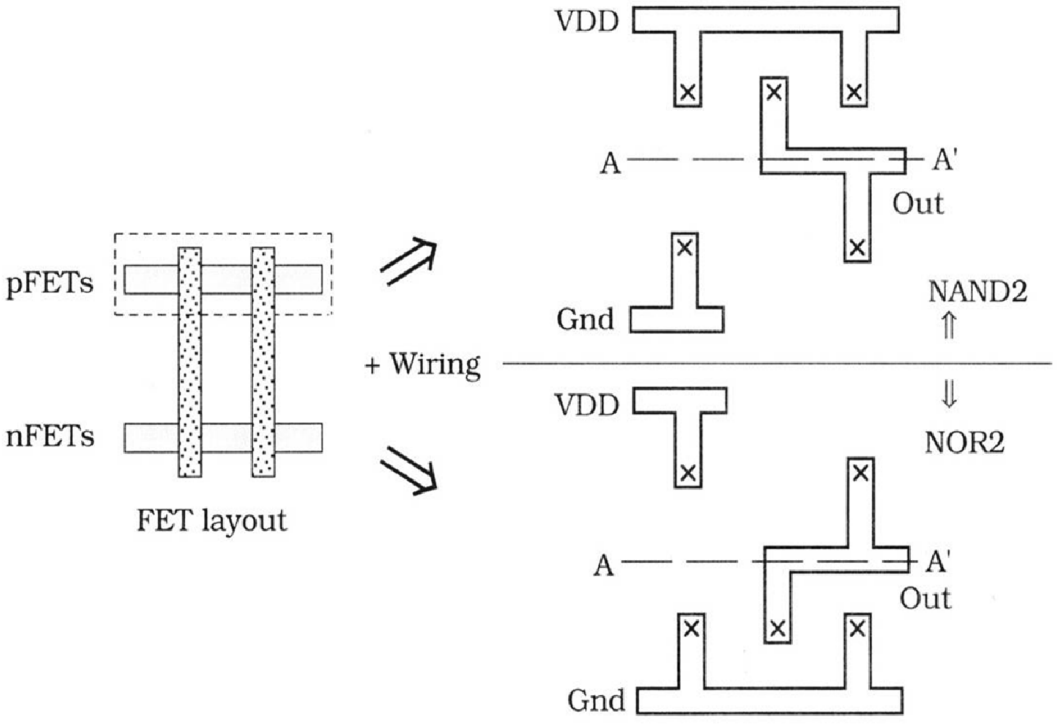
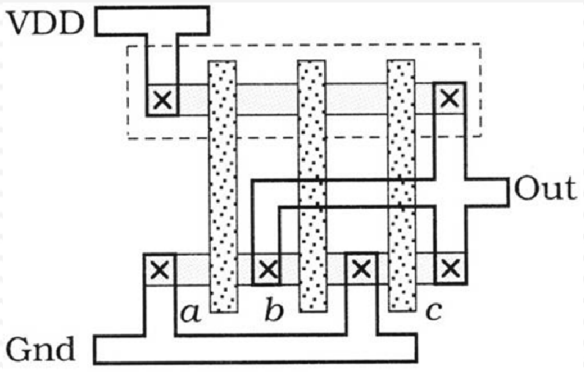
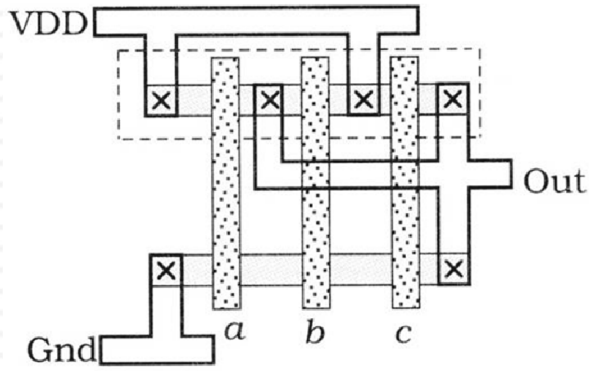


Figure 3.38 NAND2-NOR2 layout comparison



(a) NOR3



(b) NAND3

Figure 3.39 Layout for 3-input gates

Complex Logic Gates (1/2)

- Figure 3.40 shows the function

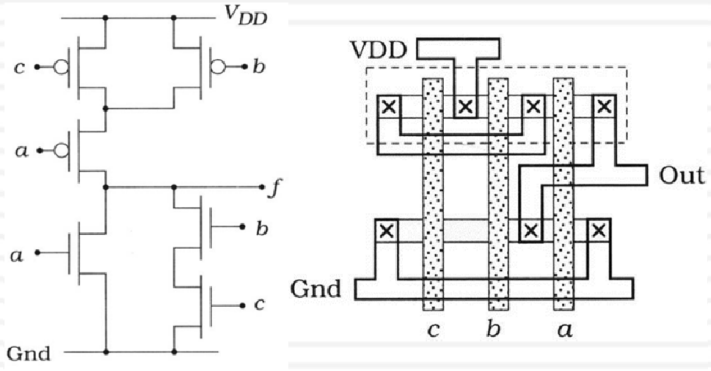
$$f = \overline{a + b \cdot c} \qquad (3.68)$$

  - The signal placement order is critical to obtaining the logic output

- Dual logic: In physical circuit, suppose that we flip the metal wiring pattern around an imaginary horizontal line. We will get

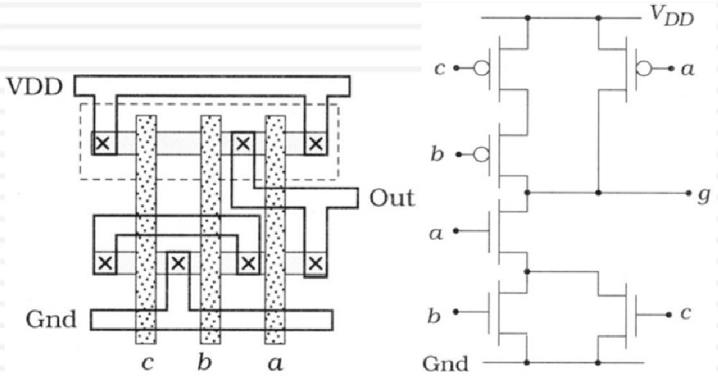
$$g = \overline{a \cdot (b + c)} \qquad (3.69)$$

- This is the same relationship that we found for the NOR-NAND gates



(a) Circuit (b) Patterning

Figure 3.40 Extension of layout technique to a complex logic gate



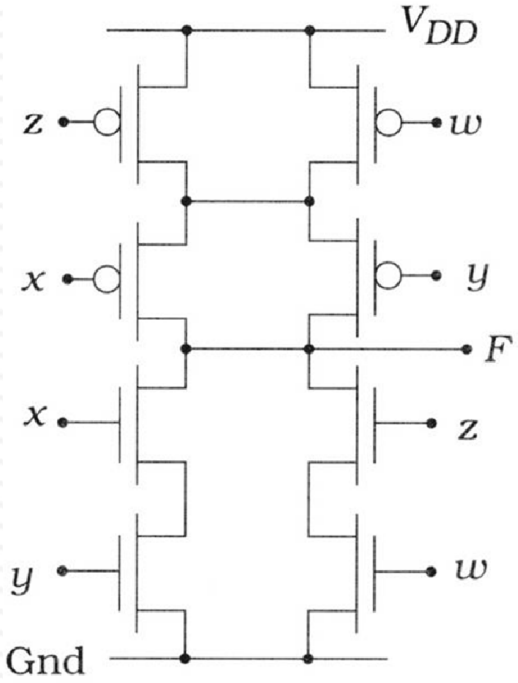
(a) Patterning (b) Circuit

Figure 3.41 Creation of the dual network

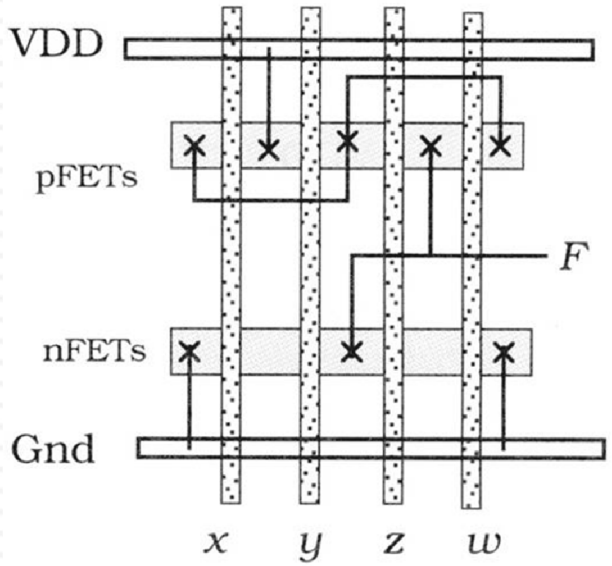
Complex Logic Gates (2/2)

- A logical function

$$F = \overline{x \cdot y + z \cdot w} \qquad (3.70)$$



(a) Circuit



(b) Layout wiring

Figure 3.42 A general 4-input AOI gate

General Discussion

- A basic techniques that it was possible to share n+ or p+ regions among several transistors
  - Randomly placed polygons should be avoided
  - It can reduce the area and wiring complexity
  - A power supply (VDD), a ground (VSS)
  - connection, and pFETs will be embedded in n-wells around VDD
  - nFETs are closer to the ground rail
- One approach to layout is based on the concept of simple *stick diagram*
  - It often used to perform quick layouts or
  - To study large complex routing problems
- Moreover, any CMOS circuit can be translated into an *equivalent graph* consisting of edges and vertices (Euler graph)

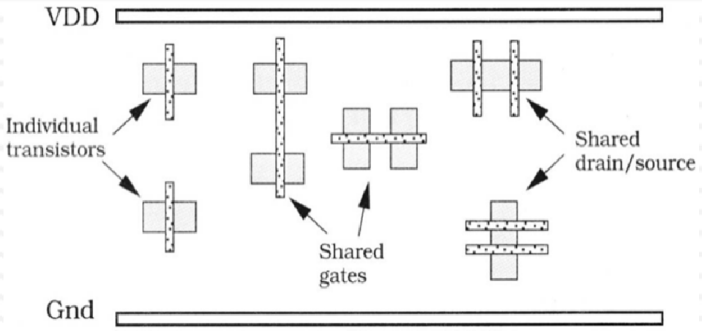


Figure 3.43 General gate layout geometry

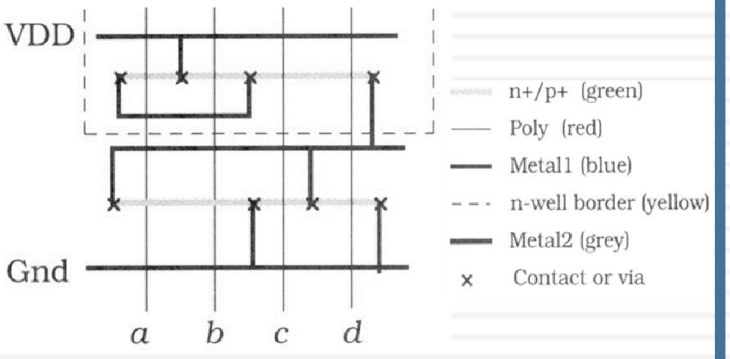


Figure 3.44 Basic stick layout diagram

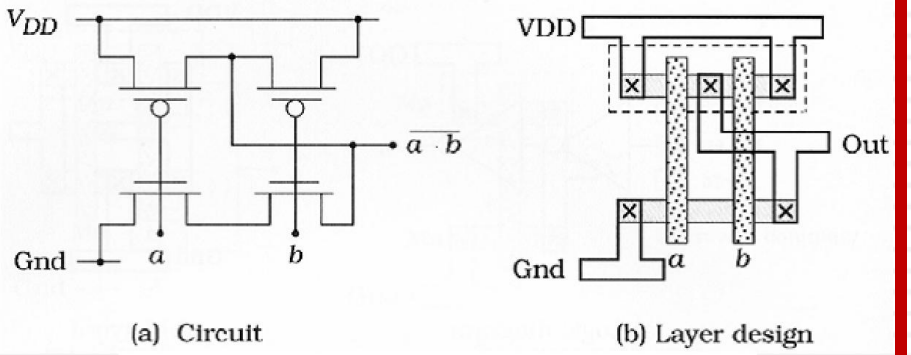
Mapping Schematics to Layout

- Layout organization: how to optimize layout connections
  - trial and error
  - works OK for simple gates but can require a lot of iterations
  - Stick Diagrams
  - simple method to draw layout options and see what is best before committing to "real" layouts
- Mapping techniques: how to arrange txs in layout
  - trial and error
  - works OK for simple gates
  - Euler Graph (pronounced "oiler")
  - graphical method to determine transistor arrangement in layout
- Best approach: combine some Euler Graph methods and Stick Diagrams

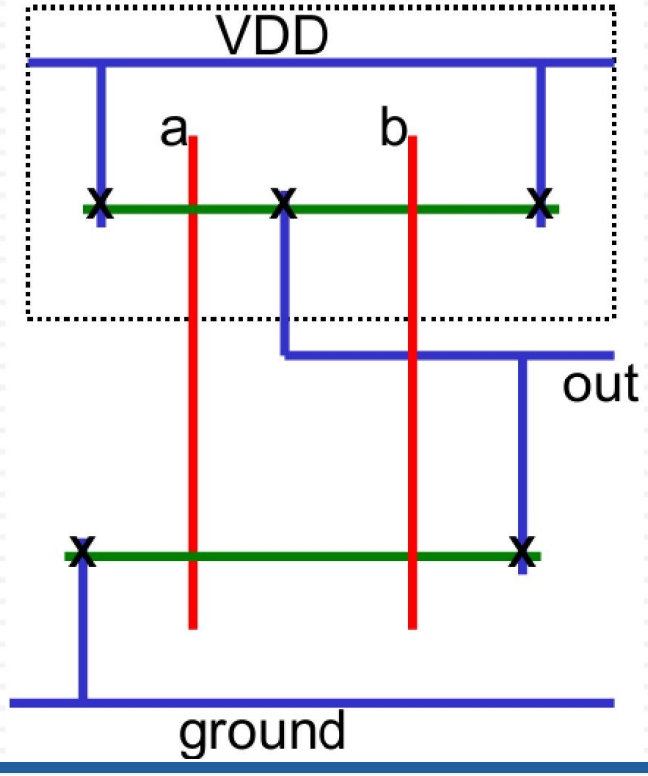
Stick Diagram method for sketching layouts

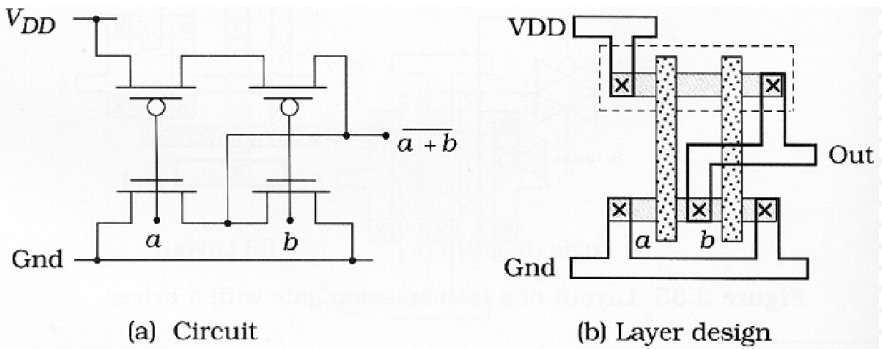
- Motivation
  - often hard to predict best way to make connections within a cell
  - Stick Diagram is a simple sketch of the layout that can easily be changed/modified/redrawn with minimal effort
- Stick Diagram
  - shows only active, poly, metal, contact, and n-well layers
  - each layer is color coded (typically use colored pencils or pens)
  - active, poly, metal traces are drawn with lines (not rectangles)
  - contacts are marked with an X
  - typically only need to show contacts between metal and active
  - n-well are indicated by a rectangle around pMOS transistors
  - typically using dashed lines
- Show routing between tx's, to VDD, Ground and Output

Stick Diagram of NAND & NOR

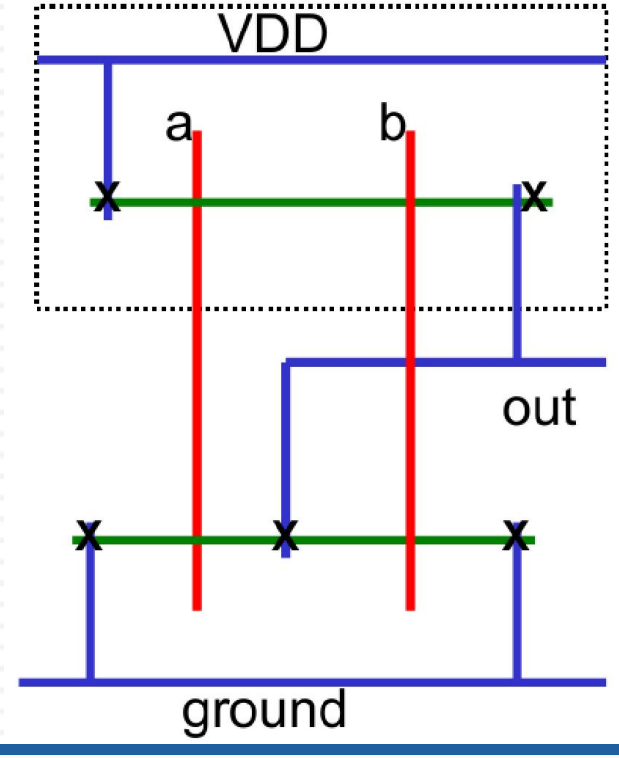


(a) Circuit (b) Layer design





(a) Circuit (b) Layer design

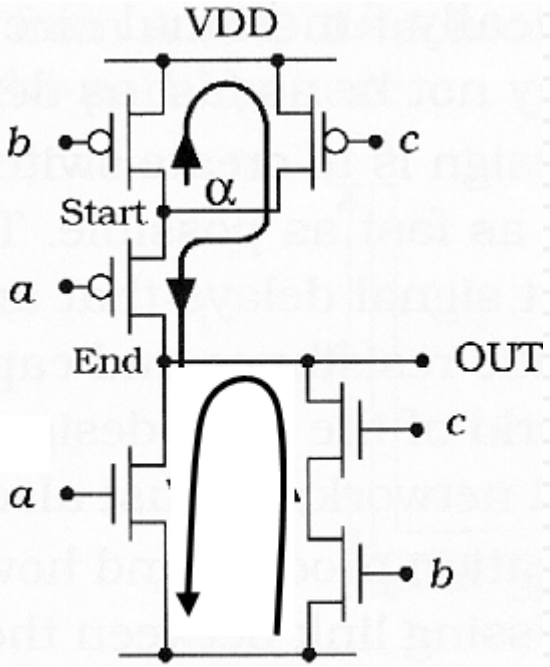


Euler "Path"

- Euler "Path"
  - simplified layout methodology for multi-input circuits; based on Euler Graphs
  - see textbook for full Euler Graph method; unnecessarily confusing for most students
  - used to determine what order (left to right) to layout transistors
  - identifies if all transistors will fit onto a single (non-broken) active strip
- Method
  - try to draw a loop through all transistors
  - separate loop for nMOS and pMOS
  - starting point can be anywhere; may need to try different points to achieve goals

Euler "Path" (2)

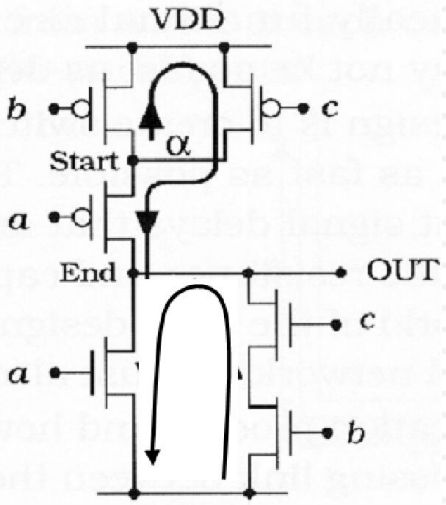
- Rules
  - can only trace through each transistor once
  - otherwise layout won't match schemati
  - can only re-cross any point/node once
  - otherwise multiple activestrips will be required to complete layout
  - must trace through nMOS in the same order as pMOS
- may have to rearrange txs in schematic (without changing function) to achieve rules

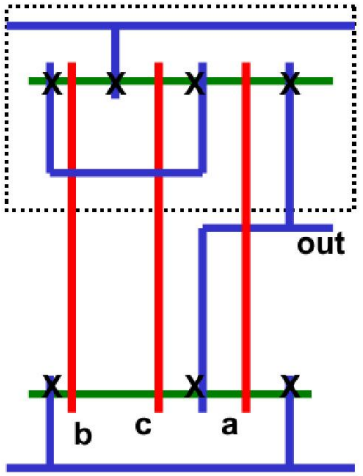


Euler Path Example

$$out = \overline{a + bc}$$

- PMOS Loop
  - start pMOS at node α, through 'b' to VDD, through 'c' to α, through 'a' to OUT
  - check loop follows rules
- NMOS Loop
  - trace through same tx order as pMOS
  - start nMOS at ground, through 'b' and to 'c' OUT then through 'a' to OUT again
- Form stick diagram with polys in order b, c, a determined by Euler Path
- Alternative Loops
  - start pMOS loop at OUT, through a, then b, then c.
  - to follow pMOS loop order, start at OUT, through a to ground then b, then c

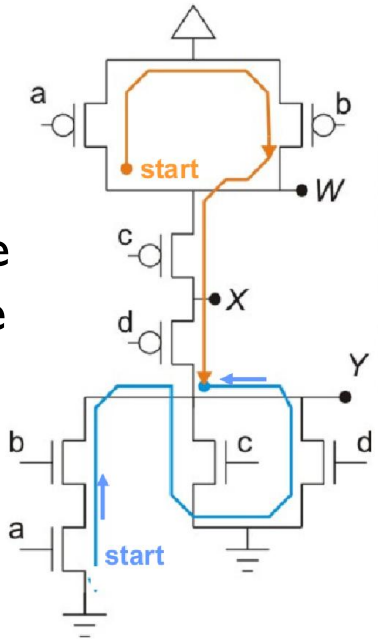


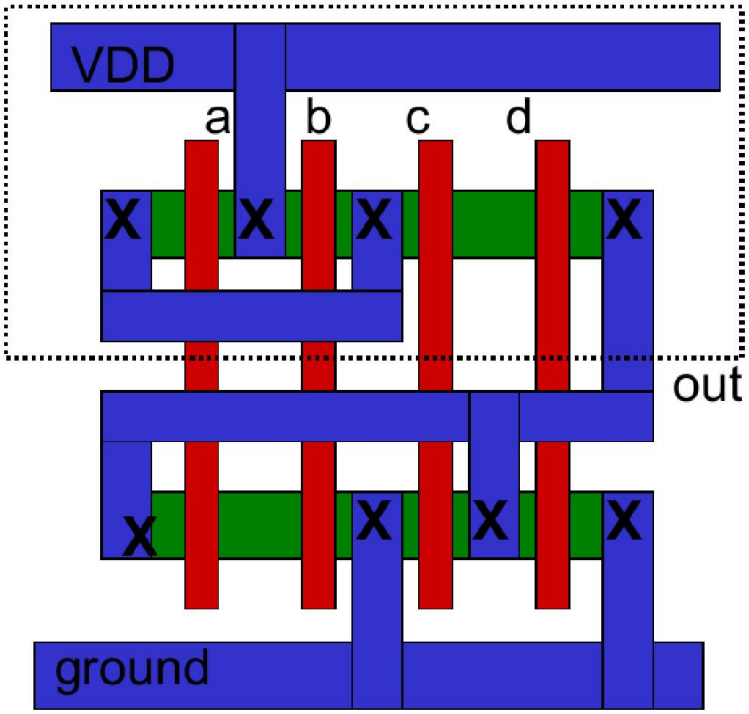


Example

- Circuit with pMOS and nMOS paths

Rule for single active strip: loop can not cross the same point/node more than twice
- pMOS through W twice
- nMOS through Y twice

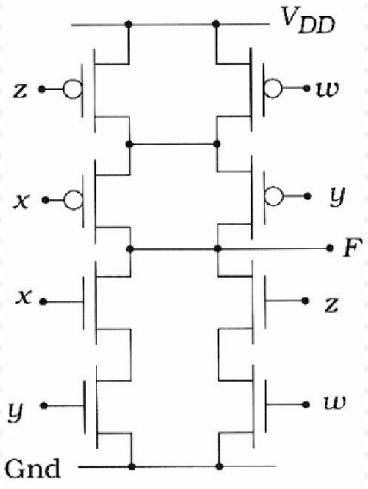




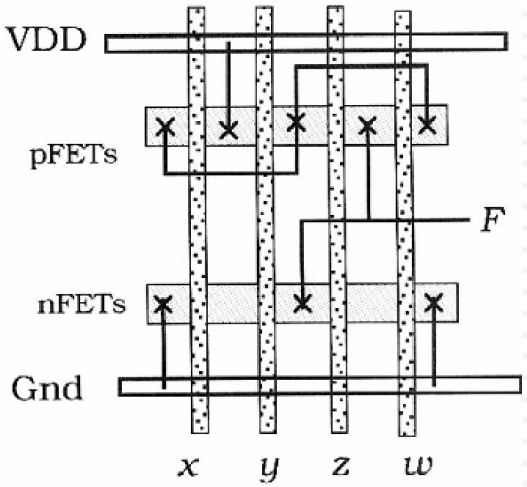
- Shows layout can be constructed with a single p/n active trace
- Order of txs (poly traces) is a,b, c, d, on both p- and n-side

Structured Layout

- General Approach
  - power rails
  - horizontal Active
  - vertical Poly (inputs from top/bottom)
  - Metal1 connects nodes as needed in schematic
- Structured Layout
  - AOI circuit figure
  - useful for many logic functions
  - see examples in textbook
- Disadvantages
  - not optimized for speed
  - large S/D regions = higher capacitance
  - interconnect paths could be shorter
- not optimized for area/size



(a) Circuit



(b) Layout wiring

Project Ideas

- Design and Characterization of a CMOS 8-bit Microprocessor Data Path (Group Project 3-4)
- Read the following papers and use Tanner EDA tools to design and verify the presented circuit
  - 4-Bit-Fast-Adder-Design-Topology-and-Layout-with-Self-Resetting-Logic-for-Low-Power-VLSI-Circuits
  - Optimal Design of A Reversible Full Adder
- Individual projects: Adders (Ripple-carry, carry-lookahead), Shifters (Barrel shifter), Multipliers, Mixed Elements (A/D and D/A circuits), Sequential circuits (Registers and shifters), Memory elements (SRAM, DRAM)
- Other proposals: must be approved before proceeding