Alexandria University
Faculty of Engineering
Division of Communications & Electronics

EE 432 VLSI Modeling and Design
Lab#2: Physical Design of MUX2:1 and XOR

Objectives

Upon the completion of this Lab, you should be able to:

1. Optimize the layout of complex, multi-transistor, logic gates.
2. Design cells to meet size objectives.
3. Identify and correct DRC and LVS errors.

Requirements

Lab 2 will expose students to the design of more complex logic gates where an optimized layout can be difficult to achieve. A 2:1 MUX and 2-input XOR with built-in input signal inverters will be developed.

You are required to draw an optimized layout of a 2:1 MUX and 2-input XOR gate with minimum transistor width on a MOSIS/Orbit n-well 2.0 micron process. Use Tspice to verify the functionality of the circuits through transient analysis (check all possible input/output combinations).

Note: Estiamted time to complete this assignment is 3 hours. You are required to develop either the Mux or the XOR gate in the Lab and develop the second gate as a homework and present it to the TA.

Procedure:

1. Create the schematic for a 2:1 multiplexer cell (MUX21) using pass transistor logic (transmission gate) with minimum-sized nMOS and pMOS transistors (L=2 lambda, W= 5 Lambda). See Figure 1 below and Chapter 2 notes. Include an inverter within this cell to invert the select signal. Create the inverter at the transistor level; do not instantiate an inverter cell into this schematic. You are not required to make a transmission gate cell, rather you can implement transmission gates with transistors directly within the MUX21 cell. The cell should have three inputs (e.g., a, b, s) and one output. When drawing the schematic, consider how the transistors might be arranged in the layout (step 3).
2. For this Lab the power and ground rails will be made 10 lambda wide using the Metal-1 layer and the standard cell pitch (height

from bottom of the GND rail to top of the VDD rail) will be 70 lambda.

3. Complete the cell layout for the 2:1 multiplexer and pass DRC and LVS. This cell must be designed as a primitive cell. Do not use Metal-2. You should optimize the size of the cell by minimizing the cell width. You should be able to get the width of this layout close to 40 lambda. Do not forget to provide contacts to the pMOS substrate and the n-well.
4. Pass DRC and LVS on the MUX21 cell and extract the spice file.
5. Use Tspice to verify the functionality of the circuit through simulations (check all possible input/output combinations).
6. Create a 2-input CMOS XOR (XOR2) gate.
7. Construct a width-minimized layout for a static CMOS XOR2. This cell must be designed as a primitive cell using only polygons. Do not use Metal-2. Minimize the width of this cell while keeping the standard 70 lambda cell pitch. This can be challenging, but a main purpose of this lab is to learn how to optimize the layout of cells with several transistors. A width of 56 lambda can be achieved following the basic primitive cell layout guidelines. Do not forget to provide contacts to the pMOS substrate and the n-well.

   HINTS: One way to layout XOR2 is to assume the A input comes from the left and the B input comes from the right, with the input inverters at the left and right side of the cell. Also, keep in mind that Source and Drain regions can be shared between transistors (even the inverter transistors – hint, hint!). When optimized, it is possible to have only one active region for the pMOS transistors and one active region for all the nMOS.
8. Pass DRC and LVS on the XOR2 cell and extract the spice file.
9. Use Tspice to verify the functionality of the circuit through simulations (check all possible input/output combinations).

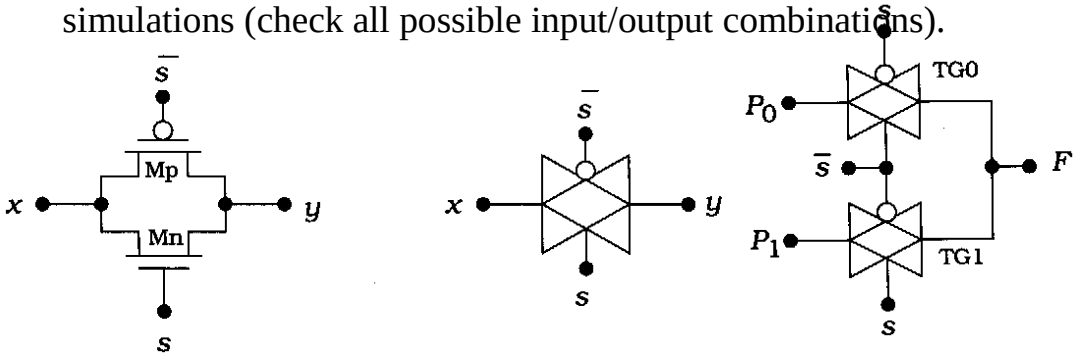

Fig. 1: (a) CMOS transmission gate, (b) transmission gate symbol, (c) 2:1 transmission-gate multiplexer, MUX21.