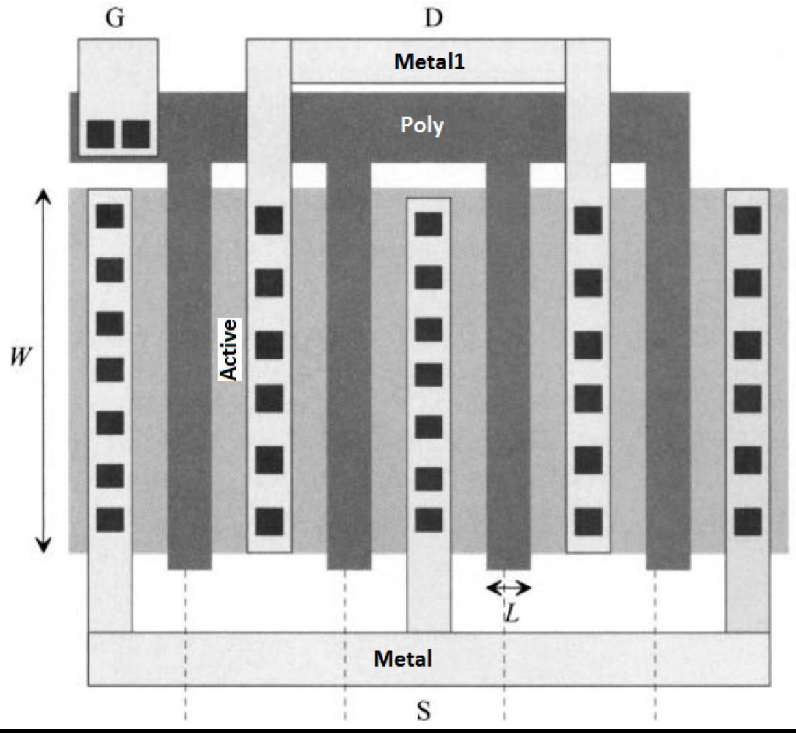
Alexandria University	جامعة الإسكندرية
Faculty of Engineering	كلية الهندسة
Electrical Engineering Department	قسم الهندسة الكهربية
Mid-term Exam, May 2014	امتحان نصف الفصل الدراسي الثاني (مايو ٢٠١٤)
Course Title and Code Number:	اسم المقرر والرقم الكودي له: نمذجة و تصميم
VLSI Modeling and Design (EE432)	الدوائر المتكاملة ذات الكثافة العالية جداً (EE432)
Fourth Year (Communications and Electronics)	السنة الدراسية الرابعة (اتصالات و الكترونيات)
Time Allowed: 1.5 Hrs	الزمن: ساعة ونصف

MOSIS Scalabale Design Rules Are Allowed

Answer Only Two Questions: **(25 marks)**

1. The following Figure shows an example of using the fingering strategy to layout MOSFETs with large aspect ratio. This strategy is used to get a square-shape layout. **(15 marks)**
   a. Draw a schematic representation of this layout and explain how it is equivalent to a MOSFET with large aspect ratio.
   b. Sketch the layout of a MOSFET with aspect ratio of 9 using the fingering strategy.
      - Attempt to keep the layout aspect ratio near to 1.
      - Minimize the layout area while respecting MOSIS design rules.
   c. The structure is to be fabricated in a scalable 1.2µm n-well CMOS process having the following parameters:
      - Gate-to-Channel capacitance =1.6 fF/µm^2, Metal1-to-Substrate capacitance=0.03 fF/µm^2, Metal1-to-Poly capacitance=0.05 fF/µm^2, and Polysilicon-to-Substrate capacitance=0.06 fF/µm^2.
      - Substrate sheet resistance=100 Ω, Active sheet resistance=10 Ω, Poly sheet resistance=4 Ω, Metal1 sheet resistance=2 Ω, and contact resistance=1 Ω.

   Draw the transistor equivalent circuit indicating approximate values of the resistors and capacitors. Assume that the substrate and source are connected to ground.



2. Consider the following logical function. **(15 marks)**

$$w_1 = \overline{a + b.c + d.e}\ , \qquad w_2 = \overline{f \oplus g}$$

$$result = \overline{w_1 \,.\, w_2 \,.\, h}$$

The inputs are *a, b, c, d, e, f, g,* and *h,* the output is *result,* and w_1 and w_2 are internal signals. Exclusive-OR is shown as $\oplus$.

a. Design a CMOS circuit realizing this function using the fewest number of transistors.

b. Is it possible to find an equivalent nFET and pFET Euler paths for individual circuits? If so, construct a colored stick diagram layout. If not, find a layout strategy and construct the corresponding stick diagram. You can use two-layer of metals if needed.
Follow these I/O constraints exactly:
1. Please make Vdd and GND run horizontally across the circuit in metal1.
2. Please make the inputs, a; b; c; d; e come from the left in metal1
3. Please make the inputs, f; g; h come from the right in metal 1
4. Please make the output ”result” exit to the right in metal 1
(Note: Please use an entire page for the stick diagram.)

c. Can you layout the *result* logical function in a smaller area? If so, explain without plotting how to do that.

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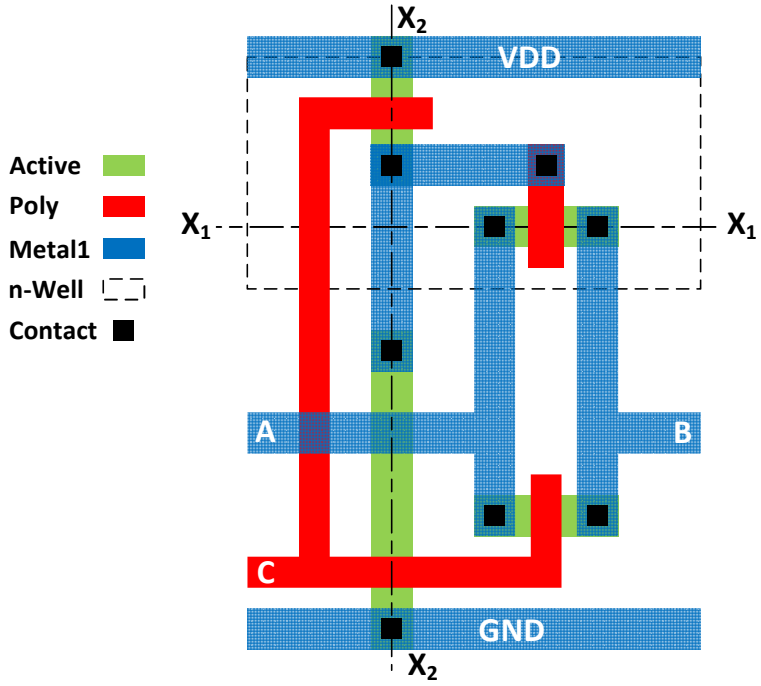
3. For the Layouts shown in the following Figure: **(10 marks)**

a. Draw the schematic representation and write the logical function equation.

b. Sketch the cross-sectional views of the layouts at the locations indicated.

c. Calculate the minimum cell height and width. Use MOSIS scalable design rules.



Good Luck

Examiner: ***Dr. Mohammed Morsy***