Alexandria University
Faculty of Engineering
Electrical Engineering Department
Mid-term Exam, April 2013

جامعة الإسكندرية
كلية الهندسة
قسم الهندسة الكهربية
امتحان الفصل الدراسي الثاني (ابريل ٢٠١٣)

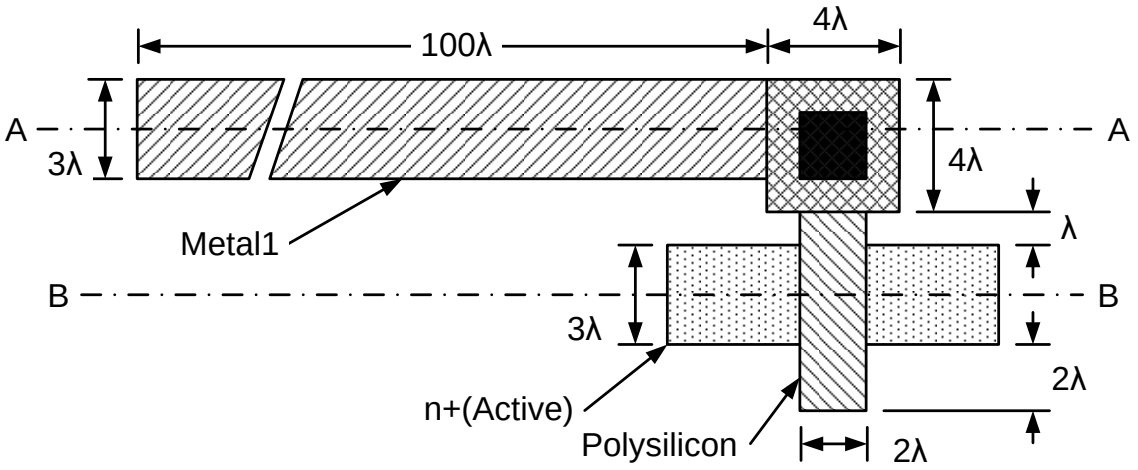
Course Title and Code Number:
VLSI Modeling and Design (EE432)
Fourth Year (Communications and Electronics)
Time Allowed: 1.5 Hrs

اسم المقرر والرقم الكودي له: نمذجة و تصميم
الدوائر المتكاملة ذات الكثافة العالية جداً (EE432)
السنة الدراسية الرابعة (اتصالات و الكترونيات)
الزمن: ساعة ونصف

MOSIS Scalabale Design Rules Are Allowed

Answer All Questions: **(25 marks)**

1. For the Layout shown below: **(5 marks)**
   a. What structure does it represent?
   b. The structure is to be fabricated in a scalable 1.2µm n-well CMOS process having the following parameters:
   λ=0.6 µm, Gate-to-Channel capacitance =1.6 fF/µm^2, Metal-to-Substrate capacitance=0.03 fF/µm^2, Polysilicon-to-Substrate capacitance=0.06 fF/µm^2 (f≡femto≡10^{-15}).
   Estimate the total capacitance associated with the structures as seen from Metal1 layer to ground. Note that the substrate is connected to ground.



2. In a scalable 0.5 µm CMOS process, it is intended to realize a resistor in a polysilicon layer. The process has the following parameters: **(5 marks)**
   λ=0.25 µm, Poly sheet resistance R_s=25Ω, Poly-to-Substrate capacitance = 0.12 fF/ µm^2.
   If the chip area allocated for the resistor is 10 µm x 10 µm,
   a. Layout the poly layer in this area in such a way that a maximum resistance is attained (use λ-based design rules).
   b. Calculate the maximum attainable resistance and the associated parasitic capacitance. Note that a straight-square has a resistance R_s while a corner-square has a resistance of 0.65R_s.
   c. Estimate the propagation delay time of such a structure.

Password: Snake

3. Consider the AOI logic function: **(7 marks)**

$$f = \overline{a.(b + c.(d + e))}$$

a. Design a CMOS circuit realizing this function using the fewest number of transistors.
b. Is it possible to find an equivalent nFET and pFET Euler paths for the circuit? If so, construct a colored stick diagram layout. If not, find a layout strategy and construct the corresponding stick diagram.
c. Determine the transistor sizes relative to βn and βp such that the logic circuit has approximately the same propagation delays as an inverter with βn = βp.

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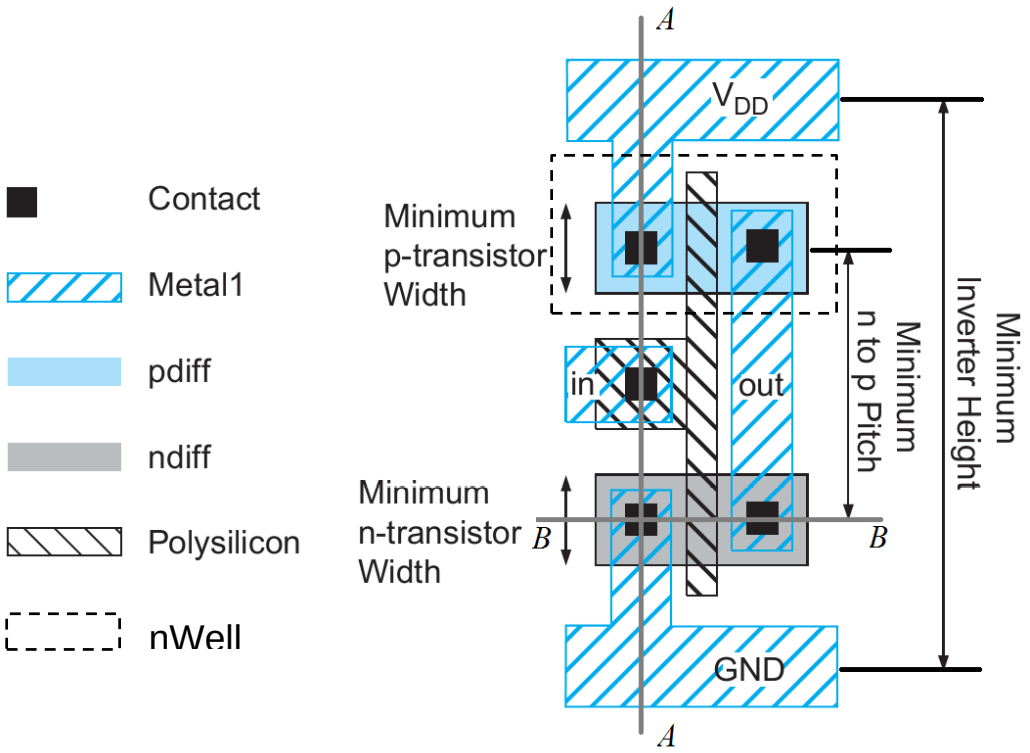
4. For the Layouts shown in Figure 3: **(8 marks)**
   a. Sketch the cross-sectional views of the layouts at the locations indicated.
   b. Calculate the minimum n to p pitch and the minimum inverter height with and without the poly contact to the gate (in). Use MOSIS scalable design rules.
   c. Briefly describe the physical limitations and potential problems associated with four design rules of different classes.



Good Luck

*Examiner**: Dr. Mohammed Morsy***