Alexandria University
Faculty of Engineering
Electrical Engineering Department
Final-Term Exam (Spring 2014)

جامعة الإسكندرية
كلية الهندسة
قسم الهندسة الكهربية
امتحان نهاية الفصل الدراسي (ربيع ٢٠١٤)

Course Title and Code Number:
VLSI Modeling and Design (EE432)
Fourth Year (Communications and Electronics)
Time Allowed: 3 Hrs

اسم المقرر والرقم الكودي له: نمذجة و تصميم
الدوائر المتكاملة ذات الكثافة العالية جداً (EE432)
السنة الدراسية الرابعة (اتصالات و الكترونيات)
الزمن: ٣ ساعات

MOSIS Scalabale Design Rules and Verilog Quick Reference Card Are Allowed

Answer All Questions: **(75 marks)**

Question One: **(15 marks)**

Figure 1 shows an example of using the fingering strategy to layout MOSFETs with large aspect ratio. This strategy is used to get a square-shape layout.

a. Draw a schematic representation of this layout and explain how it is equivalent to a MOSFET with large aspect ratio.
b. Sketch the layout of a MOSFET with aspect ratio of 16 using the fingering strategy.
   - Attempt to keep the layout aspect ratio near to 1.
   - Minimize the layout area while respecting MOSIS design rules.
c. Estimate the height and width for the layout you developed in (b) and compare them to those of the straight-forward layout of the same MOSFET.

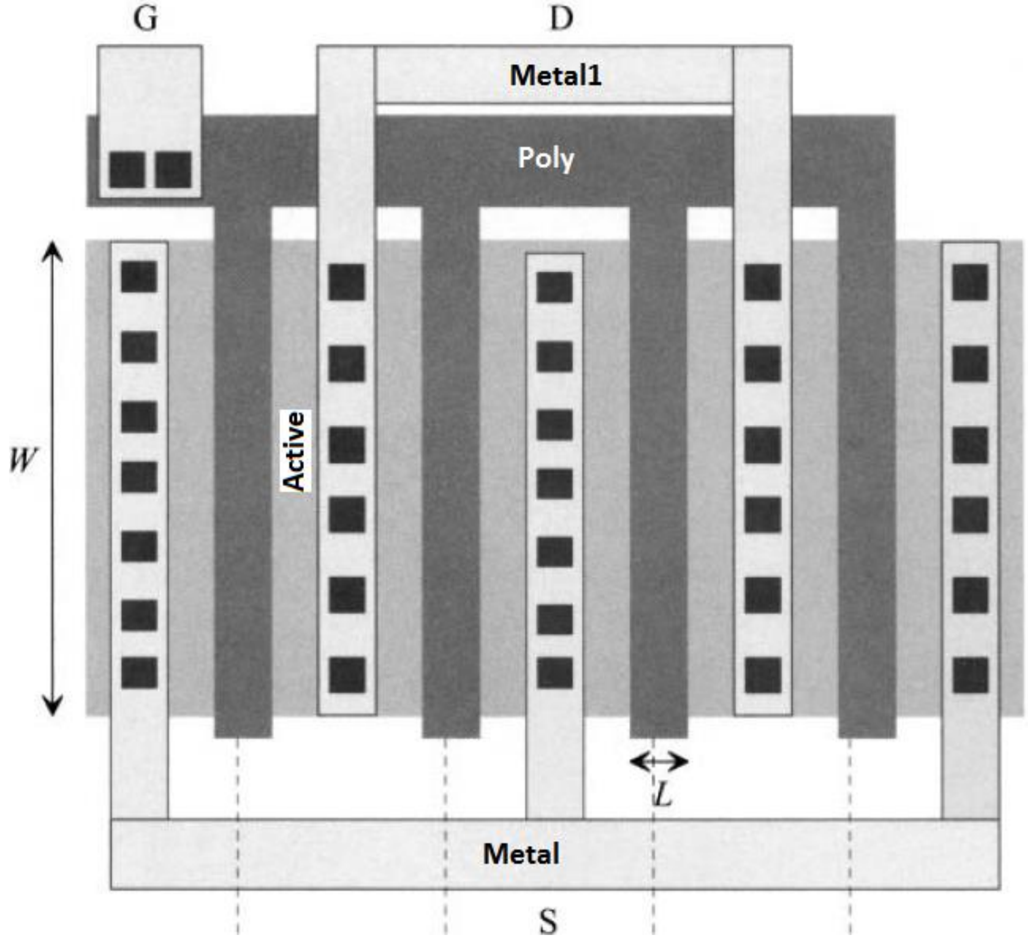


Figure 1: MOSFET layout

<u>Question Two:</u> **(15 marks)**

For the CMOS inverter shown in Figure 2:

a) Sketch the cross-sectional view of the inverter at the location indicated and estimate the height and width for the layout.

b) Sketch the set of masks used to fabricate the inverter ordered in the fabrication sequence.

c) Construct a table indicating each layer of the inverter and listing the fabrication processes used to create it.

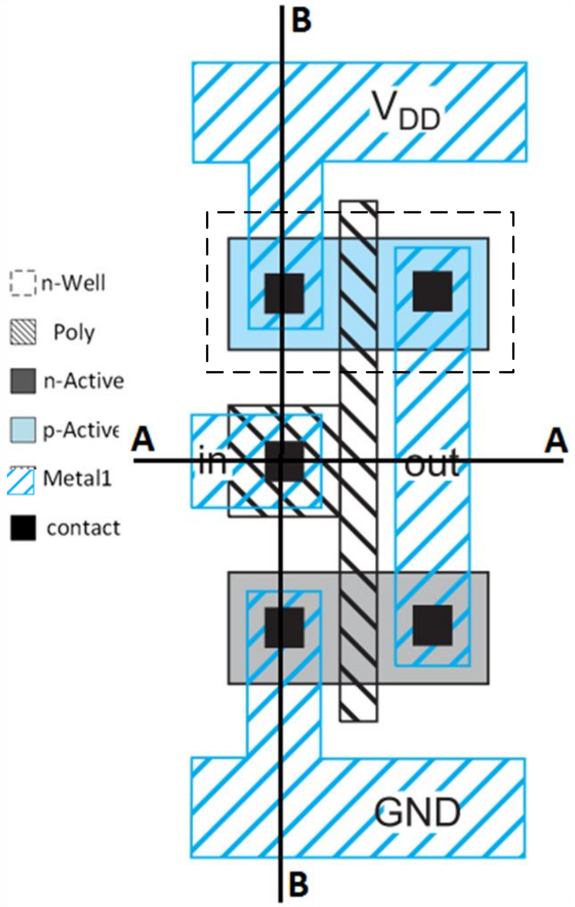


Figure 2: CMOS inverter layout

<u>Question Three:</u> **(15 marks)**

a) Write a Verilog description of an even parity checker with a 4-bit data input *d*, a single-bit parity output *parity*, and an active high *output_enable* input. Choose a proper modeling style (structural, data-flow, or behavioral) and operators to **minimize** the number of code lines.

b) Draw the schematic diagram of a CMOS circuit to be synthesized for the parity checker module you developed in (a). The synthesis objective is to **minimize** the circuit area. Assume that the synthesis tool is allowed to use combinational gates with 2,3, or 4 inputs.
Hint: The key to minimize area is transistor sizing.

c) Draw an **optimized** stick diagram for the parity checker schematic you developed in (b).

Question Four: (15 marks)

Write a Verilog description of the following:

a) A 4-to-1 multiplexer with a tri-state output and an active low *output_enable* input. The multiplexer is a combinational circuit having data inputs *d[3:0]* and a two-bit selector *s[1:0]*. Use case and if statements.

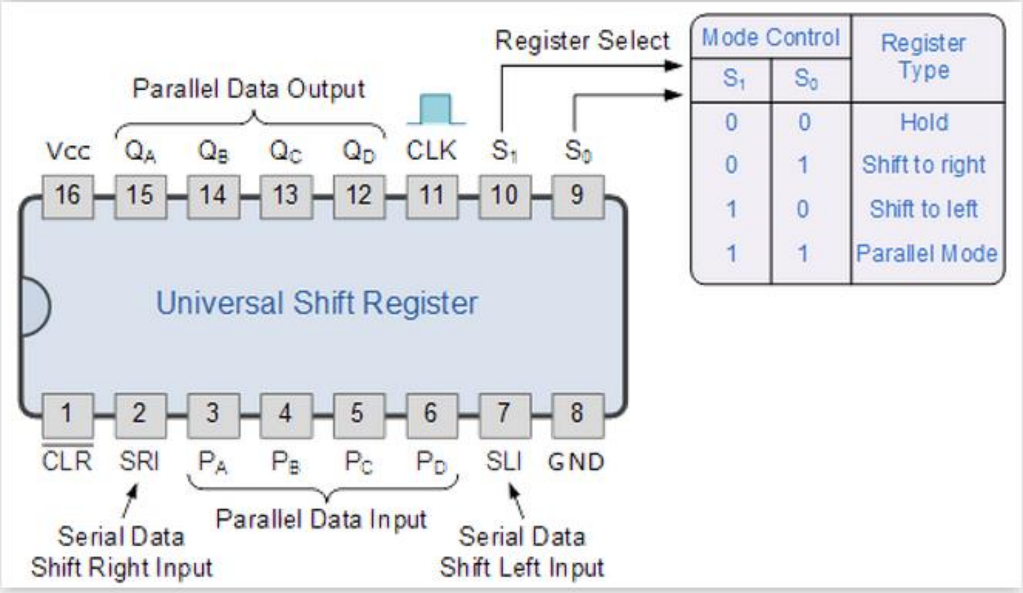
b) Use the 4-to-1 multiplexer you developed in (a) in a hierarchical fashion to build an 8-to-1 multiplexer. Write a Verilog testbench to **exhausitively** test the 8-to-1 multiplexer.

c) Use **only** a single instance of the 8-to-1 multiplexer you developed in (b) to build a 3-input XOR gate.

Hint: Use the multiplexer selectors as the gate inputs and force other multiplexer inputs to either '1' or '0' according to the gate truth table. This simple idea is the basis for building reconfigurable look-up tables (LUTs) used in FPGAs.

Question Five: (15 marks)

a) The universal shift register (USR) is a sequential logic circuit that can perform any combination of parallel and serial input to output operations but require additional inputs to specify desired function. Figure 3 shows the block diagram of a 4-bit USR circuit. The USR has four distinct modes of operation, namely: (i) Parallel (broadside) load, (ii) Shift right (in the direction Q_A toward Q_D), (iii) Shift left (in the direction Q_D toward Q_A), (iv) Hold clock (do nothing). Write a **parametric** Verilog code of an **n-bit** USR with a positive-edge clock and asynchronous clear. You are allowed to use any appropriate modeling style (structural, data-flow, or behavioral) or a combination of them to describe the USR. Also write a Verilog code of a testbench to test the developed USR at different modes of operation for a clock period of 10ns.



Mode Control		Register Type
S_1	S_0	
0	0	Hold
0	1	Shift to right
1	0	Shift to left
1	1	Parallel Mode

Figure 3: Block diagram and operating modes of a 4-bit universal shift register

b) Write a verilog procedural block to swap contents of two 8-bit registers using a temporary register. Rewrite the block to swap the two registers without using a temporary register. Declare the used registers.
Hint: Blocking Vs. Nonblocking assignments.

c) A simple sequential multiplier is developed by adding *A* to itself *B* number of times. Both *A* and *B* inputs are 4-bit unsigned numbers. The circuit has a *start* input that becomes 1 for one clock when the inputs are valid. The inputs will not be valid when this signal is 0. After the start, the circuit sets its *done* output to 0 and starts the multiplication process. When done, it puts the result on *r* and sets *done* to 1. Given the following interface, write the complete code of this multiplier.

```
module mult (a, b, start, clk, r, done);
input [3:0] a, b;
input start, clk;
output [7:0] r;
output done;
reg [3:0] abuf, bbuf; // use these if you like
reg [7:0] r;
. . .
endmodule
```

Good Luck

*Examiner**: Dr. Mohammed Morsy***