Alexandria University
Faculty of Engineering
Electrical Engineering Department
Final-Term Exam (Spring 2013)

جامعة الإسكندرية
كلية الهندسة
قسم الهندسة الكهربية
امتحان نهاية الفصل الدراسي (ربيع ٢٠١٣)

Course Title and Code Number:
VLSI Modeling and Design (EE432)
Fourth Year (Communications and Electronics)
Time Allowed: 3 Hrs

اسم المقرر والرقم الكودي له: نمذجة و تصميم
الدوائر المتكاملة ذات الكثافة العالية جداً (EE432)
السنة الدراسية الرابعة (اتصالات و الكترونيات)
الزمن: ٣ ساعات

MOSIS Scalabale Design Rules and Verilog Quick Reference Card Are Allowed

Answer All Questions: **(75 marks)**

Question One: **(15 marks)**

For the layout shown in Figure 1:

a) Extract the circuit schematic.

b) Write the output equation. What logic function does it represent?
Hint: Constuct the truth table of the circuit to realize its function.

c) Respecting the design rules, estimate the layout hight and width.

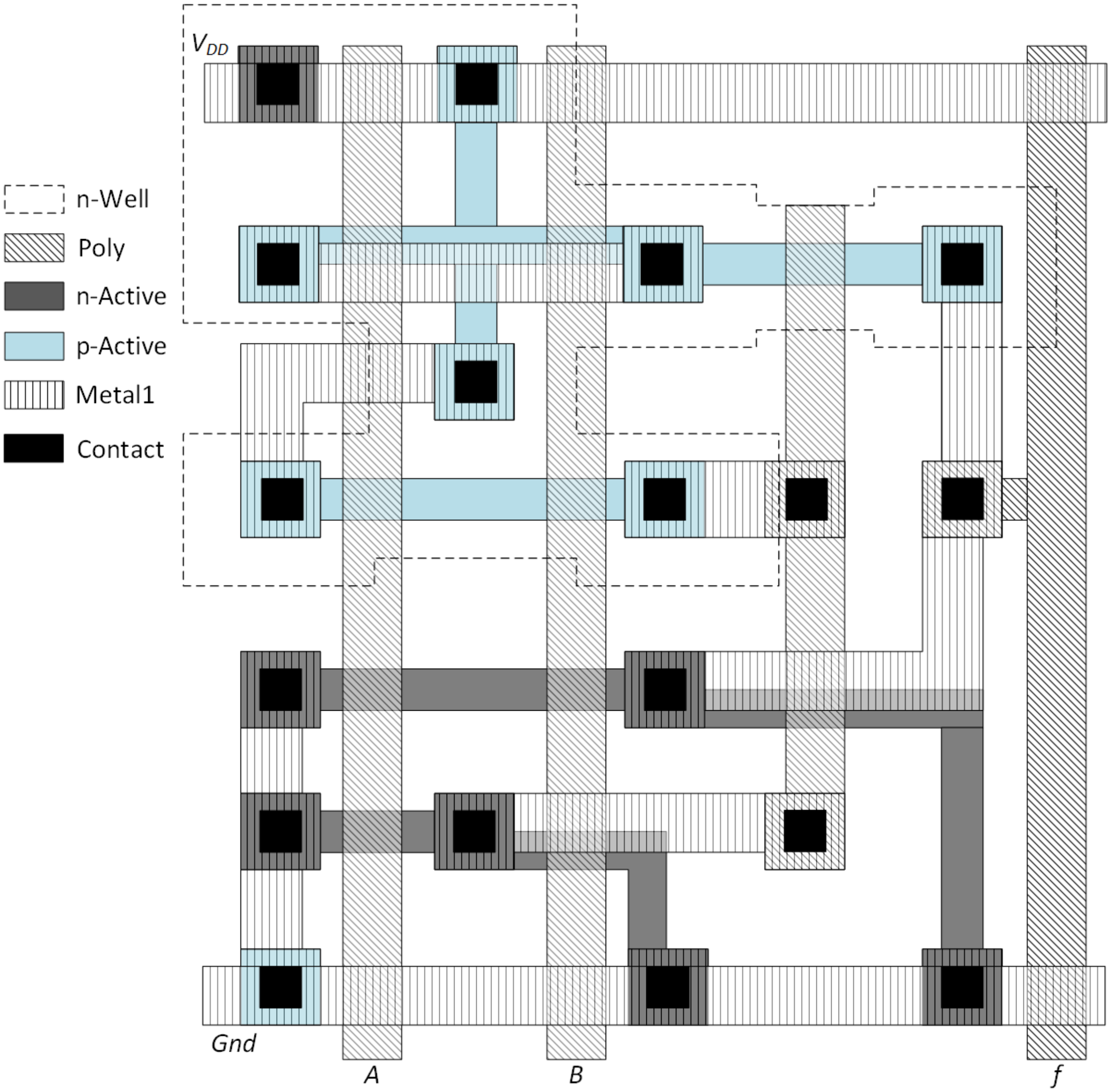

Figure 1: CMOS circuit layout

Question Two: (15 marks)

For the CMOS inverter shown in Figure 2:

a) Sketch the cross-sectional view of the inverter at the location indicated.

b) Sketch the set of masks used to fabricate the inverter ordered in the fabrication sequence.

c) Construct a table indicating each layer of the inverter and the fabrication processes used to create tit.

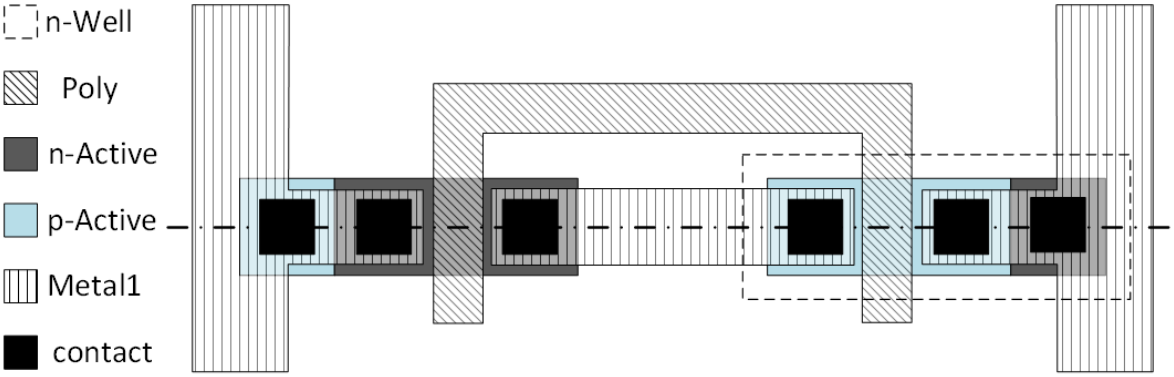

Figure 2: CMOS inverter layout

Question Three: (15 marks)

Write a Verilog description of the following:

a) A magnitude comparator that compares between two 4-bit inputs A and B and yields two outputs: A_GT_B and A_LT_B. Use continuous assignments to build the comparator.

b) Use the 4-bit comparator module developed in (a) in hierarchial fashion to build an 8-bit magnitude comparator that compares between two 8-bit inputs A and B and yields three outputs: A_GT_B, A_LT_B, and A_EQ_B. You can only use structural and dataflow modeling to build the comparator.

c) A testbench to functionaly verify the 8-bit comparator developed in (b).

Question Four: (15 marks)

a) Write a Verilog description of a 4-bit bidirectioanl counter module with asynchronous reset and synchronous load signal. Asserting the reset signal RST forces the output Q to 0 while asserting the load signal LD forces the output Q to the initial count D_IN. The following are the ports of the module:

CLK	1-bit clock input (synchronous actions performed on rising edge)
RST	1-bit reset (asynchronous reset)
UP_DOWN	1-bit input (if ‘1’, then count up, if ‘0’, then count down)
LD	1-bit load enable input, loads synchronized with CLK rising edge
D_IN	4-bit input data for loading counter value
Q	4-bit output

b) Write a verilog procedural block to swap contents of two 8-bit registers using a temporary register. Rewrite the block to swap the two registers without using a temporary register. Declare the used registers.
Hint: Blocking Vs. Nonblocking assignments.

c) Using case statement, design a 4-function ALU that has 4-bit inputs A and B and a 2-bit input select signal S, clock signal CLK, and a 5-bit output OUT. The ALU implements functions shown in Table based on the signal select. Ignore any overflow or underflow bits.

Select signal	Function
2’b00	OUT = A + B
2’b01	OUT = A - B
2’b10	OUT = A / B
2’b11	OUT = A % B

Question Five: (15 marks)

Figure 3 shows a 4-bit rotate-right network. The input bits are $a_3a_2a_1a_0$, and the output bits are $f_3f_2f_1f_0$. The network uses four bits Ror_0, Ror_1, Ror_2, and Ror_3 to specify an n-bit right rotation (n=0,1,2,3).

a) Modify the circuit to perform a shift-right operation that forces 0 into the empty space. Rename the control bits Ror_0 to 3 as Shr_0 to 3.

b) Construct a colored stick diagram for the shifter network, Make the horizontal interconnections in Metal-1 and the vertical interconnection in Metal-2.

c) Write a Verilog description of a parametric general shifter/rotator netwok as shown in Figure 4 .
The function of the combinational module is as follows: *f* = shift/rotate (*a*) to the right/left by (*s*) bits.
The following are the ports of the module:

a	n-bit input data, where n =2, 4, 8, …
f	n-bit output data
s	m-bit input representing the shift/rotation amount, where $m=\log_2(n)$
SH/RO	1-bit input specifying rotate or shif operation ('0' ≡ rotate and '1' ≡ shift)
R/L	1-bit input specifying right or left shift/rotation ('0' ≡ right and '1' ≡ left)

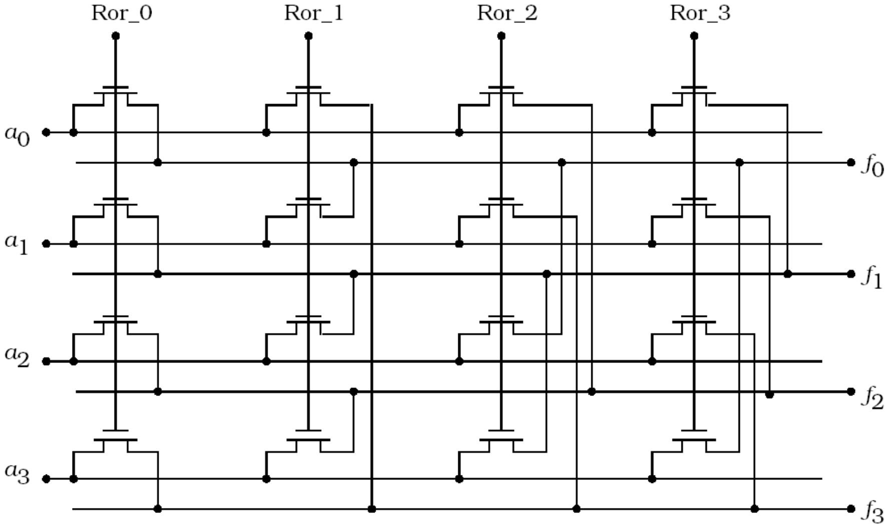

Figure 3: Rotate-right network

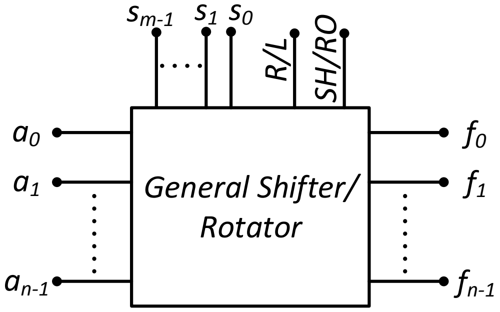

Figure 4: General shifter/rotator module

Good Luck

*Examiner: **Dr. Mohammed Morsy***