Alexandria University
Faculty of Engineering
Division of Communications & Electronics

EE431: Digital Integrated Circuits
Sheet 3: Layout of CMOS Circuits

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1. Draw the schematic for the CMOS circuit that implements the function F described by the truth table below. Use the least possible number of transistors. Explain your procedure and show the reduced function equation used to design the schematic.

Inputs			*Output*
X	**Y**	**Z**	**F**
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

2. Sketch a color-coded stick diagram for the circuit that implements the function $f = \overline{a + b.c + d}$. Organize the layout so that the transistors can be implemented on a continuous strip of active (i.e., do not break the active).

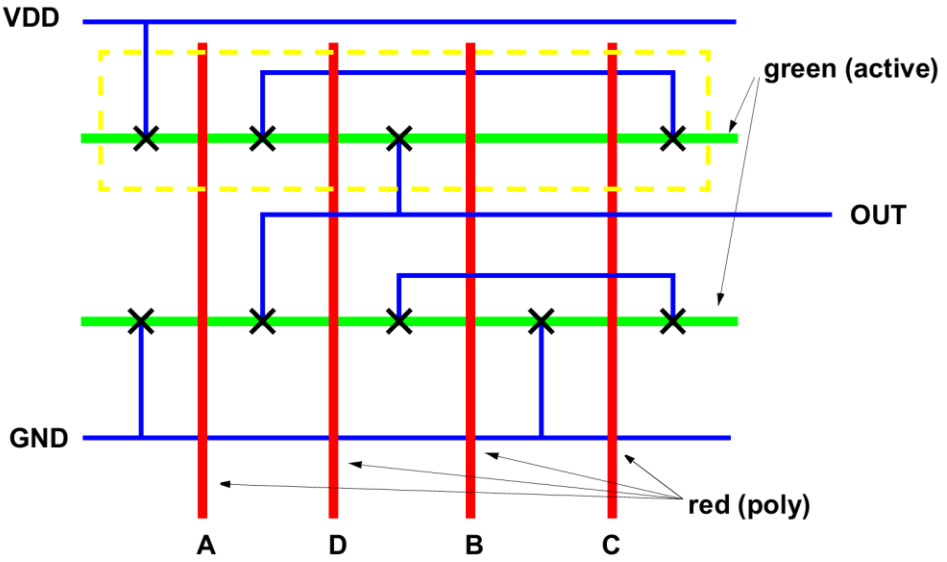
3. Design a CMOS circuit to implement the following function $f = \overline{x.(y.z + z.w)}$
   a. Construct the schematic for the circuit using the minimum number of transistors.
   b. Sketch the layout for this circuit using a stick diagram using colored pencils/pens/crayons. Show the Euler Path used for your stick diagram on your schematic. The stick diagram should include the active (green), poly (red), metal (blue), and contact (black X) layers and should be implemented between a power (VDD) and ground rail.

4.
   a. Draw the schematic for the circuit that implements $f = \overline{x.(y + z + w)}$
   b. Using an inverter with βn= βp, as a sizing reference, determine the size of each transistor in this circuit that will equalize the

nMOS and pMOS resistances. That is, specify size of each transistor (in terms of β) relative to βn or βp.

c. Draw the layout of the CMOS realization of the function *f* for the specified transistor sizes.

5. Consider the following stick diagram. Draw the transistor-level schematic. What logic equation does the circuit implement?



6. Draw a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata. What is the logic equation represented by the layout.