# Alexandria University
## Faculty of Engineering
*Electrical Engineering Department*


**EE431: Digital Integrated Circuits**
**Sheet 2: MOS Dynamic Characteristics**

1) Consider switching delays for 1 pF in a 10-kΩ resistive-load inverter circuit, where

$$\mu_n \cdot C_{ox} = 25\ \mu A/V^2$$
$$W/L = 10$$
$$V_{T0} = 1.0\ V$$

   a. Find $\tau_{PHL}$ (50% high-to-low transition delay) by using the average-current method. Assume that the input signal is an ideal rectangular pulse switching between 0 and 5 V with zero rise/fall times. You will have to calculate $V_{OL}$ to solve this problem.
   b. By using an appropriate differential equation and the proper initial voltage across the capacitor (when the input voltage is at $V_{OH}$) which is $V_{OL}$ and not 0 V, calculate $\tau_{PLH}$. Use the same input voltage as in part (a).

2) Consider a CMOS ring oscillator consisting of an odd number (*n*) of identical inverters connected in a ring configuration as shown in Figure 1. The layout of the ring oscillator is such that the interconnection (wiring) parasitics can be assumed to be zero. Therefore, the delay of each stage is the same and average delay is called intrinsic delay ($\tau_p$) as long as identical gates are used. The ring oscillator circuit is often used to quote the circuit speed of a particular technology using ring oscillator frequency (*f*).
   a. Derive an expression for the intrinsic delay ($\tau_p$) in terms of number of stages *n*.
   b. Show that ($\tau_p$) is independent of the transistor sizing (it remains the same when all gates are scaled uniformly up or down).

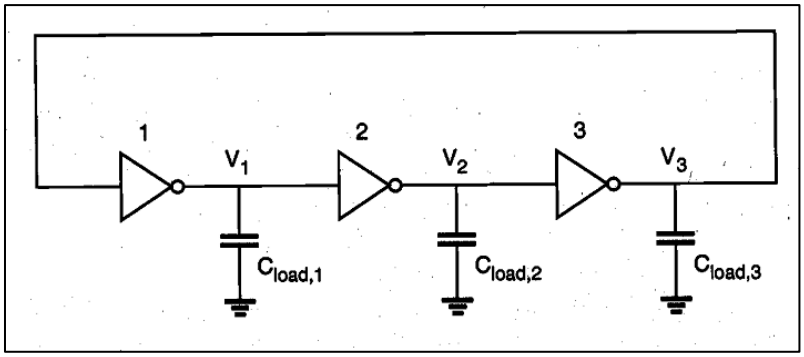


**Figure 1: ring oscillator**

3) Suppose that the resistive-load inverter examined in Exercise 1 is connected to a load capacitance of 1.0 pF which is initially discharged. The gate of the NMOS transistor is

driven by a rectangular pulse which changes from high to low at *t=0*. As a result, the nMOS transistor begins to charge up the capacitor. Solve the following two parts by using the differential equations and not by using the average-current methods.

a. Determine the 50% low-to-high delay time, which is defined as the time difference between 50% points of input and output waveforms when the output waveform switches from low to high.
b. Determine the 50% high-to-low delay time, which is defined as the time difference between 50% points of input and output waveforms when the output waveform switches from high to low when the capacitor is initially charged to 5.0 V.

4) A resistive-load inverter with $R_L=50\ k\Omega$ has the following device parameters:

$V_{TN}(V_{SB}=0) = 1.0$ V
$\gamma = 0.5\ V^{1/2}$
$t_{ox} = 0.05\ \mu m$
$\mu_n = 500\ cm^2/V{\cdot}s$
$W = 10\ \mu m$ and $L = 1.0\ \mu m$

A ring oscillator is formed by connecting nine identical inverters in a closed loop. We are interested in finding the resulting oscillation frequency.

a. Find the delay times of the inverter for an ideal step pulse whose voltage swing is between $V_{OL}$ and $V_{OH}$, i.e., $\tau_{PHL}$ and $\tau_{PLH}$. It should be noted that the loading capacitance of each inverter is strictly due to the drain parasitic capacitance and the gate capacitance of the following stage. For simplicity, neglect the drain parasitics and assume $C_{load}$ is equal to gate capacitance.
b. The rise and fall times are defined between. 10% and 90% of the full voltage swing. But for simplicity, we will assume that $\tau_{fall} = 2\ \tau_{PHL}$ and $\tau_{rise} = 2\ \tau_{PLH}$. Estimate the actual propagation delays $\tau_{PHL}$ and $\tau_{PLH}$ by using the rise and fall times of the inverter and the ideal delays found in (a).
c. Find the oscillation frequency from the information in part (b).

5) Consider a CMOS inverter, with the following device parameters:

*nMOS:* $V_{T0,n} = 0.8\ V$, $\mu_n C_{ox} = 50\ \mu A/V^2$
*pMOS:* $V_{T0,p} = -1.0\ V$, $\mu_p C_{ox} = 20\ \mu A/V^2$

The power supply voltage is $V_{DD}=5V$. Both transistors have a channel length of $L_n=L_p=1\mu m$. The total output load capacitance of this circuit is $C_{out}=2pF$, which is independent of transistor dimensions.

a. Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 2.2 V and the output rise time is $\tau_{rise} = 5$ ns.
b. Calculate the average propagation delay time $\tau_p$ for the circuit designed in (a).
c. How do the switching threshold $V_{th}$ and the delay times change if the power supply voltage is dropped from 5 V to 3.3 V. Provide an interpretation of the results.

6) Consider a CMOS inverter with the same process parameters as in Problem 3. The switching threshold is designed to be equal to 2.4 V. A simplified expression of the total output load capacitance is given as:

$$C_{out} = 500\ fF + C_{db,n} + C_{db,p}$$

Furthermore, we know that the drain-to-substrate parasitic capacitances of the NMOS and the PMOS transistors are functions of the channel width. A set of simplified capacitance expressions are given below.

$$C_{db,n} = 100\ fF + 9\ W_n$$
$$C_{db,P} = 80\ fF + 7\ W_p$$

Where $W_n$ and $W_p$ are expressed in µm.

a. Determine the channel width of both transistors such that the propagation delay $\tau_{pHL}$ is smaller than 0.825 ns.
b. Assume now that the CMOS inverter has been designed with $(W/L)_n = 6$ and $(W/L)_p = 15$, and that the total output load capacitance is 250 fF. Calculate the output rise time and fall time using the average current method.

7) Consider a CMOS inverter with the following parameters:

| | | | |
|---|---|---|---|
| *nMOS* | $V_{T0,n} = 1.0\ V$ | $\mu_n C_{ox} = 45\ \mu A/V^2$ | $(W/L)_n = 10$ |
| *pMOS* | $V_{T0,p} = -1.2\ V$ | $\mu_p C_{ox} = 25\ \mu A/V^2$ | $(W/L)_p = 20$ |

The power supply voltage is 5 V, and the output load capacitance is 1.5 pF.

a. Calculate the rise time and the fall time of the output signal using
   i. exact method (differential equations)
   ii. average current method
b. Determine the maximum frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0 V to 5 V in each cycle.
c. Calculate the dynamic power dissipation at this frequency.
d. Assume that the output load capacitance is mainly dominated by fixed fanout components (which are independent of $W_n$ and $W_p$). We want to re-design the inverter so that the propagation delay times are reduced by 25%.
   Determine the required channel dimensions of the NMOS and the PMOS transistors. How does this re-design influence the switching (inversion) threshold?