# CMOS Digital Integrated Circuits

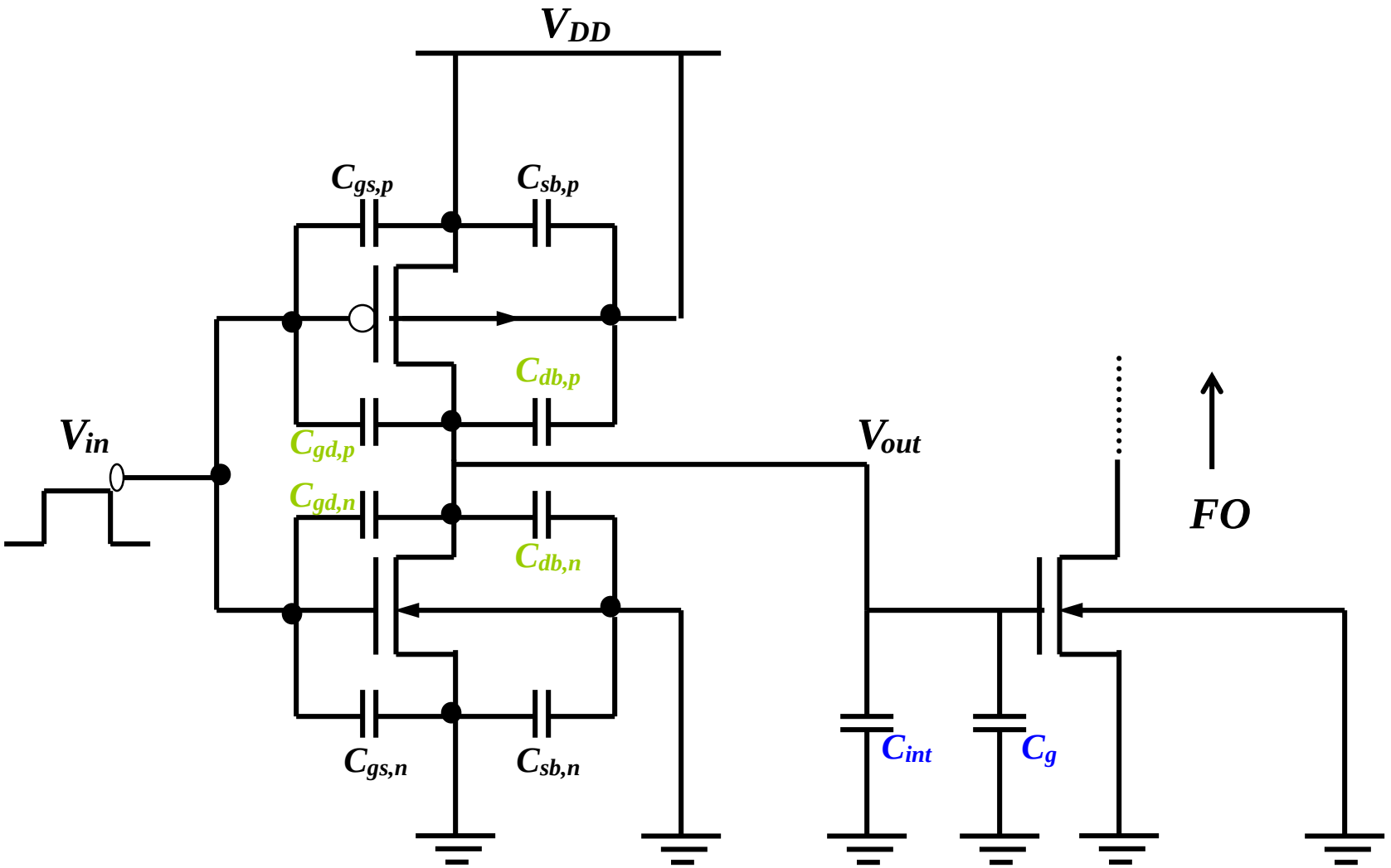
## Lec 7

## CMOS Inverters: Dynamic Analysis and Design

# CMOS Inverters – Dynamic Analysis and Design

- **Goals**
  - **Understand the detail dynamic analysis of the CMOS inverter.**
  - **Understand one set of design form CMOS equations.**
  - **Understand the basic CMOS design process using the CMOS static and CMOS design form dynamic equations.**

# CMOS Dynamic Analysis
# Capacitance Model for CMOS



# CMOS Dynamic Analysis
# Capacitance Model for CMOS

- The aggregate capacitance driven by the output node of a CMOS inverter is in detail working from left to right,
- $C_{load} = C_{input} + C_{int} + C_g$

  in which

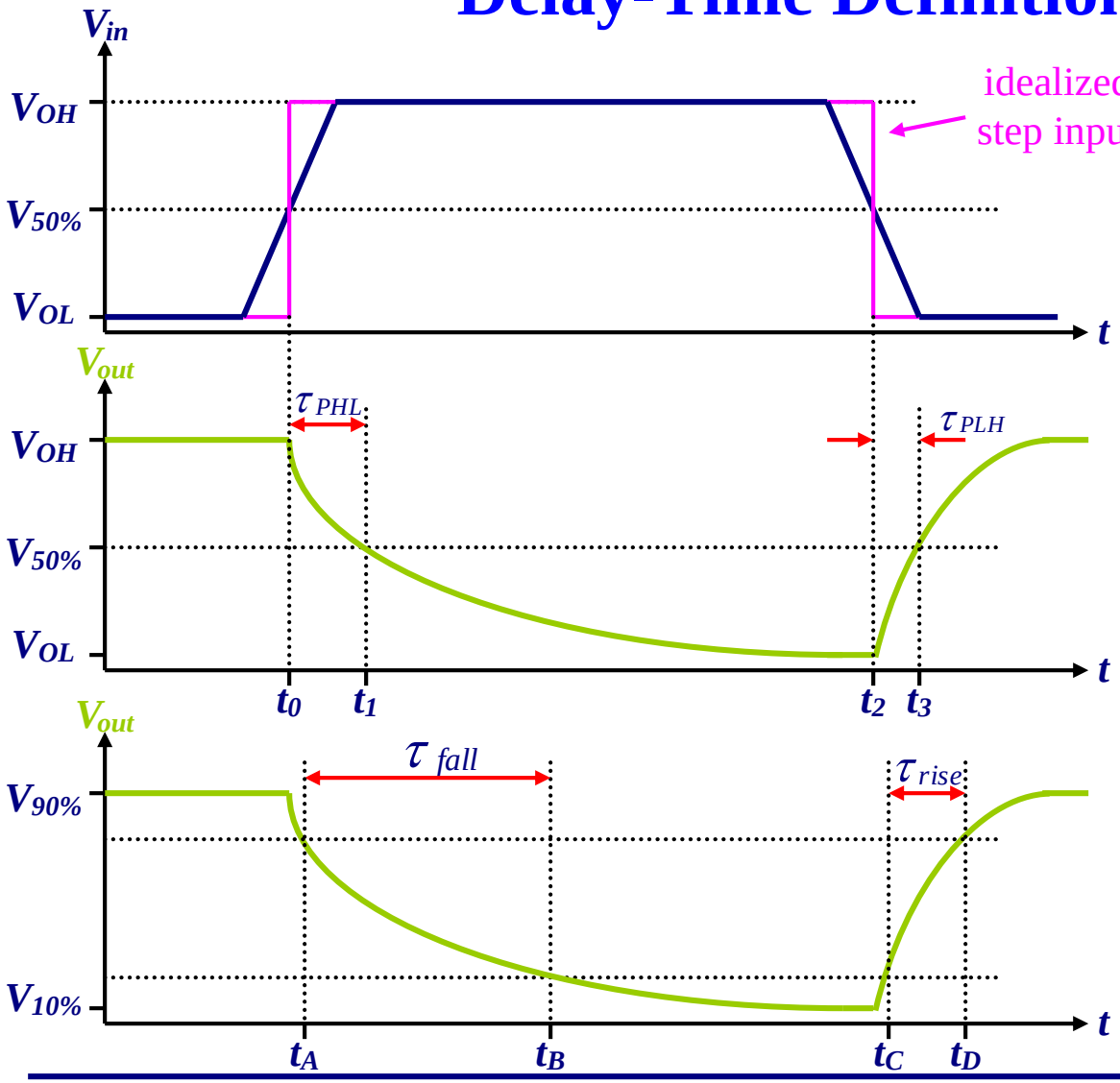
  $C_{input} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p}$ **(intrinsic component)**

  $C_{int}$ = interconnect capacitance

  $C_g$ = thin-oxide capacitance over the gate area

  } **(extrinsic component)**

# CMOS Dynamic Analysis
# Delay-Time Definitions




$V_{50\%} = V_{OL}+(V_{OH}-V_{OL})/2$

$= (V_{OH}+V_{OL})/2$

$\tau_{PHL} = t_1-t_0$

$\tau_{PLH} = t_3-t_2$

$\tau_P = (\tau_{PHL}+\tau_{PLH})/2$

$V_{10\%} = V_{OL}+0.1(V_{OH}-V_{OL})$

$V_{90\%} = V_{OL}+0.9(V_{OH}-V_{OL})$

$\tau_{fall} = t_B-t_A$

$\tau_{rise} = t_C-t_D$

# CMOS Dynamic Analysis
# Delay-Time Calculation (*First Order Estimates*)

- The simplest approach of calculating the propagation delay is based on estimating the *average capacitance current* during charge down/up.

$$\tau_{PHL} = \frac{C_{load}(V_{OH} - V_{50\%})}{I_{avg,HL}}$$

$$\tau_{PLH} = \frac{C_{load}(V_{50\%} - V_{OL})}{I_{avg,LH}}$$

where

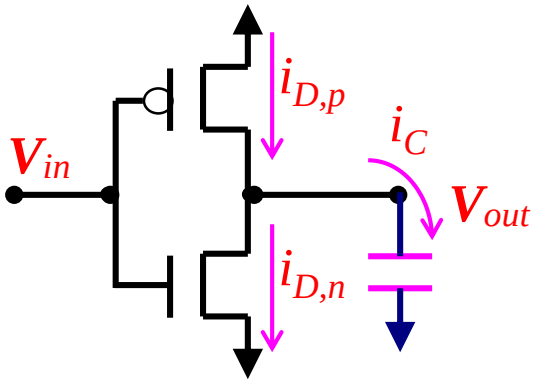
$$I_{avg,HL} = \frac{1}{2}\left[i_C(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_C(V_{in} = V_{OH}, V_{out} = V_{50\%})\right]$$

$$I_{avg,LH} = \frac{1}{2}\left[i_C(V_{in} = V_{OL}, V_{out} = V_{50\%}) + i_C(V_{in} = V_{OL}, V_{out} = V_{OL})\right]$$

# CMOS Dynamic Analysis
# Delay-Time Calculation (*More Accurate*)(1/4)

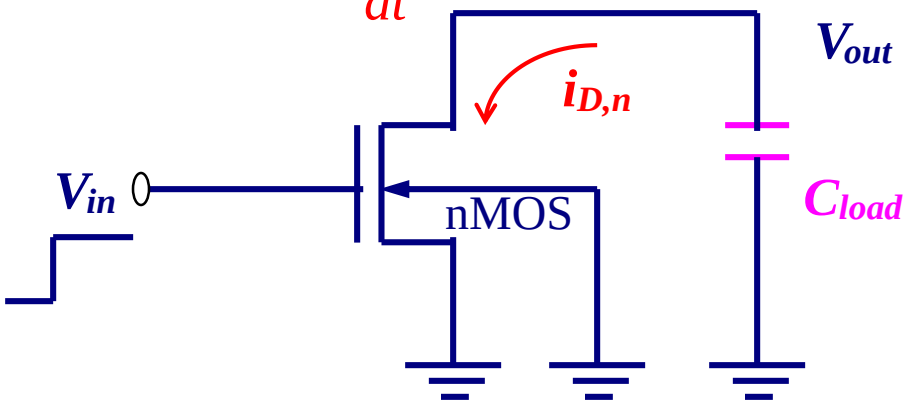
- The propagation delay can be found more accurately by solving the state equation of the output node. The current flowing through $C_{load}$ is a function $V_{out}$ as

$$C_{out}\frac{dV_{out}}{dt} = i_C = i_{D,p} - i_{D,n}$$



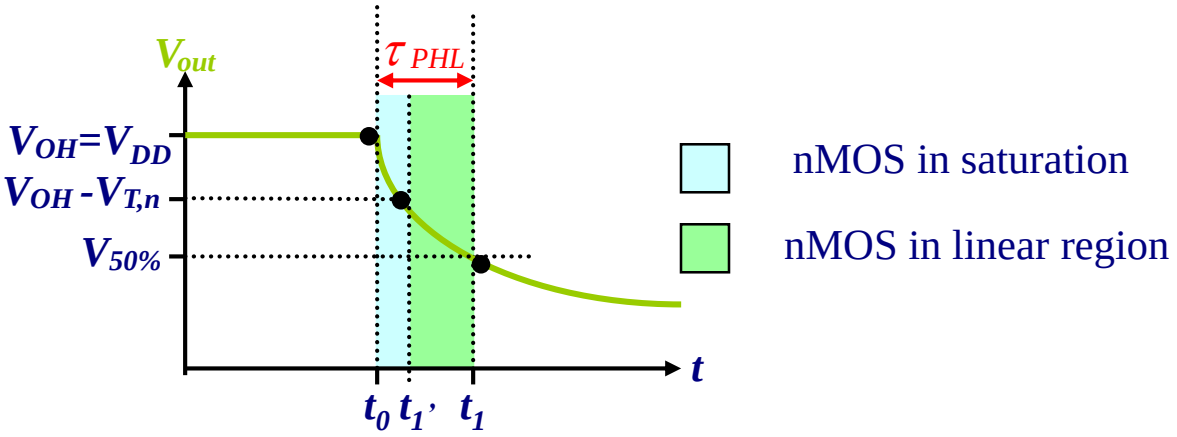

- $\tau_{PHL}$: PMOS is off. The equivalent circuit during high-to-low output transition is

$$C_{out}\frac{dV_{out}}{dt} = i_C = -i_{D,n}$$



# CMOS Dynamic Analysis
# Delay-Time Calculation (*2/4*)

The nMOS operates in two regions, ***saturation and linear***, during the interval of $\tau_{PHL}$.




- ***Saturation Region***

$$i_{D,n}=(k_n/2)(V_{in}-V_{T,n})^2=(k_n/2)(V_{OH}-V_{T,n})^2$$

» Plug $i_{D,n}$ into $C_{load}\,dV_{out}/dt=-i_{D,n}$, and integrate both sides, we get

$$t_1'-t_0 = 2C_{load}V_{T,n}/[k_n(V_{OH}-V_{T,n})^2]$$

# CMOS Dynamic Analysis
# Delay-Time Calculation (*3/4*)

- ***Linear Region***

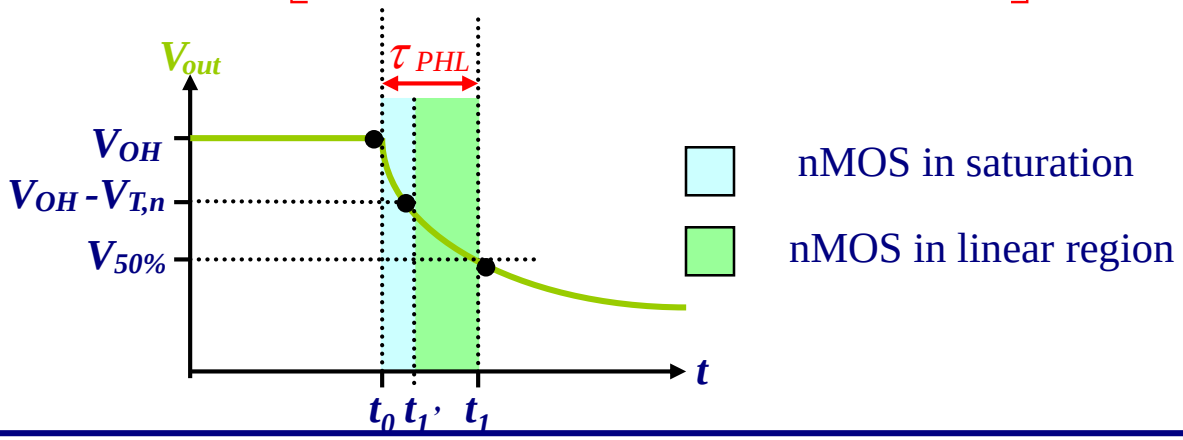
$$i_{D,n} = (k_n/2)[2(V_{in}-V_{T,n})V_{out}-V_{out}^2]$$
$$= (k_n/2)[2(V_{OH}-V_{T,n})V_{out}-V_{out}^2]$$

» Plug $i_{D,n}$ into $C_{load}\, dV_{out}/dt=-i_{D,n}$, and integrate both sides, we have

$$t_1 - t_1' = \frac{C_{load}}{\kappa_n (V_{DD}-V_{T,n})} \ln\left(\frac{4(V_{DD}-V_{T,n})}{V_{50\%}}\right)$$

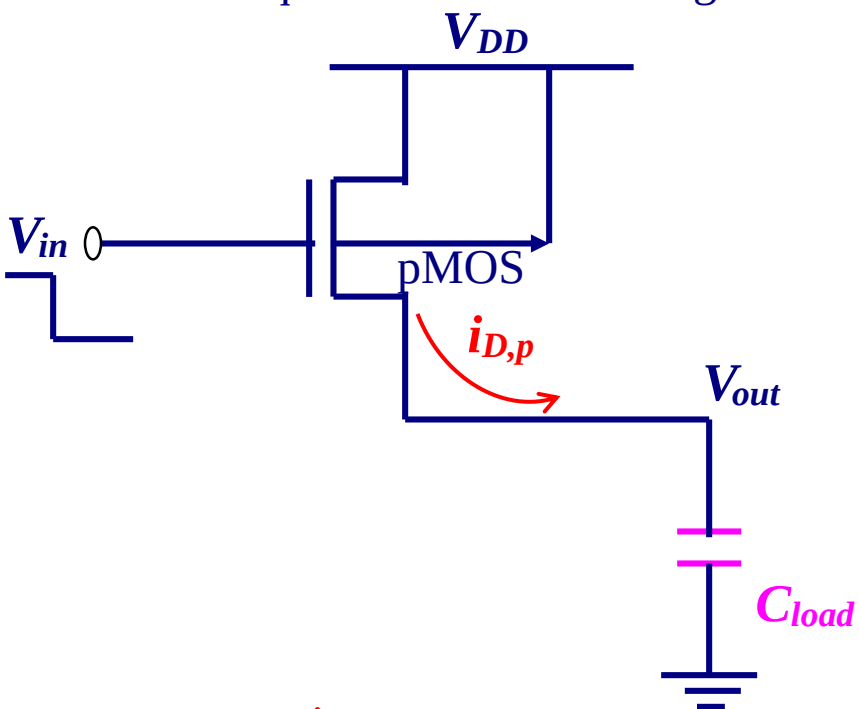
- Finally, since $V_{OH}=V_{DD}$ and $V_{OL}=0$, we have

$$\tau_{PHL} = \frac{C_{load}}{\kappa_n (V_{DD}-V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD}-V_{T,n}} + \ln\left(\frac{4(V_{DD}-V_{T,n})}{V_{DD}} - 1\right)\right]$$



# CMOS Dynamic Analysis
# Delay-Time Calculation (*4/4*)

- $\tau_{PLH}$: NMOS is off. The equivalent circuit during low-to-high output transition is




With the similar way ($t_0 \rightarrow t_1' \rightarrow t_1/0 \rightarrow |V_{T,p}| \rightarrow V_{50\%}$/*linear* $\rightarrow$*saturation*), we can have

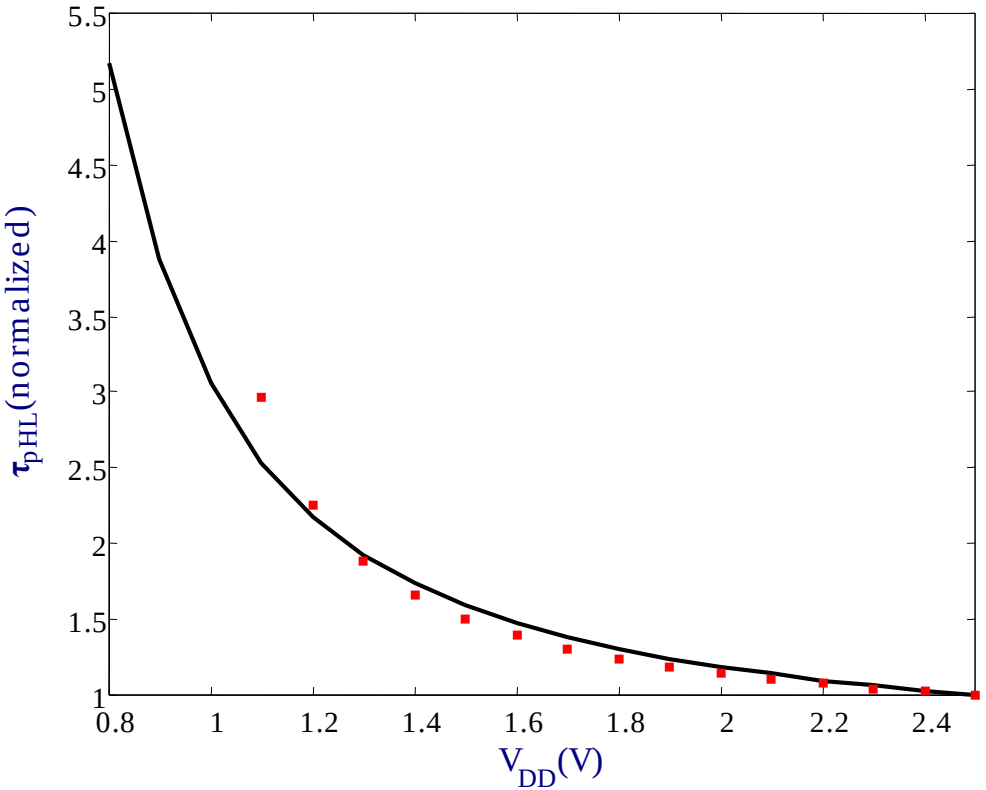
$$\tau_{PLH} = \frac{C_{load}}{\kappa_p (V_{DD} - |V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left( \frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

# CMOS Inverter Design

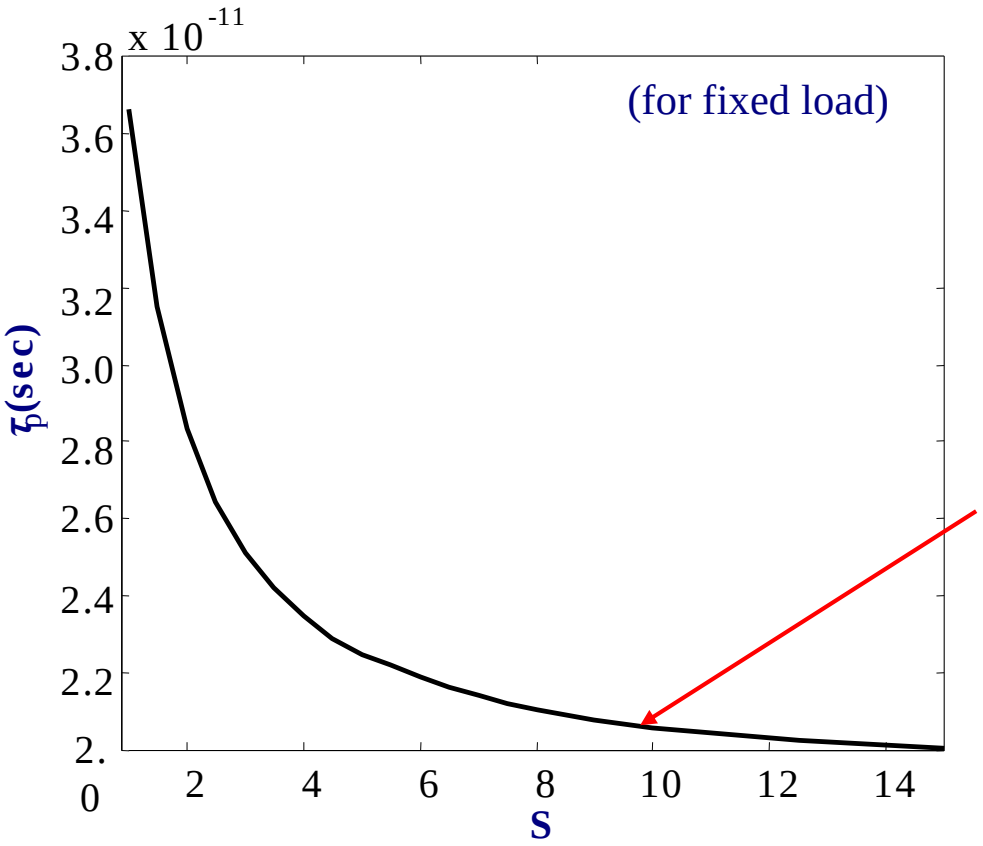
- Design for Performance
  - **Keep capacitance small**
  - **Increase transistor size**
    - » ***Watch out for self-loading!***
  - **Increase $V_{DD}$ (????)**

# CMOS Inverter Design
# Delay as a Function of $V_{DD}$

- $V_{DD}$ increases → $\tau_{PHL}/\tau_{PLH}$ decreases. However, the power consumption also increases.



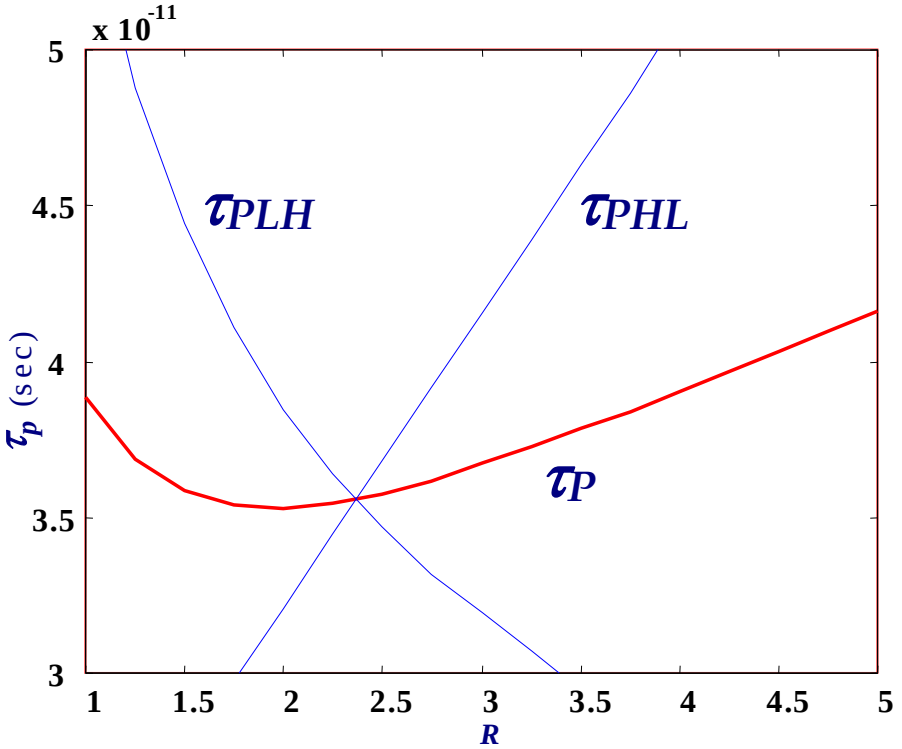
# CMOS Inverter Design
# Device Sizing (*1/5*)




Self-loading effect:
Intrinsic capacitances dominate

# CMOS Inverter Design
# Device Sizing (2/5)

- NMOS/PMOS Ratio




$$R = W_p / W_n$$

# CMOS Inverter Design
# Device Sizing (3/5)

## Self-Loading Effect

$$C_{load} = C_{gd,n}(W_n) + C_{gd,p}(W_p) + C_{db,n}(W_n) + C_{db,p}(W_p) + C_{int} + C_g$$
$$= f(W_n, W_p)$$

- Using the junction capacitance expressions in Chapter 3, we have

$$C_{db,n} = (W_n D_{drain} + x_j D_{drain}) C_{j0,n} K_{eq,n} + (W_n + 2D_{drain}) C_{jsw,n} K_{eq,n}$$
$$C_{dp,n} = (W_p D_{drain} + x_j D_{drain}) C_{j0,p} K_{eq,p} + (Wp + 2D_{drain}) C_{jsw,p} K_{eq,p}$$

- Therefore, $C_{load}$ can be rewritten as

$$C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$$

where

$$\alpha_0 = D_{drain}(2C_{jsw,n}K_{eq,n} + 2C_{jsw,p}K_{eq,p} + x_j C_{j0,n} K_{eq,n} + x_j C_{j0,p} K_{eq,p}) + C_{int} + C_g$$
$$\alpha_n = K_{eq,n}(C_{j0,n} D_{drain} + C_{jsw,n})$$
$$\alpha_p = K_{eq,p}(C_{j0,p} D_{drain} + C_{jsw,p})$$

# CMOS Inverter Design
# Device Sizing (*4/5*)

- Therefore, $\tau_{PHL}$ and $\tau_{PLH}$ are

$$\tau_{PHL} = \left(\frac{\alpha_0 + \alpha_n W_n + \alpha_p W_p}{W_n}\right) \times \left(\frac{L_n}{\mu_n C_{ox}\left(V_{DD} - V_{T,n}\right)}\right) \times \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \left(\frac{\alpha_0 + \alpha_n W_n + \alpha_p W_p}{W_p}\right) \times \left(\frac{L_p}{\mu_n C_{ox}\left(V_{DD} - |V_{T,p}|\right)}\right) \times \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

- The ratio between the channel widths $W_n$ and $W_p$ is usually dictated by other design constraints such as noise margins and the logic inversion threshold. Let's this transistor *aspect ratio* be defined as $R \equiv W_p/W_n$. Then, the propagation delay can be represented as

$$\tau_{PHL} = \Gamma_n \left(\frac{\alpha_0 + (\alpha_n + R\alpha_p)W_n}{W_n}\right)$$

$$\tau_{PLH} = \Gamma_p \left(\frac{\alpha_0 + (\frac{\alpha_n}{R} + \alpha_p)W_p}{W_p}\right)$$

# CMOS Inverter Design
# Device Sizing (*5/5*)

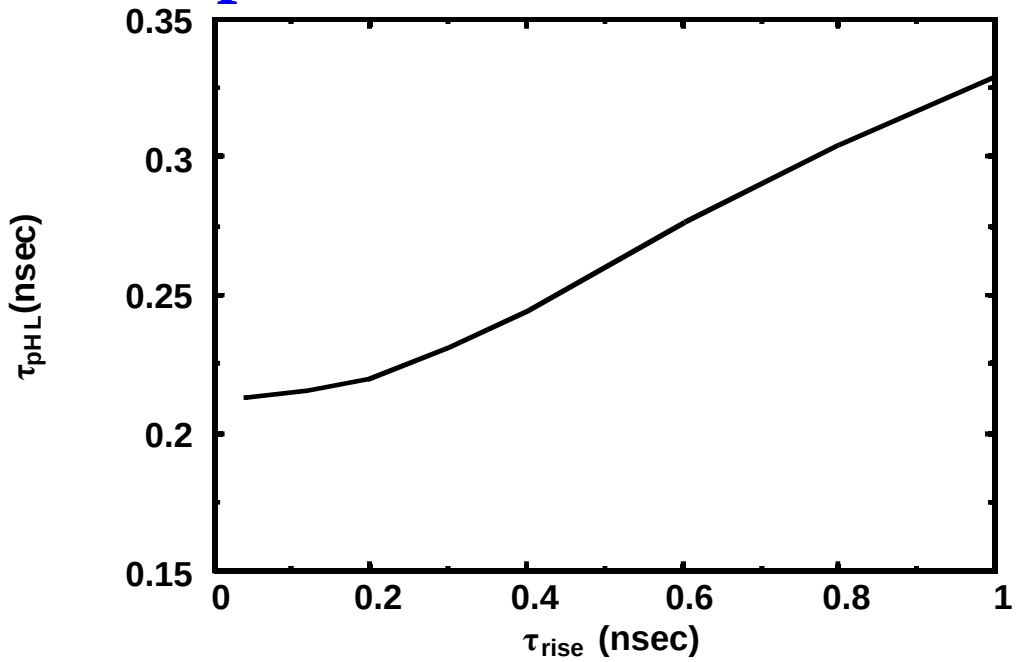
- As we continue increase the values of $W_n$ and $W_p$, the propagation delay will asymptotically approach a limit value for lager $W_n$ and $W_p$,

$$\tau_{PHL}^{limit} = \Gamma_n(\alpha_n + R\alpha_p)$$

$$\tau_{PLH}^{limit} = \Gamma_p(\frac{\alpha_n}{R} + \alpha_p)$$

- The propagation delay times cannot be reduced beyond the above limits, and the limit is *independent* of the extrinsic capacitances.

# CMOS Inverter Design
# Impact of Rise Time on Delay




$$\tau_{PHL} = \sqrt{\tau_{PHL(\text{step input})}^2 + \left(\frac{\tau_r}{2}\right)^2}$$

$$\tau_{PLH} = \sqrt{\tau_{PLH(\text{step input})}^2 + \left(\frac{\tau_f}{2}\right)^2}$$

Propagation delay increases since both PMOS and NMOS are on during the charge-up and charge-down events.

# CMOS Inverter Design
# Impact of Channel Velocity Saturation

- The drain current is *linearly dependent on* $V_{GS}$

$$I_{sat} = \kappa W_n (V_{GS}-V_T)$$

- Propagation delay only has a weak dependence on the supply voltage $V_{DD}$

$$\tau_{PHL} \approx \frac{C_{load} V_{50\%}}{I_{sat}} = \frac{C_{load}(V_{DD}/2)}{\kappa W_n (V_{DD} - V_T)}$$

# CMOS Dynamic Analysis
# Dynamic Power Dissipation (*1/2*)

- The dynamic power dissipation can be derived as follows.

$$P_{dyn,avg} = V_{DD}\, I_{DD,avg}$$

- With $I_{DD,avg}$ taken over one clock period $T$. The capacitance current which equals the current from the power supply (assuming $I_{Dn} = 0$ during charging) is

$$I_D = C_{load}\frac{dV_{out}}{dt}$$

- Rearranging and integrating over one clock period $T$

$$\int_0^T I_D\, dt = \int_0^{V_{DD}} C_{load}\, dV_{out}$$

- Gives

$$I_{DD,avg}\, T = C_{load}\, V_{DD}$$

# CMOS Dynamic Analysis
# Dynamic Power Dissipation (*2/2*)

- Solving for $I_{DD,avg}$ and substituting in $P_{avg}$:

$$P_{avg} = \frac{1}{T} C_{load} V_{DD}^2 = C_{load} V_{DD}^2 f$$

- It should be noted here the our simple $C_{load}$ may underestimate the power dissipated.
- In terms of SPICE simulation, the authors' offer a circuit called power meter.