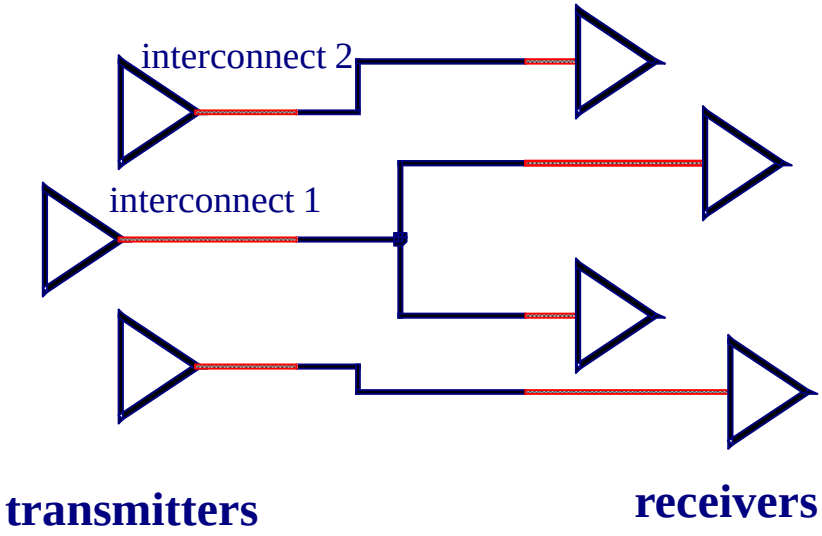
CMOS Digital Integrated Circuits

Chapter6:
Interconnect Analysis

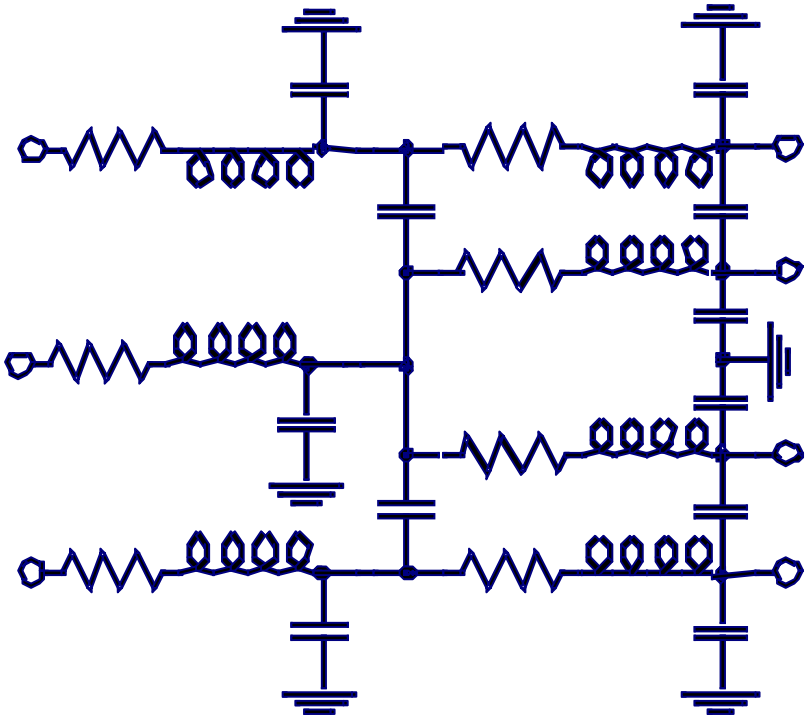
Interconnect Analysis
The Wire



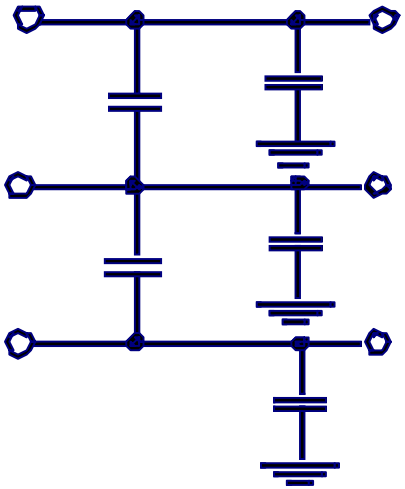
Schematics

Physical

Interconnect Analysis
Wire Models



All-inclusive model



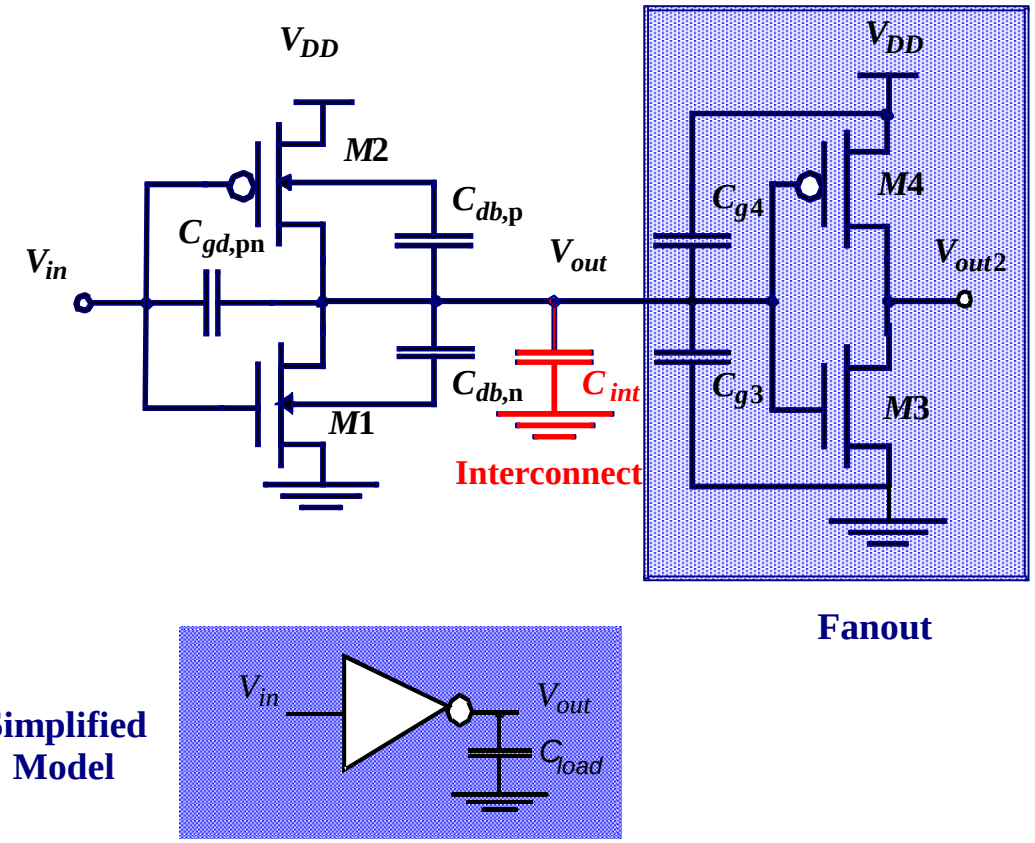
Capacitance-only

Interconnect Analysis
Impact of Interconnect Parasitics

- **Interconnect parasitics**
  - Reduce reliability
  - Affect performance and power consumption
- **Classes of parasitics**
  - Capacitive
  - Resistive
  - Inductive

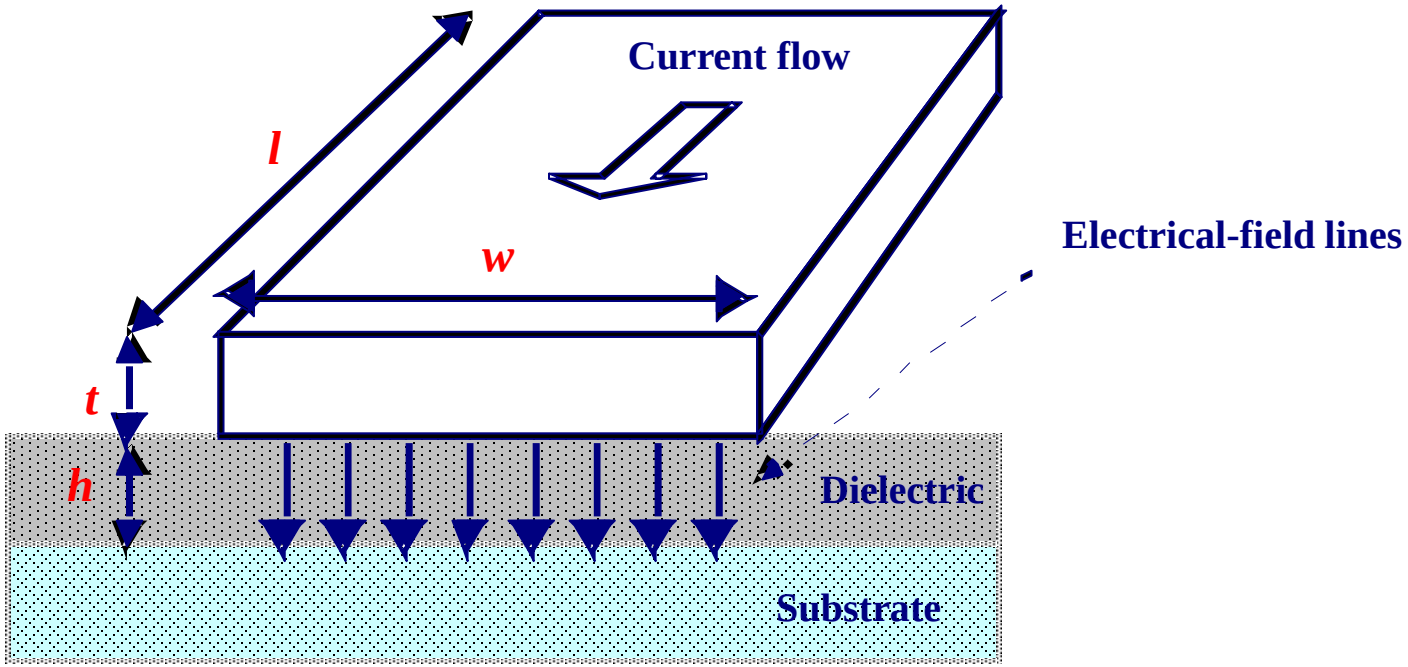
Interconnect Analysis
Capacitance (*1/8*)

- Capacitance of Wire Interconnect



Interconnect Analysis
Capacitance (*2/8*)

- The Parallel Plate Capacitance



$$C_{pp} = \frac{\varepsilon_{di}}{h} wl$$

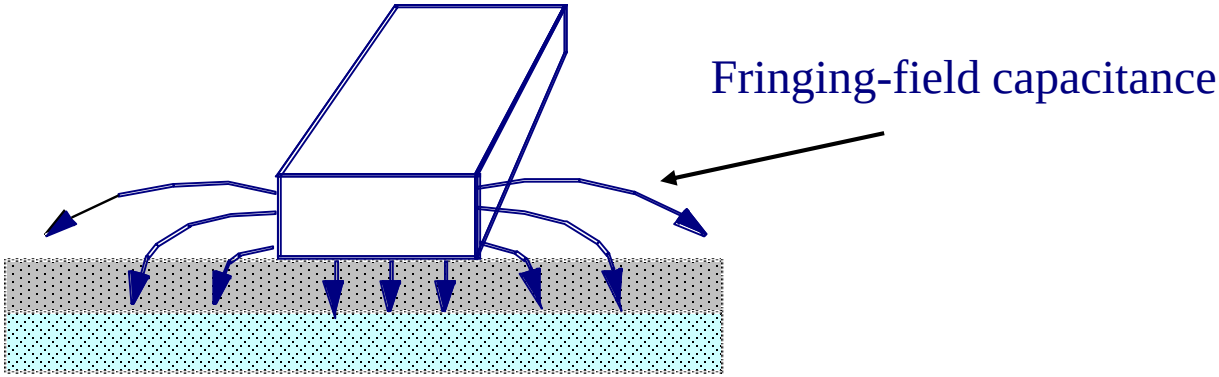
Interconnect Analysis
Capacitance (*3/8*)

- Permittivity

Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Interconnect Analysis
Capacitance (*4/8*)

- Fringing Capacitance

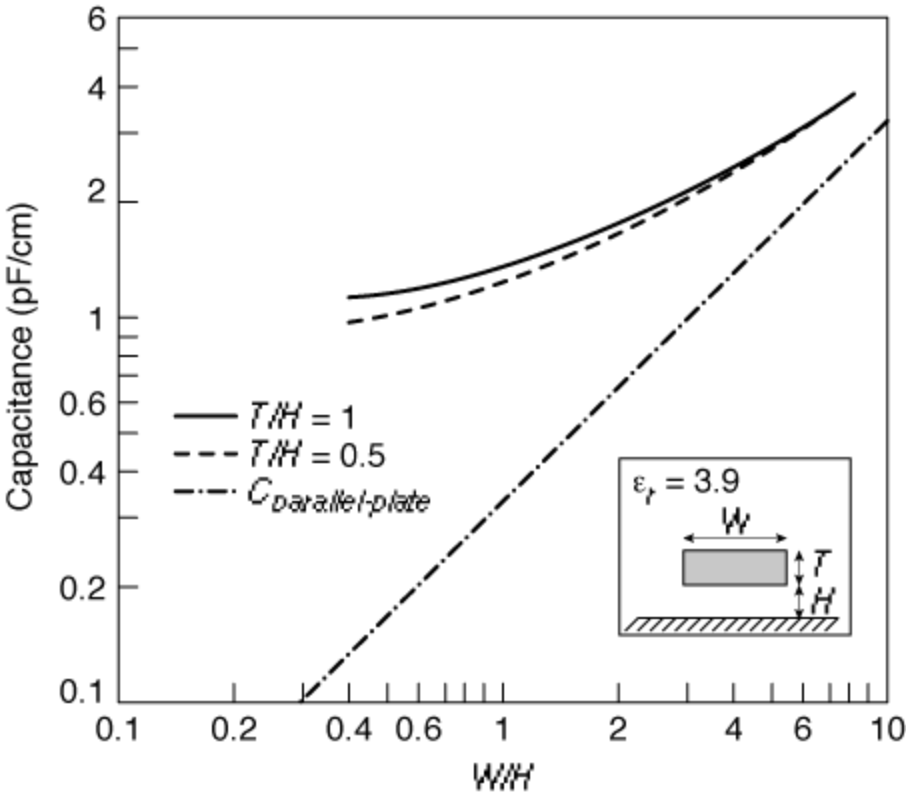


$$c_{wire} = c_{pp} + c_{fringe} = \left[\frac{w - t/2}{h} + \frac{2\pi}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} \right] \quad \text{for } w \geq \frac{t}{2}$$

$$c_{wire} = c_{pp} + c_{fringe} = \left[\frac{w}{h} + \frac{\pi(1 - 0.0543t/2h)}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} + 1.47 \right] \quad \text{for } w < \frac{t}{2}$$

Interconnect Analysis
Capacitance (*5/8*)

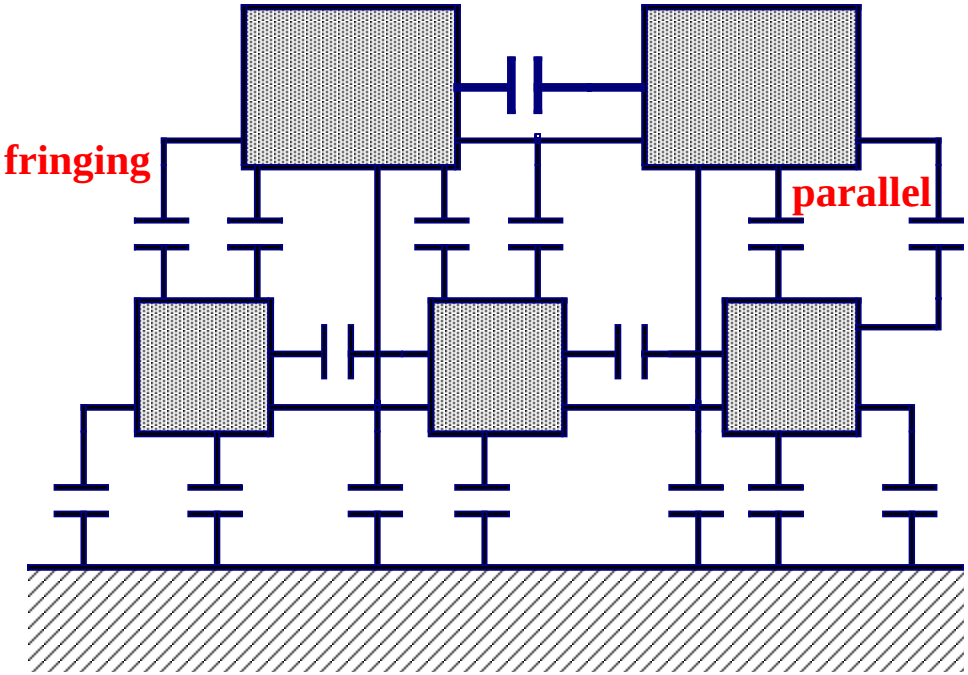
- Fringing versus Parallel Plate



(from [Bakoglu89])

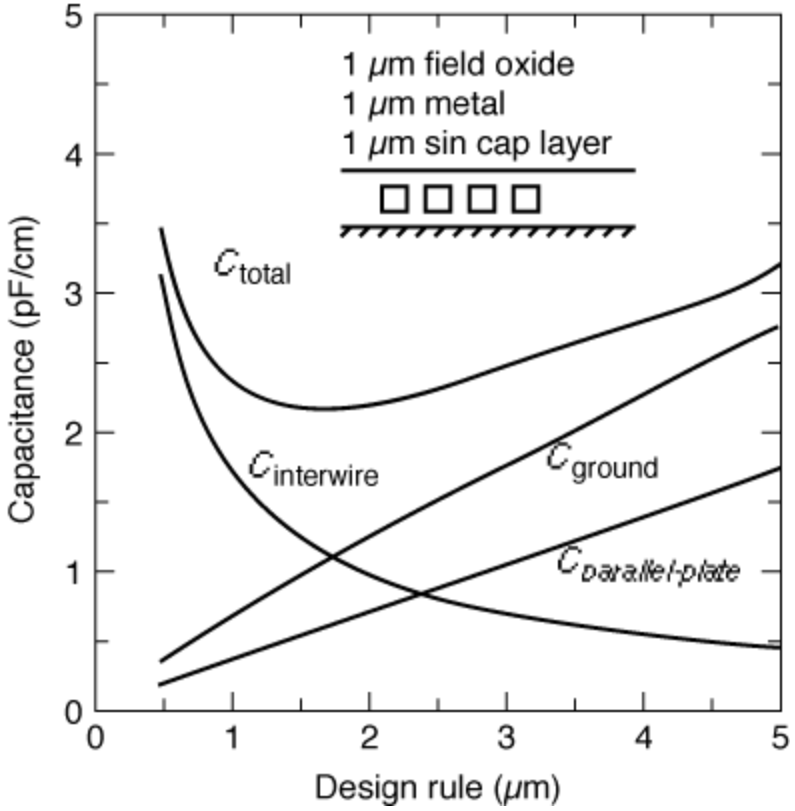
Interconnect Analysis
Capacitance (*6/8*)

- Interwire Capacitance



Interconnect Analysis
Capacitance (*7/8*)

- Impact of Interwire Capacitance



(from [Bakoglu89])

Interconnect Analysis
Capacitance (*8/8*)

- Wire Capacitances (0.25μm CMOS)

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Interconnect Analysis
Impact of Interconnect Capacitance

Influence of Interconnect Capacitance

- The wire delay is proportional to the capacitance charged.
- More capacitance means more dynamic power.
- **Coupling capacitance**
  - » Is an increasing source of noise.
  - » Makes delay estimation hard.

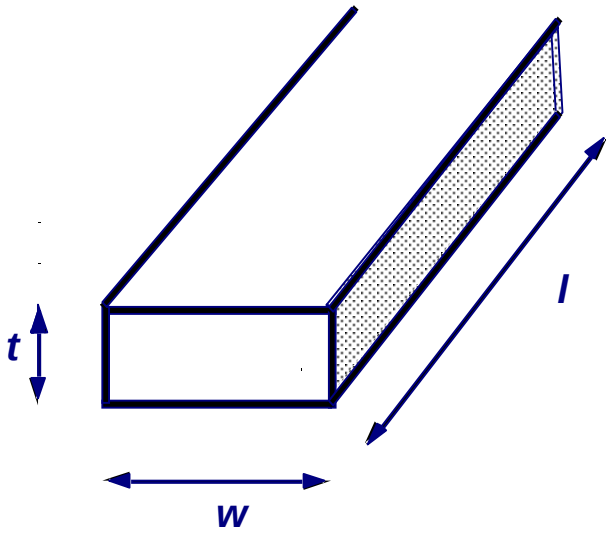
How to Reduce Interconnect Capacitance

- Use low *k* dielectric which reduces permittivity and hence the capacitance.
- Increase the spacing between the wires (***Not always possible***).
- Separate the two signals with a power or ground line (acting as shield).
- Use minimum wire width wherever possible. (***Increase resistance!***)

This slide is courtesy of Professor He.

Interconnect Analysis
Resistance (*1/3*)

- Wire Resistance



$$R = \frac{\rho\, l}{t\, w}$$

Sheet Resistance

R_o

Interconnect Analysis
Resistance (2/3)

- Interconnect Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Interconnect Analysis
Resistance (3/3)

- Sheet resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

Interconnect Analysis
Impact of Interconnect Resistance

Influence of Interconnect Resistance

- The wire delay is proportional to the wire resistance.
- **IR Drop Along the Wire**
  - » Proportional to the resistance ⇒ The noise margin is reduced.
  - » A significant problem in the power lines where current density is high.
- Contact resistance makes them vulnerable to electromigration.

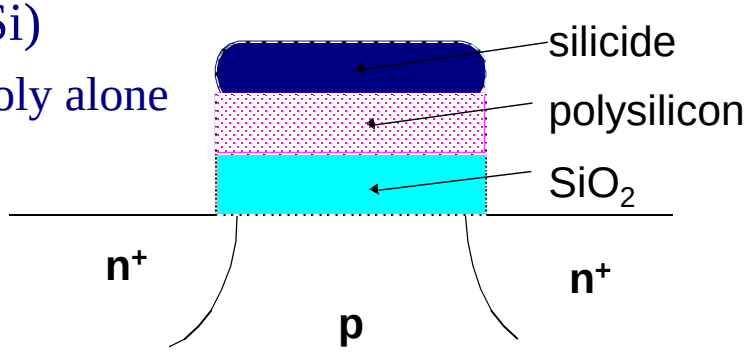
How to Reduce Interconnect Resistance

- Use materials with low resistivity (Cu).
- Reduce wire length (***Not always possible***).
- Increase width (***Increase area and capacitance!***).
- Increase height (***Increase fringe capacitance!***).
- Provide bigger contacts: Use less vias.
- Use metal instead of polysilicon even for short distance routing.
- Use silicide coating to reduce polysilicon resistance.

This slide is courtesy of Professor He.

Interconnect Analysis
Dealing with Resistance

- Selective technology scaling
  - Scale ***w*** while holding ***t*** constant
- Use better interconnect materials
  - Lower resistivity materials like copper
    - » As processes shrink, wires get shorter (reducing ***C***) but they get closer together (increasing ***C***) and narrower (increasing ***R***). So ***RC*** wire delay increases and capacitive coupling gets worse.
    - » Copper has about 40% lower resistivity than aluminum, so copper wires can be thinner (reducing ***C***) without increasing ***R***
  - Use silicides (WSi_2, $TiSi_2$, $PtSi_2$ and TaSi)
    - » Conductivity is ***8-10*** times better than poly alone

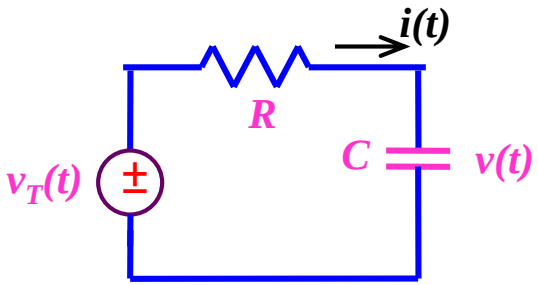


- Use more interconnect layers
  - reduces the average wire length *l* (but beware of extra contacts)

Interconnect Analysis
Analysis of Simple RC Circuit (*1/2*)

$$R \cdot i(t) + v(t) = v_T(t)$$

$$i(t) = \frac{d(Cv(t))}{dt} = C\frac{dv(t)}{dt}$$



$$\Rightarrow RC\frac{dv(t)}{dt} + v(t) = v_T(t)$$

← first-order linear differential equation with constant coefficients

state variable

Input waveform

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Interconnect Analysis
Analysis of Simple RC Circuit (2/2)

zero-input response: $$RC\frac{dv(t)}{dt}+v(t)=0$$

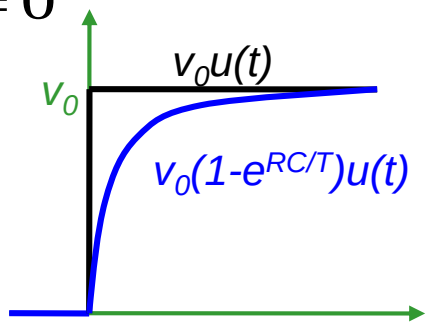
(natural response) $$\frac{1}{v(t)}\frac{dv(t)}{dt}=-\frac{1}{RC}\Rightarrow v_N(t)=Ke^{-t/RC}$$

step-input response: $$RC\frac{dv(t)}{dt}+v(t)=v_0u(t)$$

$$v_F(t)=v_0u(t)\Rightarrow v(t)=Ke^{-t/RC}+v_0u(t)$$

match initial state: $$v(0)=0 \quad\Rightarrow\quad K+v_0u(t)=0$$

output response for step-input: $$v(t)=v_0(1-e^{-t/RC})u(t)$$



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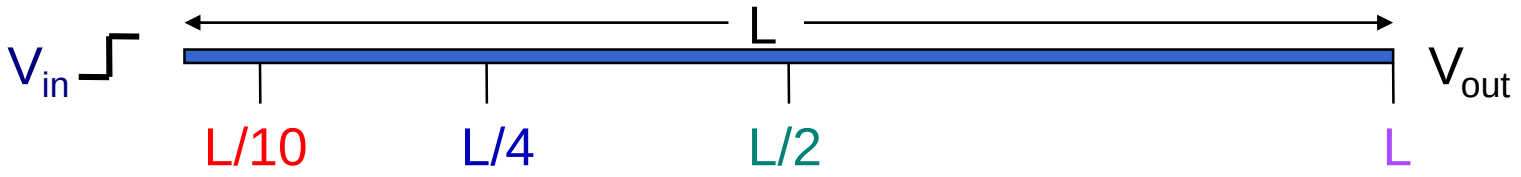
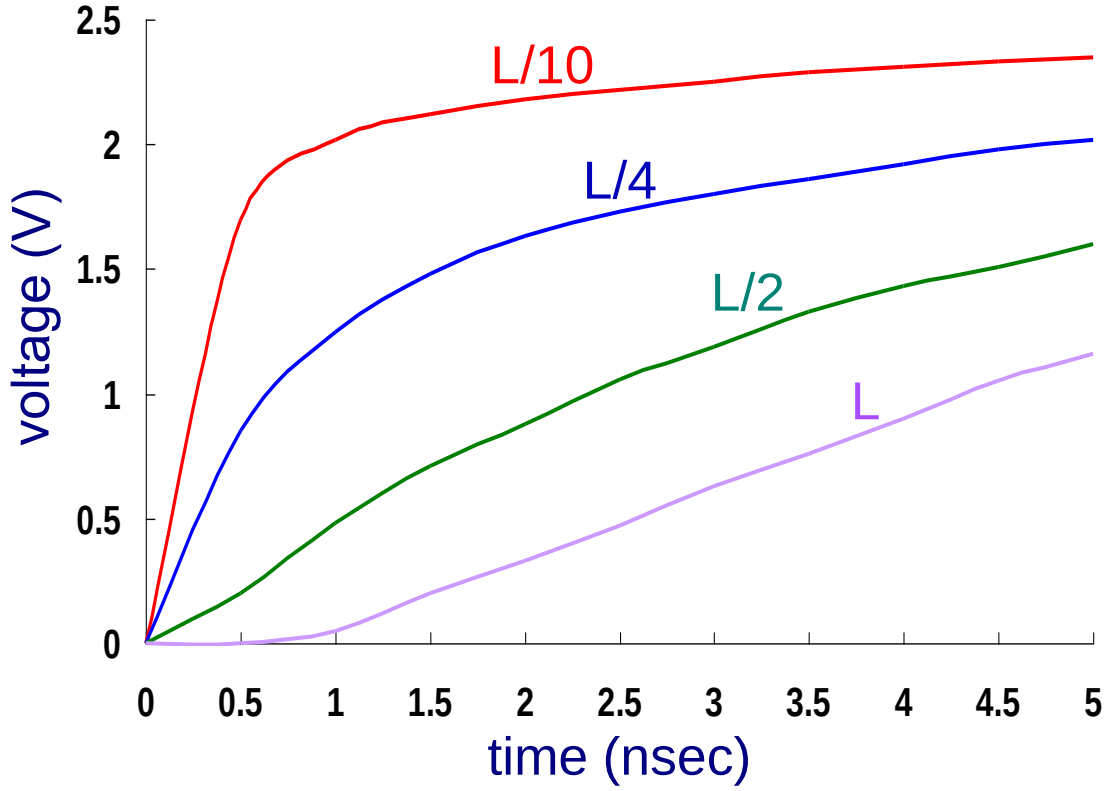
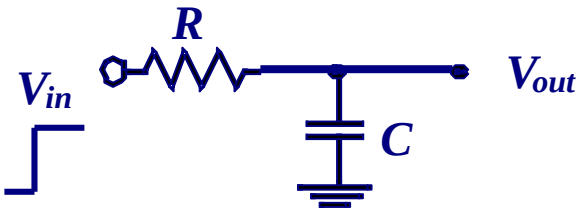
Interconnect Analysis
Step-response of RC wire





Interconnect Analysis
Wire Delay Models (*1/3*)

- **Ideal Wire**
  - » Same voltage is present at every segment of the wire at every point in time - at equal potential
  - » Only holds for *very short* wires, i.e., interconnects between *very* nearest neighbor gates
- **Lumped RC Model**
  - » Total wire resistance is lumped into a single R and total capacitance into a single C
  - » Good for short wires; pessimistic and inaccurate for long wires



$$V_{out}(t) = V_{DD}(1\text{-}exp(\text{-}t/RC))$$

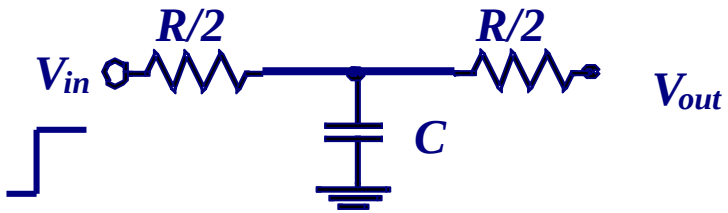
$$V_{50\%}(t) = V_{DD}(1\text{-}exp(\text{-}\tau_{PLH}/RC))$$

$$\tau_{PLH} \approx 0.69RC$$

Interconnect Analysis
Wire Delay Models (*2/3*)

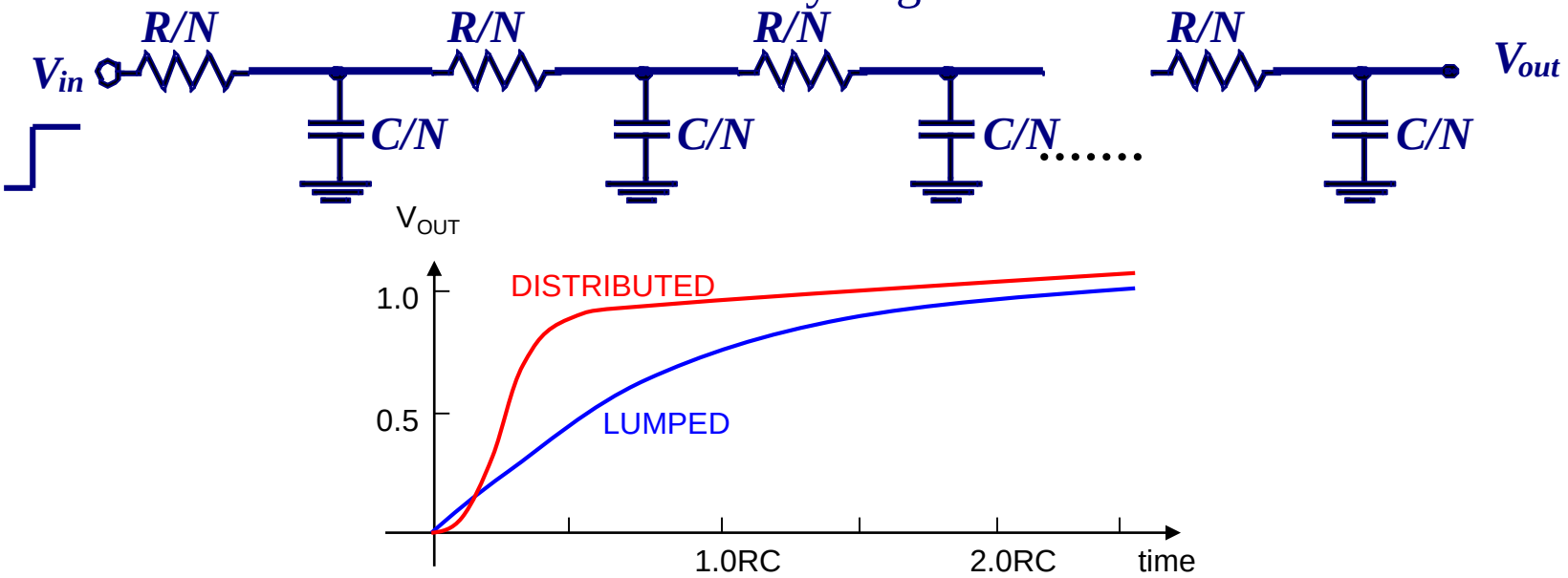
This simplest model provides a very rough approximation of the actual transient behavior of the interconnect line.

- **T-Model**
  - » The above simple lumped ***RC*** model can be significantly improved by the ***T-model*** as



Interconnect Analysis
Wire Delay Models (*3/3*)

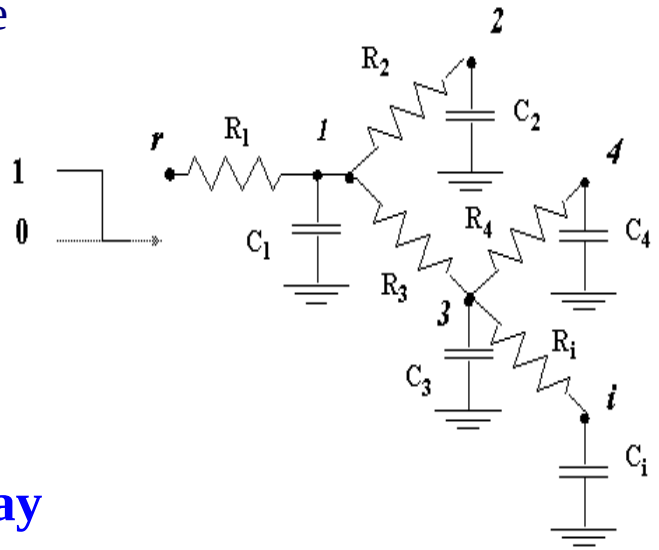
- **Distributed RC Model**
  - » The transient behavior of an interconnect line can be more accurately represented using the ***RC ladder network*****.** The transient behavior of this model approaches that of a ***distributed RC line*** for very large ***N***



Step response of distributed and lumped RC networks. A potential step is applied at V_{IN}, and the resulting V_{OUT} is plotted. The time delays between commonly used reference points in the output potential is also tabulated.

Interconnect Analysis
Computation of Elmore Delay (*1/5*)

- Consider a general ***RC tree network***
  - » No resistor loop
  - » All of the capacitances are connected between a node and ground
  - » One input node



- **The Elmore Delay**
  - » First order time constant (first moment of the impulse response) at node is a sum of **RC** components
  - » All the upstream resistances are taken into account
  - » Thus each node contributes to the delay
  - » Amount of contribution is the product of the capacitance at the node and the amount of resistance from source to the node.

Interconnect Analysis
Computation of Elmore Delay (*2/5*)

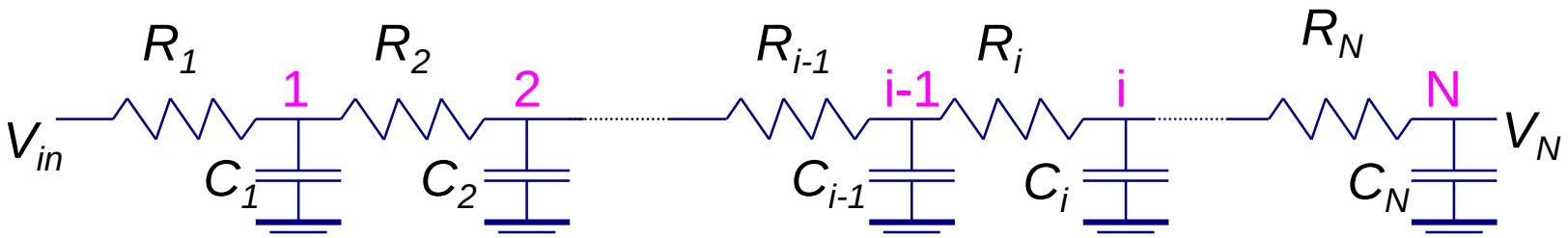
- Elmore analyzed the distributed model of the general ***RC tree network*** and came up with the figures for delay

$$\tau_{D_i} = \sum_{j=1}^{N} C_j R_{ij}$$

$$R_{ij} = \Sigma R_k \quad \textit{where } R_k \in [path(s \rightarrow i) \cap path(s \rightarrow j)]$$

Interconnect Analysis
Computation of Elmore Delay (*3/5*)

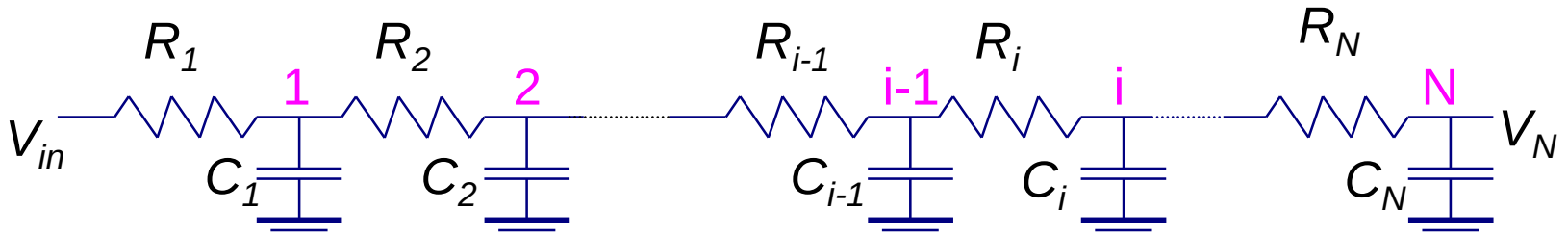
- **RC Chain**



Elmore delay equation $\tau_{DN} = \sum^{N} C_j R_{Nj}$

Interconnect Analysis
Computation of Elmore Delay (*4/5*)

$\tau_{D1}=C_1R_1 \quad \tau_{D2}=C_1R_1+C_2(R_1+R_2)$

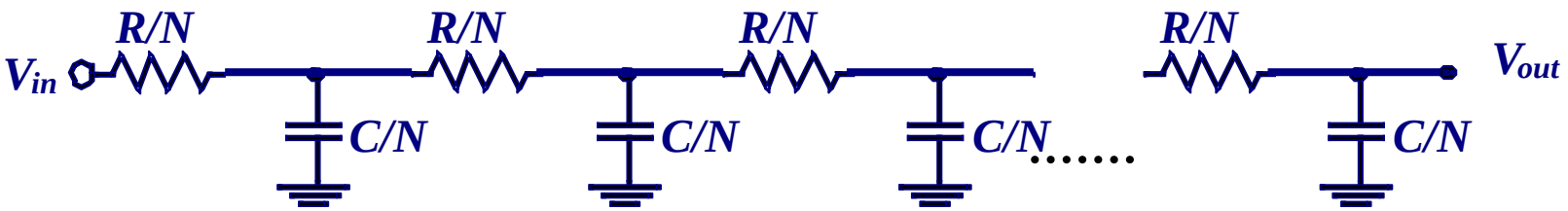


$\tau_{Di}=C_1R_1+C_2(R_1+R_2)+\ldots+C_i(R_1+R_2+\ldots+R_i)$

Elmore delay equation $\tau_{DN} = \sum C_j R_{Nj} = \sum^{N} C_j \sum^{j} R_i$

Interconnect Analysis
Computation of Elmore Delay (5/5)

- Assume: Wire modeled by ***N*** equal-length segments



$$\tau_{DN} = \sum_{j=1}^{N} \frac{C}{N} \sum_{k=1}^{j} \frac{R}{N} = \frac{R}{N^2}\left(R + 2R + \cdots + NR\right) = RC\left(\frac{N+1}{2N}\right)$$

- For large values of ***N***:

$$\tau_{DN} = RC/2$$

where ***R*** and ***C*** are the total lumped resistance and capacitance of the wire

Interconnect Analysis
Comments on Elmore Delay Model

Advantages

- Simple closed-form expression
  - » Useful for interconnect optimization
- Upper bound of 50% delay [Gupta et al., DAC'95, TCAD'97]
  - » Actual delay asymptotically approaches Elmore delay as input signal rise time increases
- High fidelity [Boese et al., ICCD'93],[Cong-He, TODAES'96]
  - » Good solutions under Elmore delay are good solutions under actual (SPICE) delay

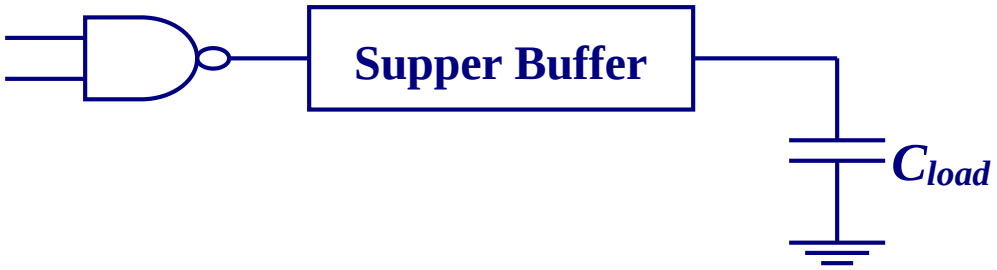
Disadvantages

- Low accuracy, especially poor for slope computation
- Inherently cannot handle inductance effect
  - » Elmore delay is first moment of impulse response
  - » Need higher order moments

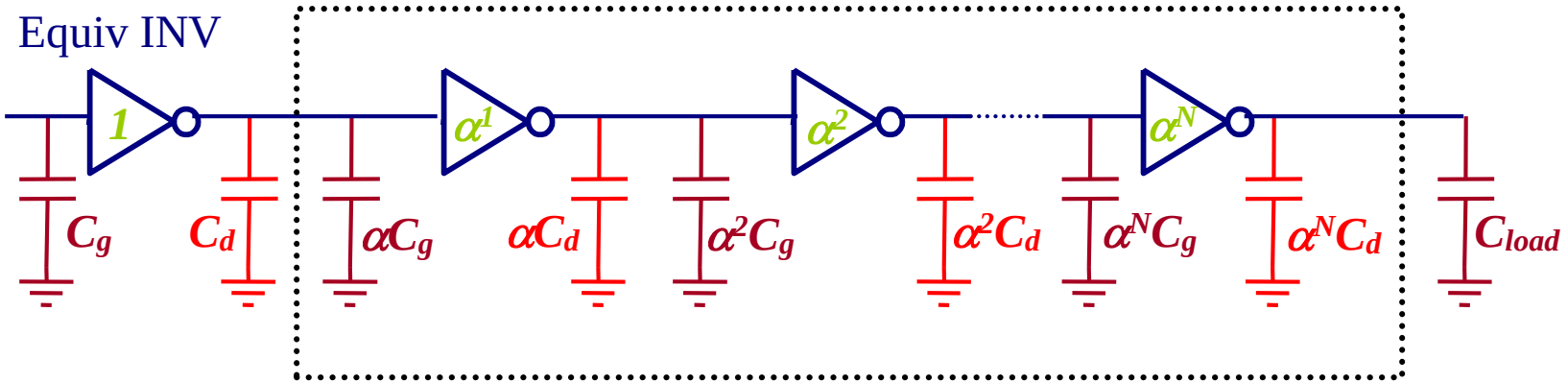
CMOS Digital Integrated Circuits

Super Buffer Design

Supper Buffer



- Given a large capacitance load C_{load}
  - How many stages are needed to minimize the delay?
  - How to size the inverters?



N: number of inverter stages

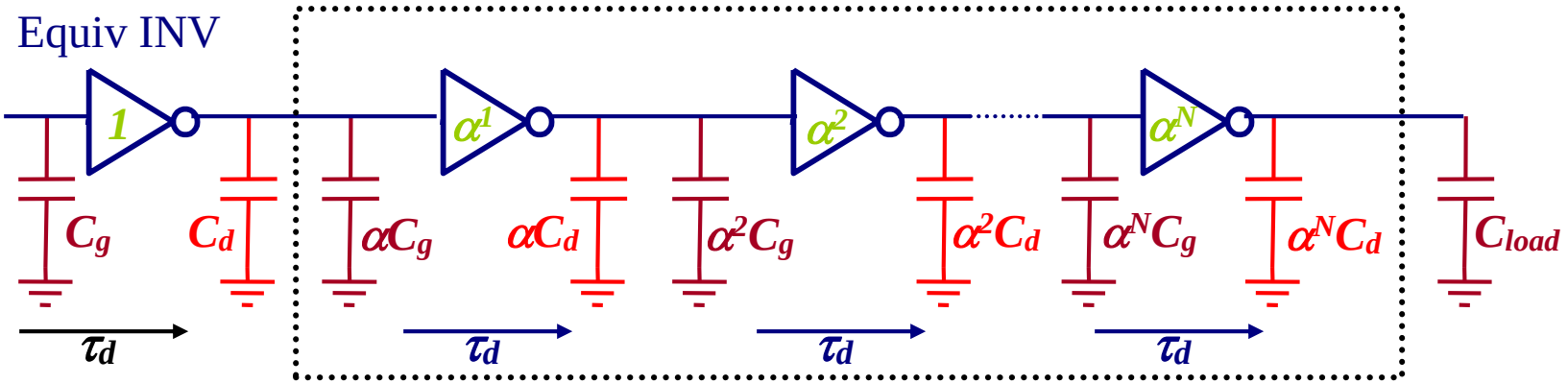
α: optimal stage scale factor

Supper Buffer (Cont.)

where

- C_g: the input capacitance of the first stage inverter.
- C_d: the drain capacitance of the first stage inverter.
- Each inverter is scaled up by a factor of α per stage.
- $C_{load} = \alpha^{N+1} C_g$
- All inverters have identical delay of $\tau_0(C_d+\alpha C_g)/(C_d+C_g)$ which τ_0 is per gate delay for Equiv INV in ring oscillator circuit with load capacitance = C_g+C_d

Supper Buffer Design



- Consider ***N*** stages, each inverter has same delay $\tau_0(C_d+\alpha C_g)/(C_d+C_g)$. Therefore,

$$\tau_{total} = (N+1)\tau_0\left(\frac{C_d + \alpha C_g}{C_d + C_g}\right)$$

Supper Buffer Design (Cont.)

- ***Goal:*** Choose α and N to minimize τ_{total}.
  - » By $C_{load} = \alpha^{N+1} C_g$, we have

$$(N+1) = \frac{\ln\left(\frac{C_{load}}{C_g}\right)}{\ln \alpha}$$

  - » Plug the above equation into τ_{total}, we get

$$\tau_{total} = \frac{\ln\left(\frac{C_{load}}{C_g}\right)}{\ln \alpha} \tau_0 \left(\frac{C_d + \alpha C_g}{C_d + C_g}\right)$$

  - » To minimize τ_{total}:

$$\frac{\partial \tau_{total}}{\partial \alpha} = \tau_0 \ln\left(\frac{C_{load}}{C_g}\right)\left[-\frac{\frac{1}{\alpha}}{(\ln \alpha)^2}\left(\frac{C_d + \alpha C_g}{C_d + C_g}\right) + \frac{1}{\ln \alpha}\left(\frac{C_g}{C_d + C_g}\right)\right] = 0$$

$$\alpha_{opt}(\ln \alpha_{opt} - 1) = \frac{C_d}{C_g}$$

Supper Buffer Design (Con.)

- » For the special case $C_d=0 \Rightarrow \ln(\alpha_{opt})=0 \Rightarrow \alpha_{opt} = e$. However, in reality the drain parasitics cannot be ignored.

- Example: For C_d=0.5 fF, C_g=1 fF, determine α_{opt} and N for C_{load} = 50 pF.

  $\alpha_{opt}(\ln \alpha_{opt} - 1) = 0.5 \Rightarrow \alpha_{opt} = 3.18$

$$N+1 = \frac{\ln(C_{load}/C_g)}{\ln \alpha_{opt}}$$

$$N = \left[\ln(C_{load}/C_g)/\ln \alpha_{opt}\right] - 1$$

$$= \left[\ln(50\times10^{-12}/1\times10^{-14})/\ln 3.18\right] - 1$$

$$= 6.36$$

The Super Buffer Design which minimizes τ_{total} for C_{load} = 50 pF is $N=7$ Equiv INV stages, and α_{opt} = 3.18

CMOS Ring Oscillator Circuit

- Oscillation period T is equal to

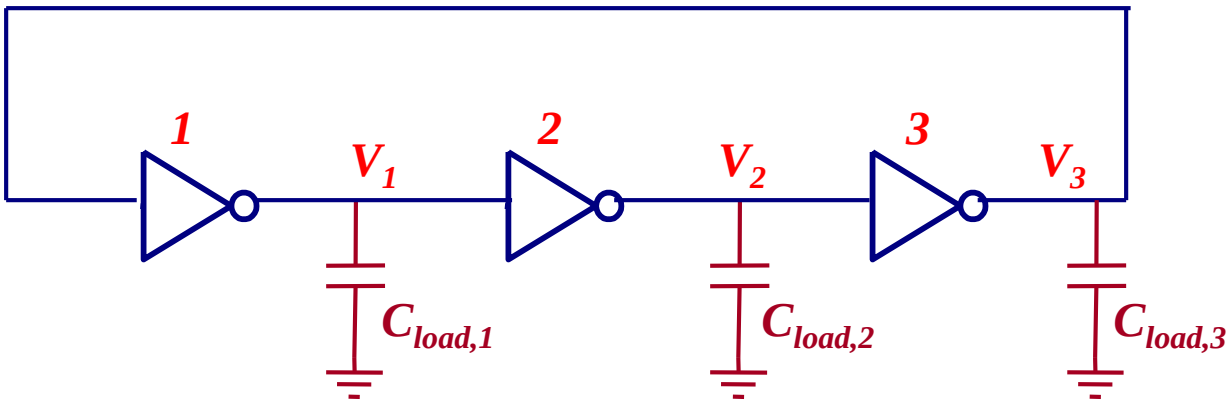
$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLL3}$$
$$= 2\tau_p + 2\tau_p + 2\tau_p$$
$$= 3 \cdot 2\tau_p = 6\tau_p$$

- For arbitrary odd number (n) of cascade-connected invertes, we have

$$f = 1/T = 1/(2 \cdot n \cdot \tau_p)$$

- Also, we can write

$$\tau_p = 1/(2 \cdot n \cdot f)$$



Voltage Waveforms of Ring Oscillator