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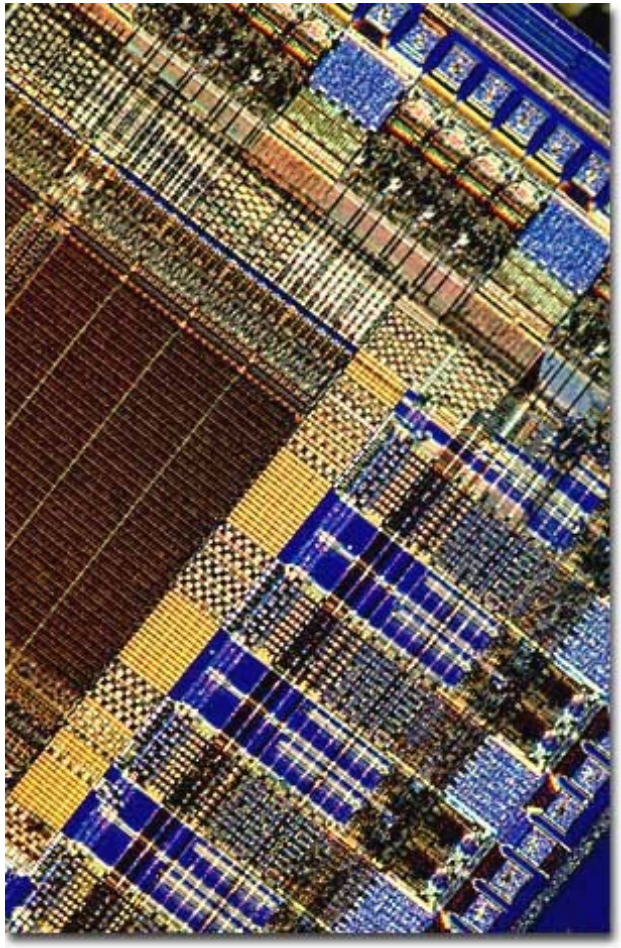

Chapter 1
Introduction

S.M. Kang and Y. Leblebici

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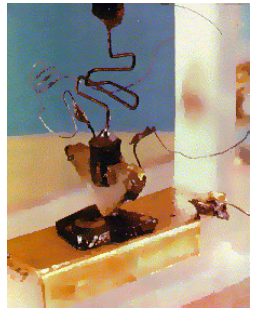
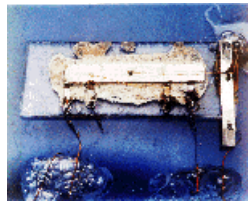
Some History

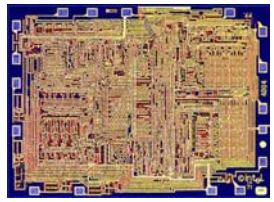
Invention of the transistor (BJT) 1947
Shockley, Bardeen, Brattain – Bell Labs



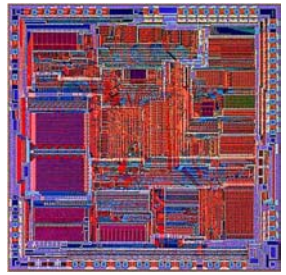
Single-transistor integrated circuit 1958
Jack Kilby – Texas Instruments



Invention of CMOS logic gates 1963
Wanlass & Sah – Fairchild Semiconductor



First microprocessor (Intel 4004) 1970
2,300 MOS transistors, 740 kHz clock frequency



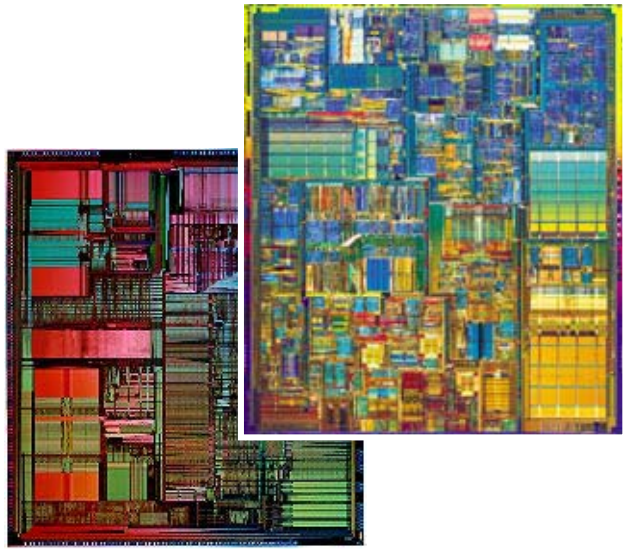
Very **L**arge **S**cale **I**ntegration 1978
Chips with more than ~20,000 devices

More Recently

Ultra **L**arge **S**cale **I**ntegration

System **o**n **C**hip (**SoC**)

20 ~ 30 million transistors in 2002



The chip complexity has increased by a factor of 1000 since its first introduction, but the term **VLSI** remained virtually universal to denote digital integrated systems with high complexity.

Some Leading-Edge Examples

Intel Pentium 4

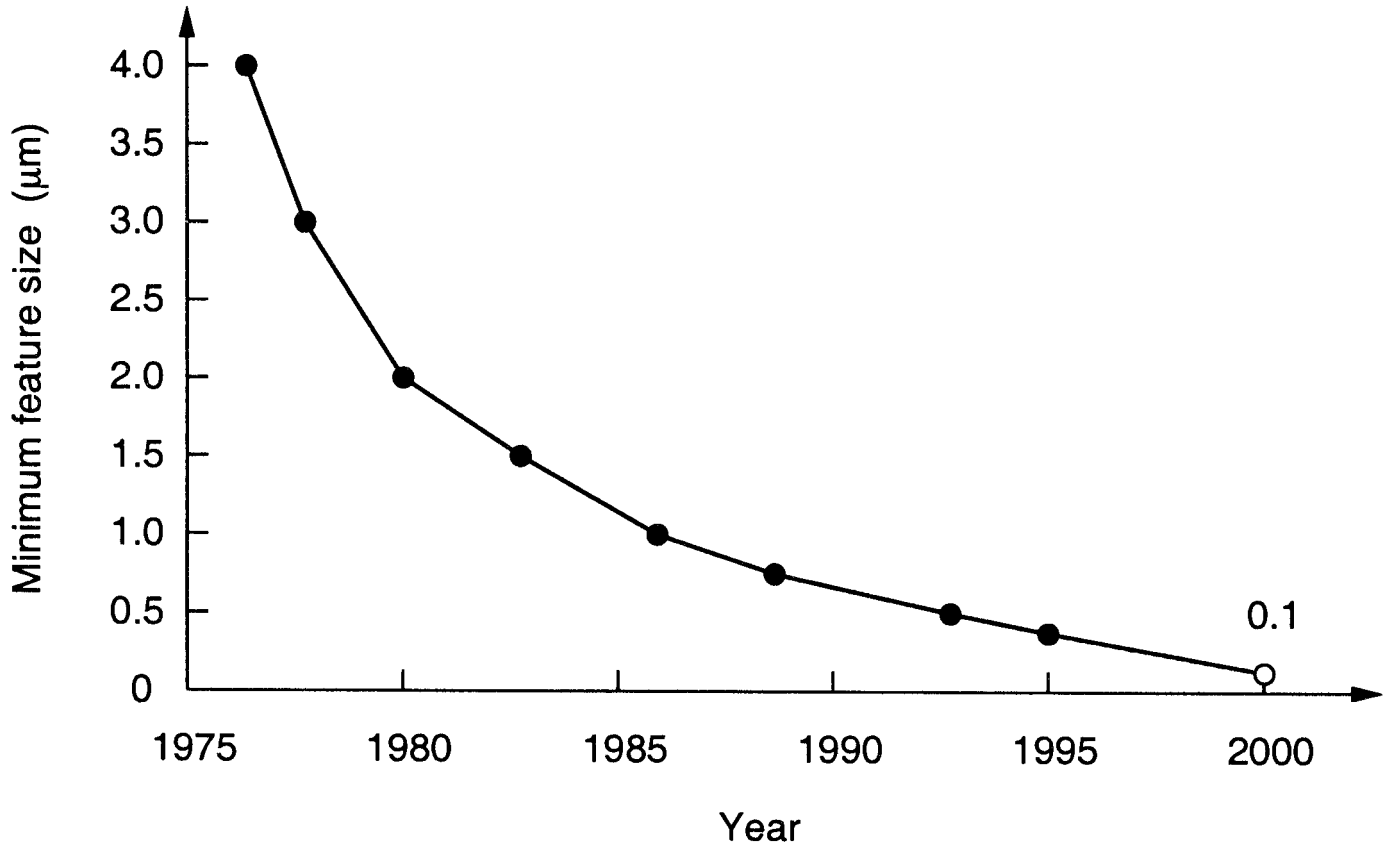
0.13μ process

55 million transistors

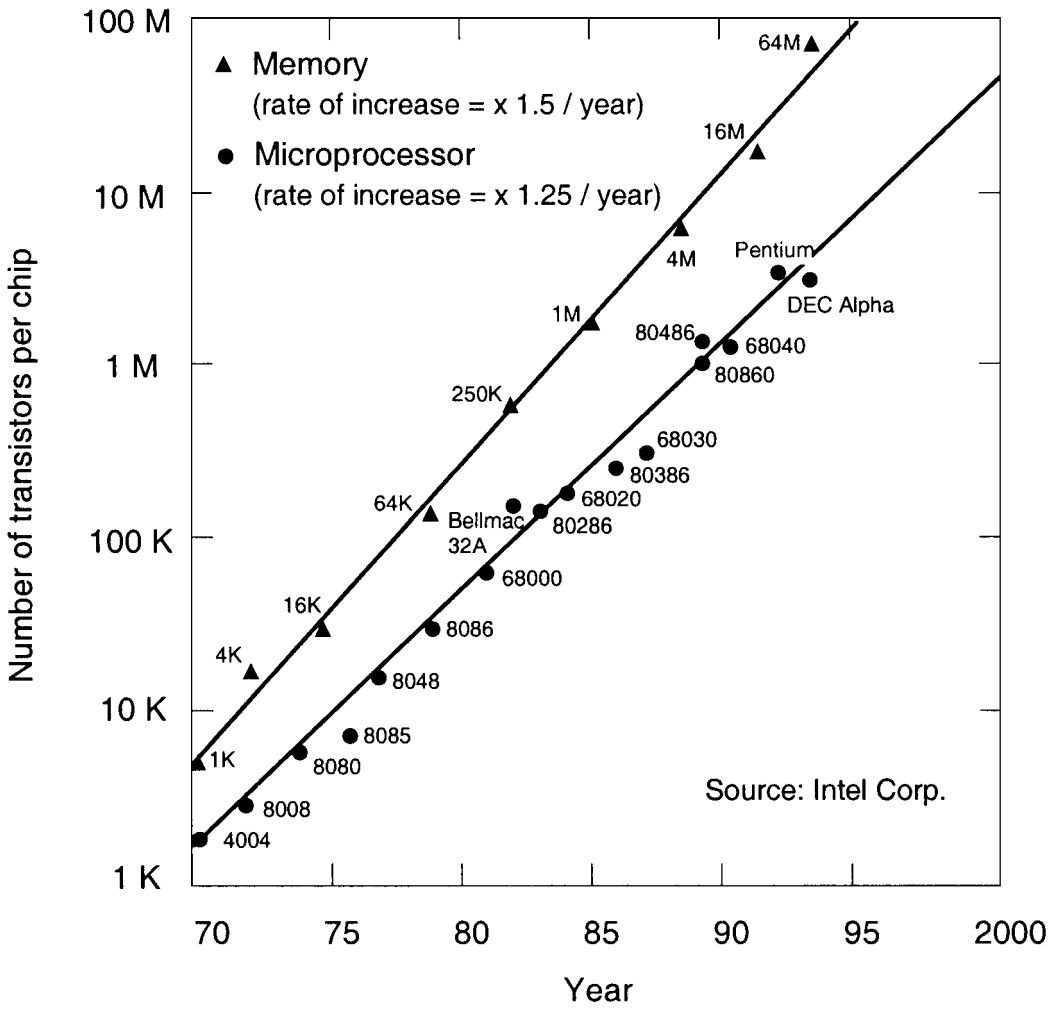
2.4GHz clock

145mm^2

Evolution of Minimum Feature Size



Moore's Law



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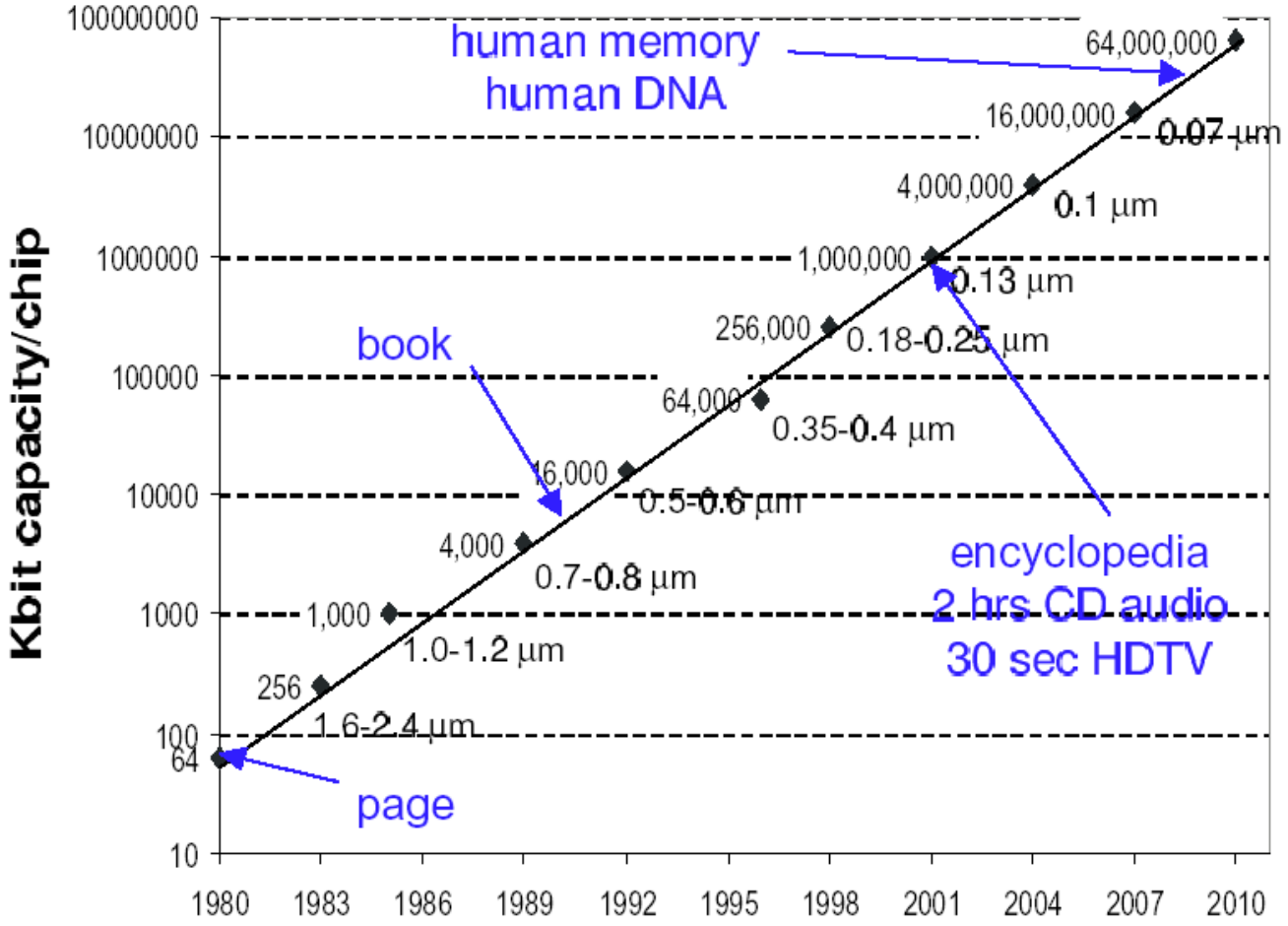
Evolution of Memory Capacity



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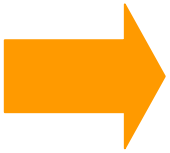
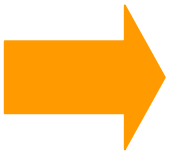
Shrinking Device Dimensions



YEAR	2002	2005	2008	2011	2014
TECHNOLOGY	130 nm	100 nm	70 nm	50 nm	35 nm
CHIP SIZE	400 mm^2	600 mm^2	750 mm^2	800 mm^2	900 mm^2
NUMBER OF TRANSISTORS (LOGIC)	400 M	1 Billion	3 Billion	6 Billion	16 Billion
DRAM CAPACITY	2 Gbits	10 Gbits	25 Gbits	70 Gbits	200 Gbits
MAXIMUM CLOCK FREQUENCY	1.6 GHz	2.0 GHz	2.5 GHz	3.0 GHz	3.5 GHz
MINIMUM SUPPLY VOLTAGE	1.5 V	1.2 V	0.9 V	0.6 V	0.6 V
MAXIMUM POWER DISSIPATION	130 W	160 W	170 W	175 W	180 W
MAXIMUM NUMBER OF I/O PINS	2500	4000	4500	5500	6000

Increasing Function Density



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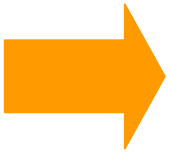
Increasing Clock Frequency



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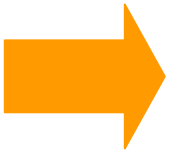
Decreasing Supply Voltage



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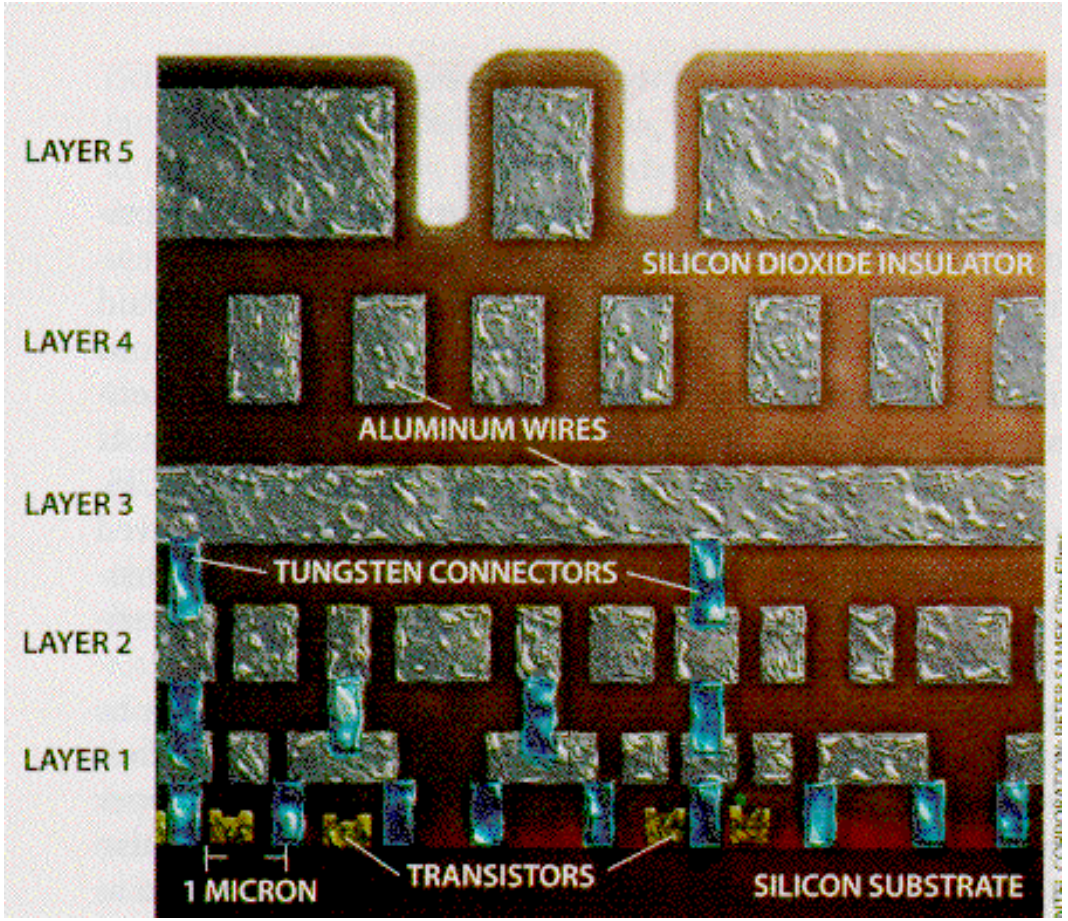
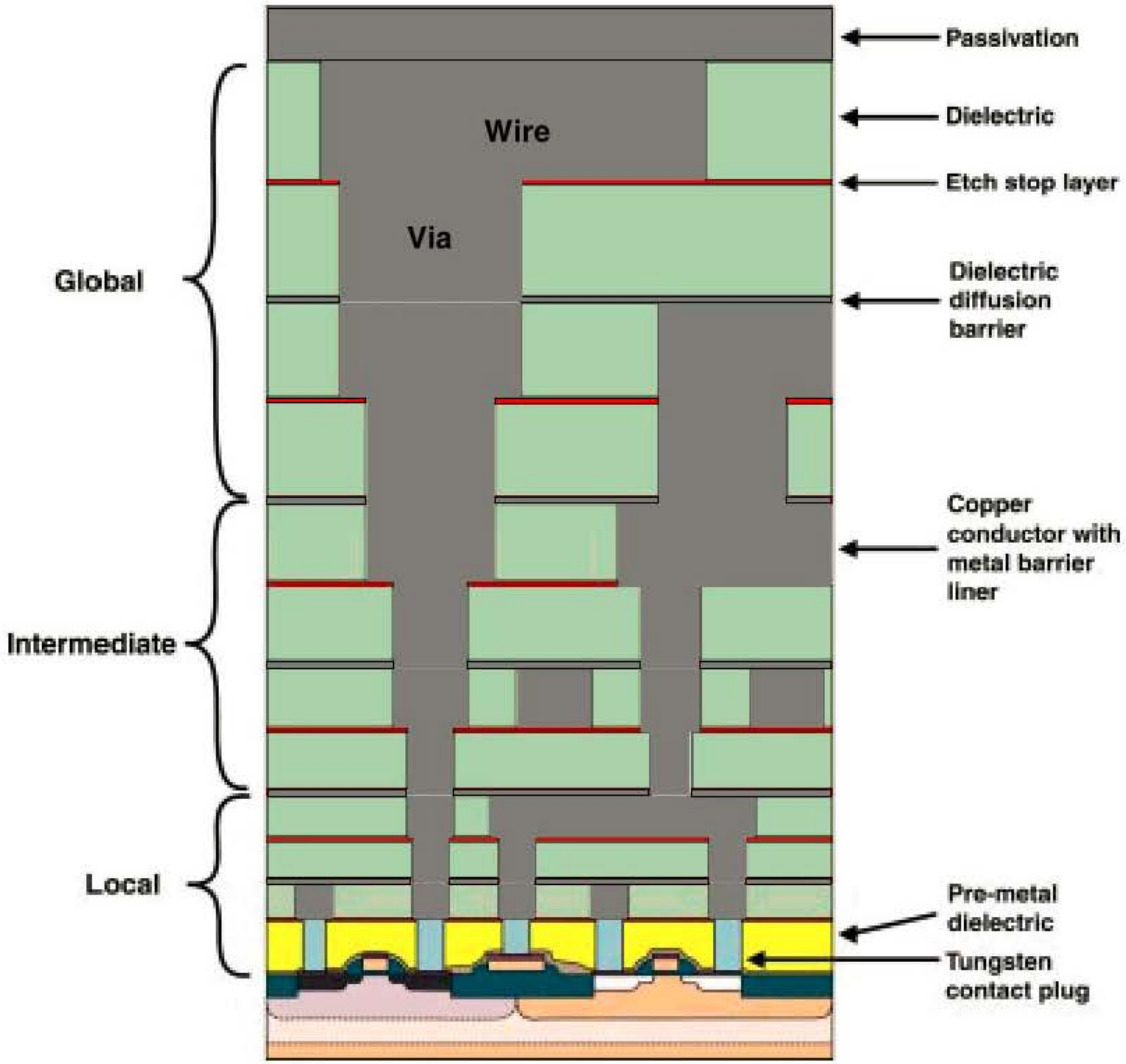


5-layer cross-section of chip

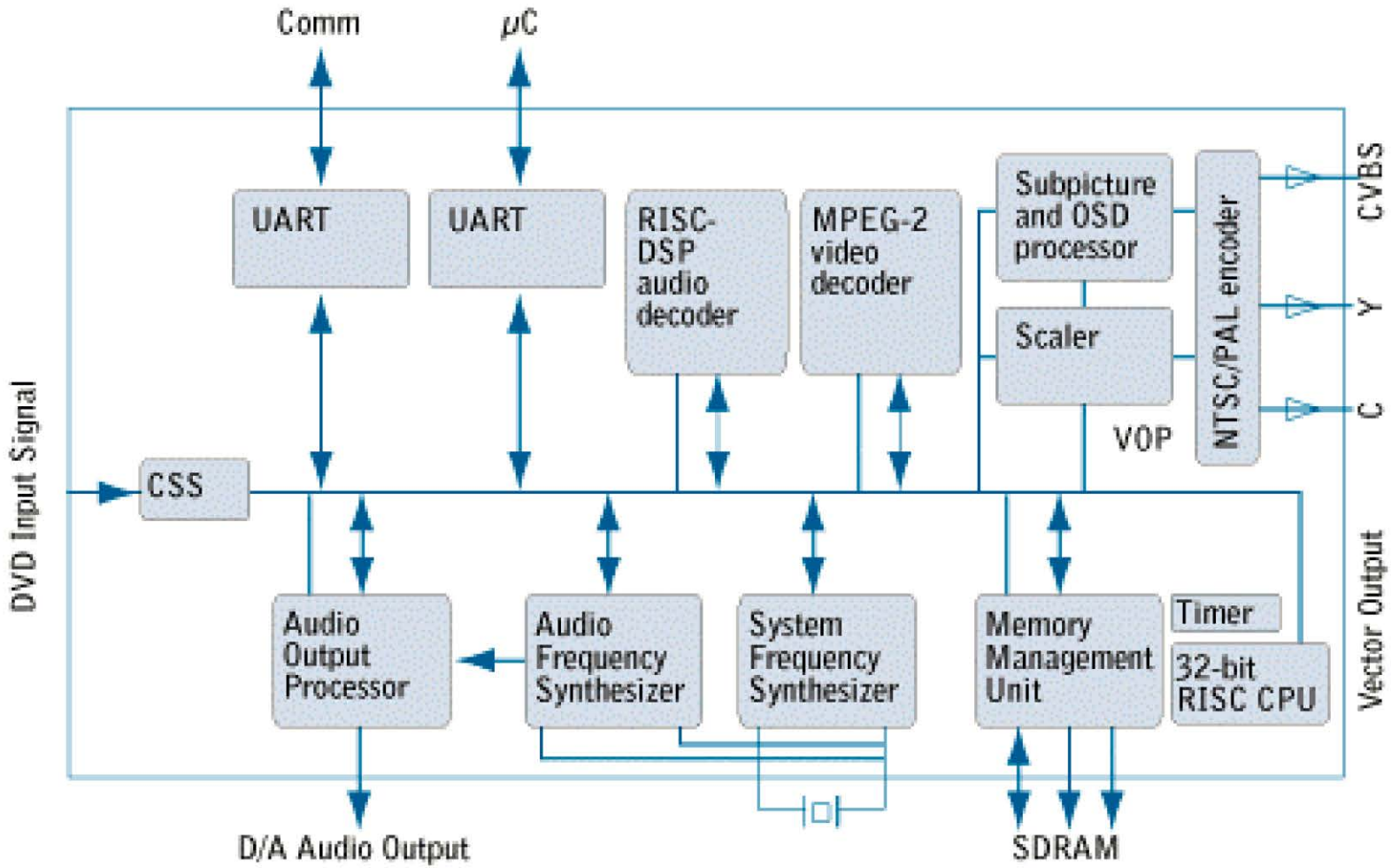
Typical Chip Cross Section



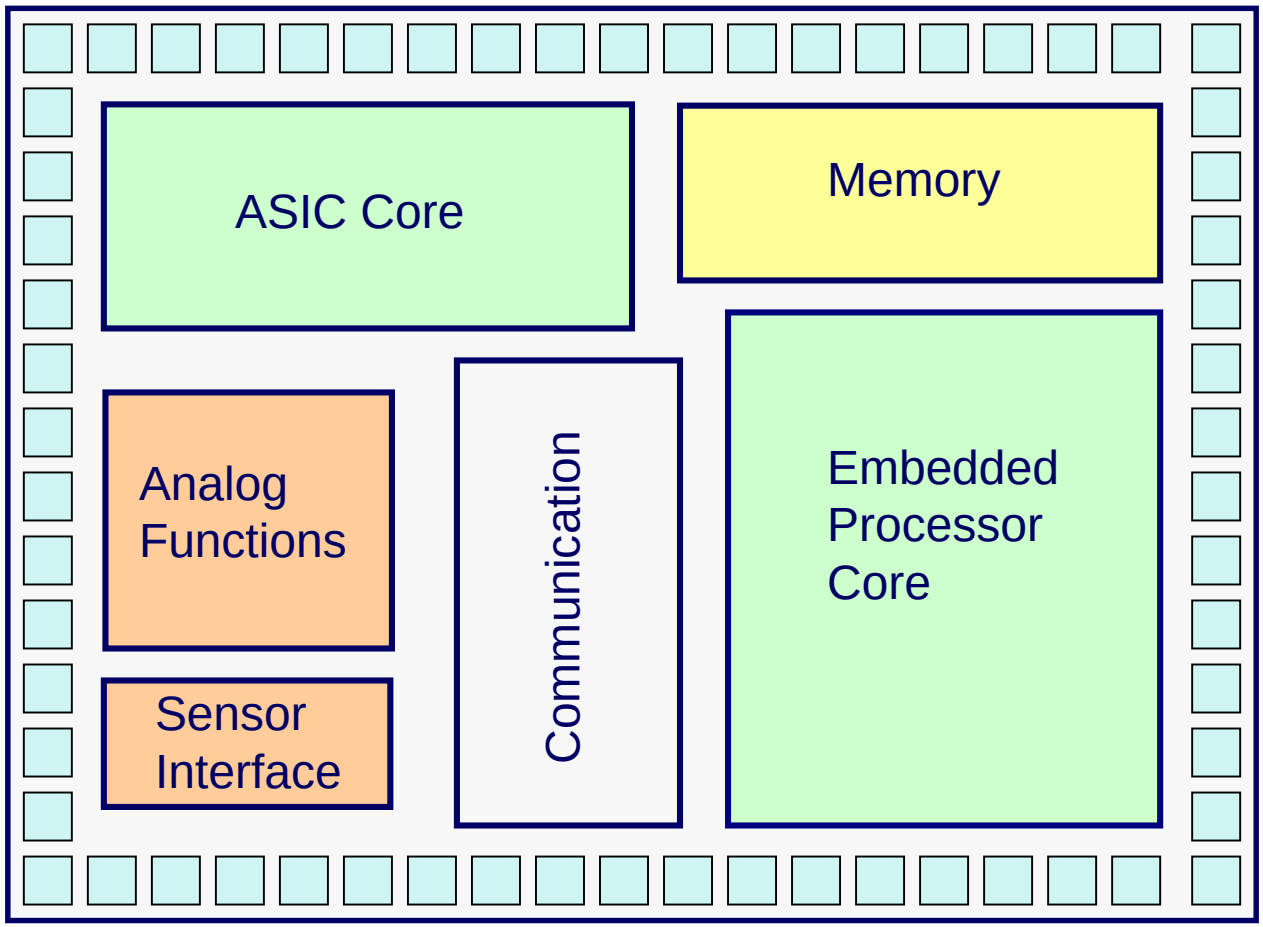
System-on-Chip

Integrating all or most of the components of a hybrid system on a single substrate (silicon or MCM), rather than building a conventional printed circuit board.

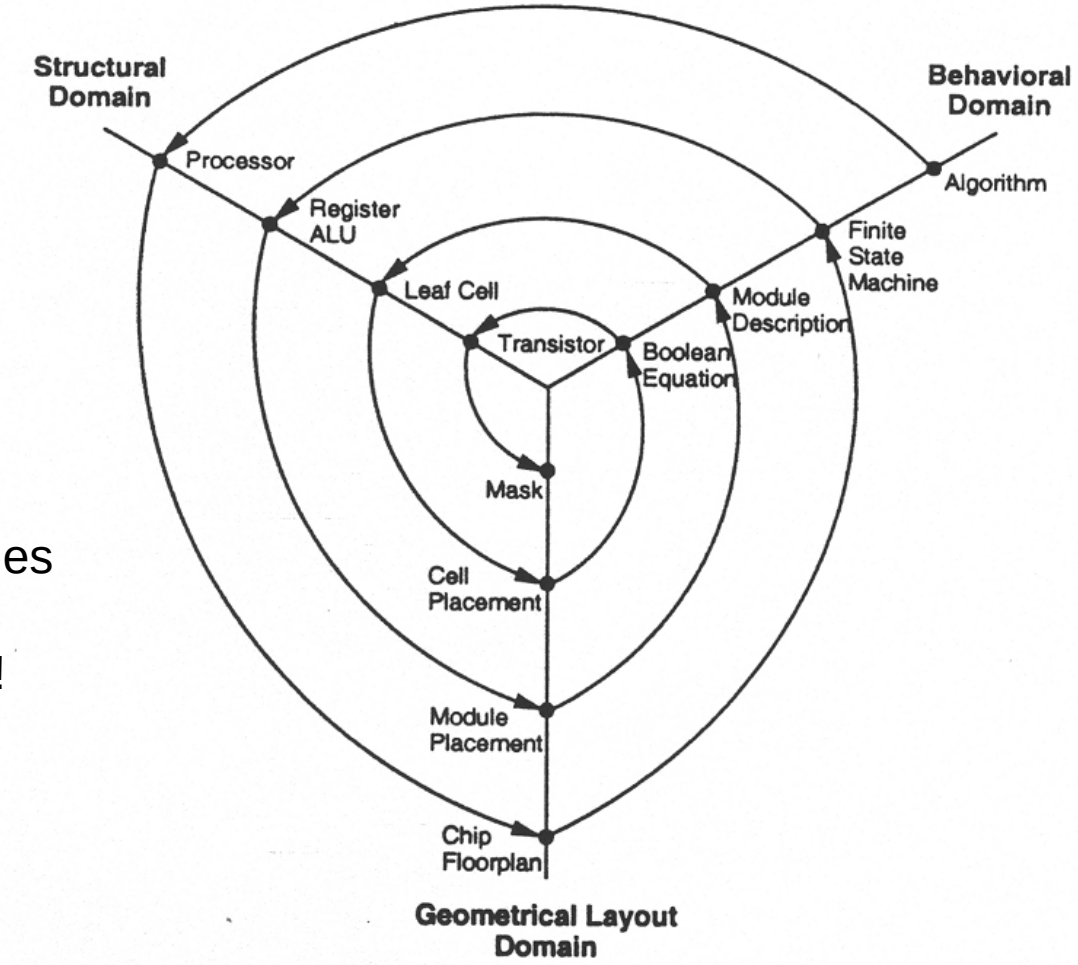
1. More compact system realization
2. Higher speed / performance
   - Better reliability
   - Less expensive !


Comm
µC
UART
UART
RISC-
DSP
audio
decoder
MPEG-2
video
decoder
Subpicture
and OSD
processor
Scaler
VOP
NTSC/PAL encoder
CVBS
Y
C
DVD Input Signal
CSS
Audio
Output
Processor
Audio
Frequency
Synthesizer
System
Frequency
Synthesizer
Memory
Management
Unit
Timer
32-bit
RISC CPU
Vector Output
D/A Audio Output
SDRAM

New Direction: System-on-Chip (SoC)



The Y-Chart



Notice: There is a need for structured design methodologies to handle the high level of complexity !

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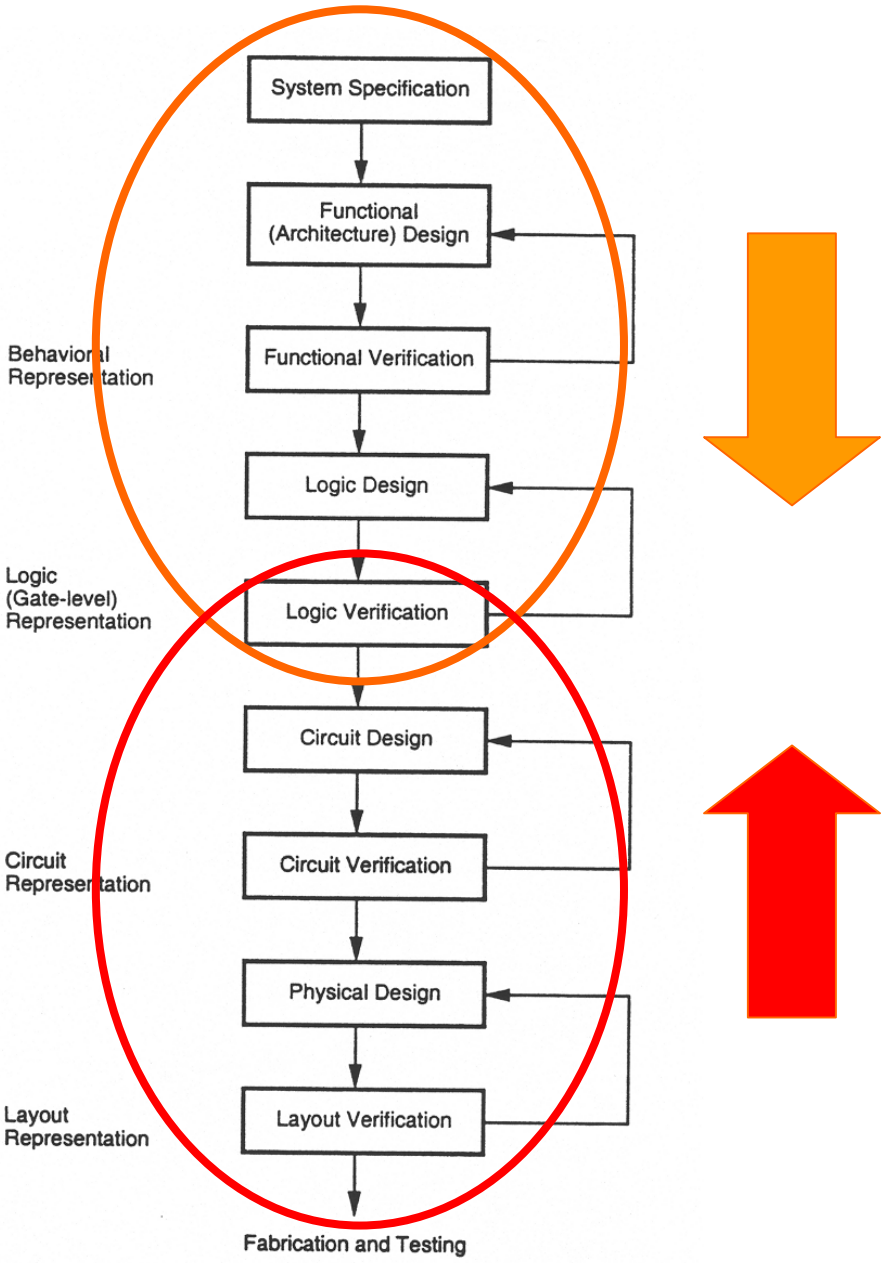
Simplified VLSI Design Flow



Top-down

Bottom-up

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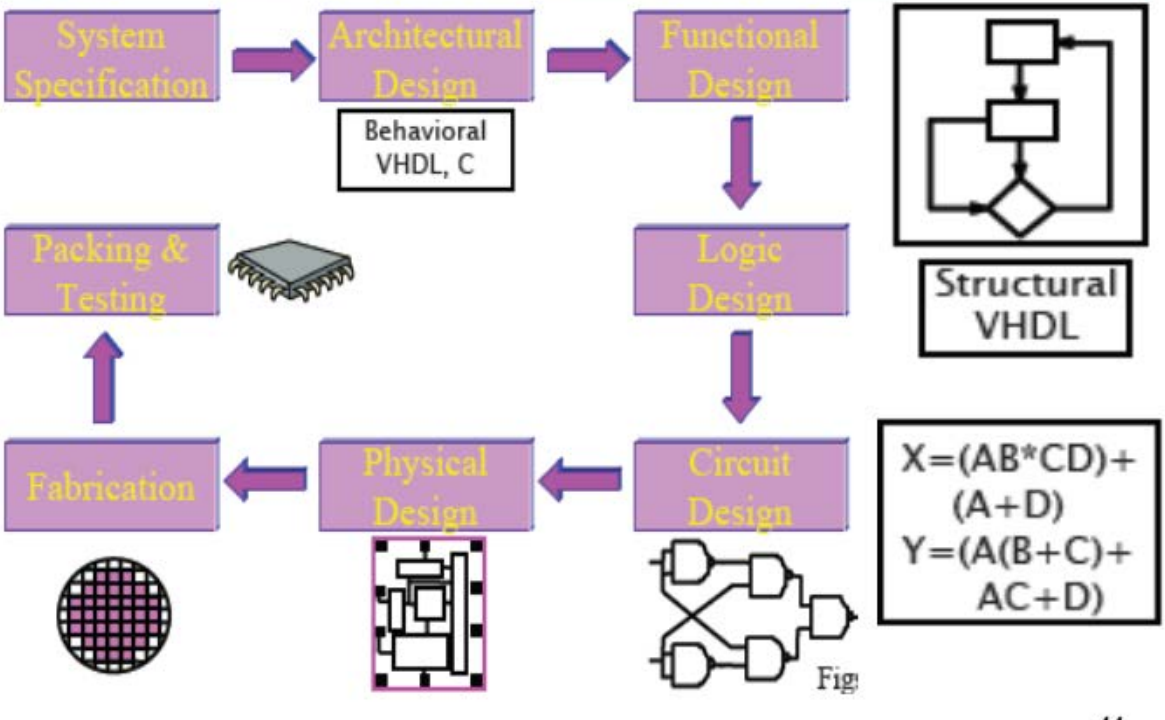
Top-down vs. bottom-up design

- Top-down design adds functional detail.
  – Create lower levels of abstraction from upper levels.
- Bottom-up design creates abstractions from low-level behavior.
- Good design needs both top-down and bottom-up efforts.

VLSI Design Cycle



VLSI Design Cycle

- **System Specification**

– A high level representation of the system

– Considered factors

» Performance

» Functionality

» Physical dimensions (die size)

– Result Specs – size, speed, power, and functionality

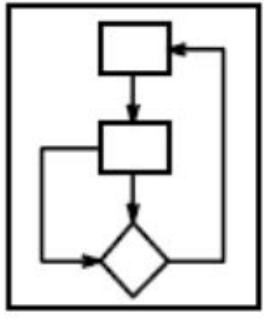
VLSI Design Cycle

- **Architectural Design**
  - RISC (Reduced Instruction Set Computer) versus CISC (Complex Instruction Set Computer)
  - Number of ALUs, Floating Point Units
  - Number and structure of pipelines
  - Cache size
  - Prediction on die size, power, and speed based on existing design
  - Early estimation are very important here

VLSI Design Cycle

Behavioral or Functional Design

- Only behavior and timing without implementation issue
- Specify behavior based on Input + output + timing
- Fast emulation and debugging for the system



```
always @(posedge clk);
  begin
    if (enable_ == 1'b0)
      data = 0;
    else
      data = data + 1;
  end
```

HDL-Based Design

1980's

Hardware Description Languages (HDL) were conceived to facilitate the information exchange between design groups.

1990's

The increasing computation power led to the introduction of logic synthesizers that can translate the description in HDL into a synthesized gate-level net-list of the design.

2000's

Modern synthesis algorithms can optimize a digital design and explore different alternatives to identify the design that best meets the requirements.

VLSI Design Cycle

- **Logic Design**

– Control flow, word widths, register allocation, arithmetic operations, and logic operations

– RTL (Register Transfer Level) – HDL (Hardware Description Language)

» Verilog – most popular

» VHDL – Europe and Eastern

» Literal + Timing Information

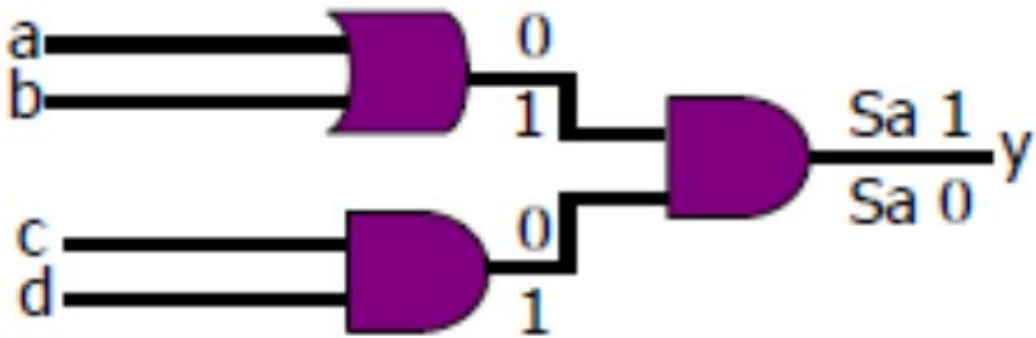
Boolean Expression

Timing Information

$$X=(AB*CD)+(A+D)$$
$$Y=(A(B+C)+AC+D)$$

VLSI Design Cycle

- **Logic Design**
  - **More actual simulation and testing**

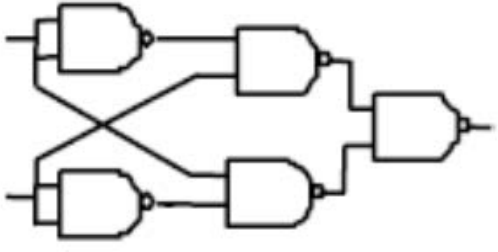


  - **High Level Synthesis: Produce a RTL description from a behavioral description of the design**

VLSI Design Cycle

Circuit Design

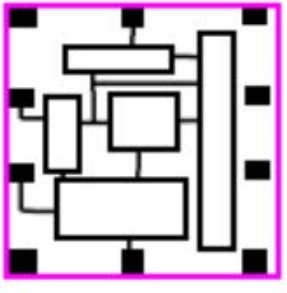
– Boolean Expression → Circuit Elements (Cells, Macros, Gates, Transistors) + Interconnection
– Each component has specific timing and power Info.
– Circuit Simulation : Verify the correctness and timing
– Terms – Netlist, Schematic
– Logic Synthesis Tool s : RTL → Netlist

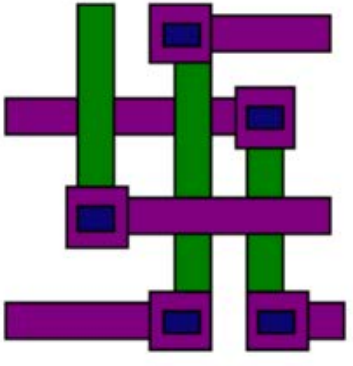


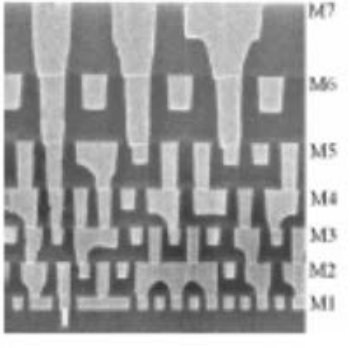
VLSI Design Cycle

Physical Design

- Netlist → Layout (Geometry Representation)
  - » Design rules of applied fabrication process
- Layout Synthesis Tools
  - » Automatic conversion (Fully/Partially)
  - » Area and performance penalty
- Crucial Challenges – Area/Delay



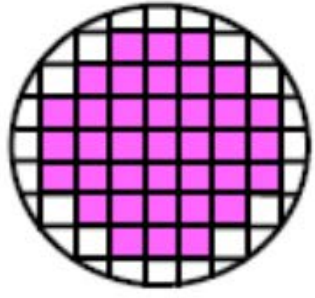




VLSI Design Cycle

Fabrication

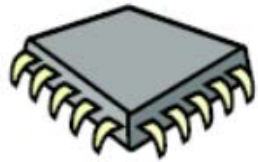
– Layout → Photo-lithographic mask
  » One mask for each layer
– Wafer : Silicon crystal are grown & sliced
– Deposition, and diffusion of various materials on
  the wafer : each step uses one mask
– Term : Tape Out, 8 inch/20cm, 12 inch/30cm



VLSI Design Cycle

Packaging, Testing, and Debugging

- For PCB (Printed Circuit Board) : DIP (Dual In-line Package), PGA (Pin Grid Array), BGA (Ball Grid Array), and QFP (Quad Flat Package)
- For MCM (Multi-Chip Modules): no packaged
- Testing
  - » Before Package – Probe line testing
  - » After Package – Tester machine applies test patterns.



Structured Design Principles

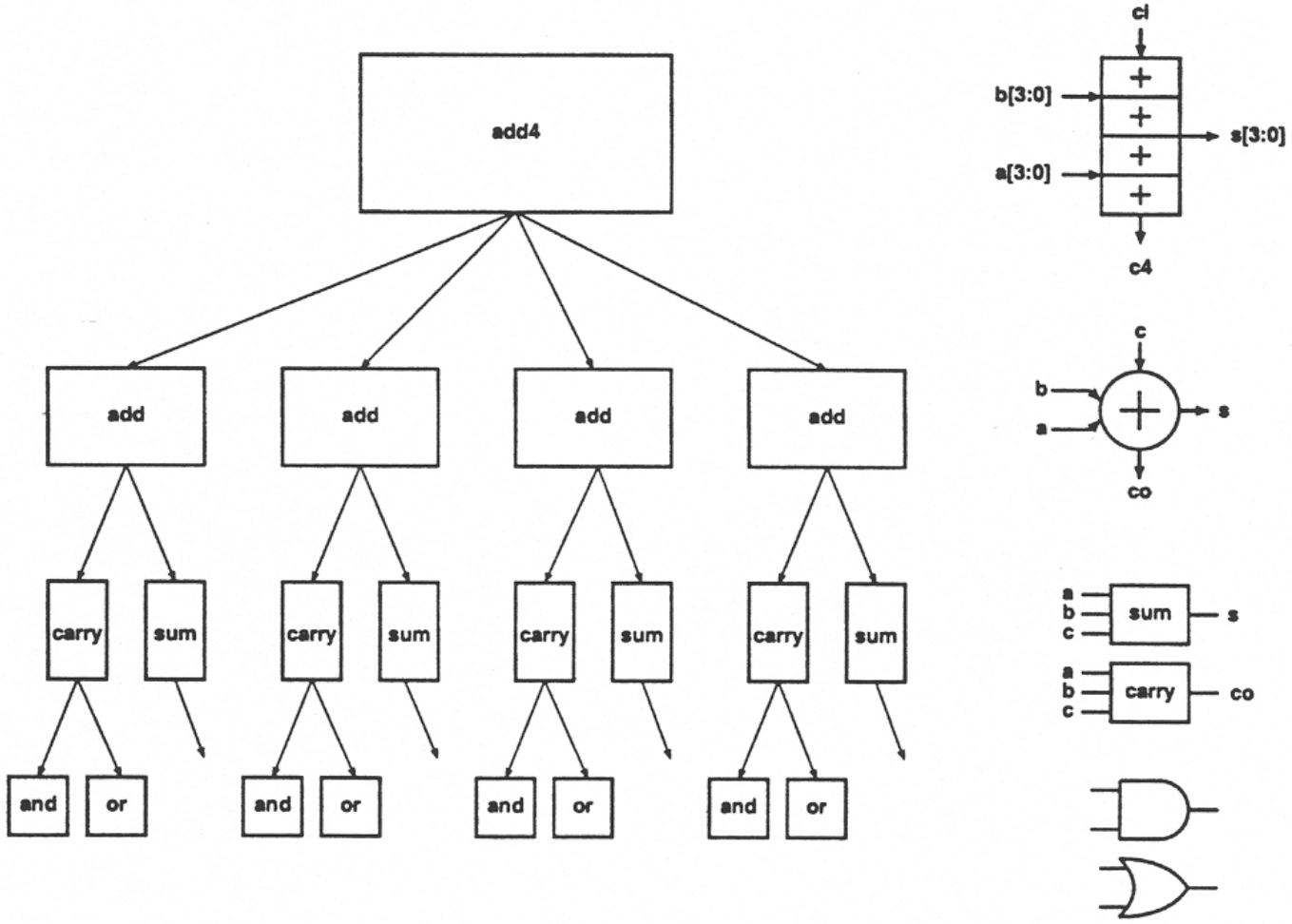
Hierarchy: "Divide and conquer" technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.

Regularity: The hierarchical decomposition of a large system should result in not only **simple**, but also **similar** blocks, as much as possible. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

Modularity: The various functional blocks which make up the larger system must have **well-defined functions** and **interfaces**.

Locality: Internal details remain at the local level. The concept of locality also ensures that connections are mostly between neighboring modules, **avoiding long-distance connections** as much as possible.

Hierarchy of a 4-bit Carry Ripple Adder



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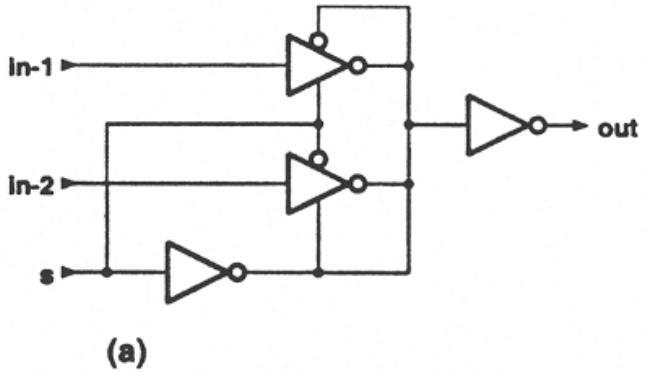
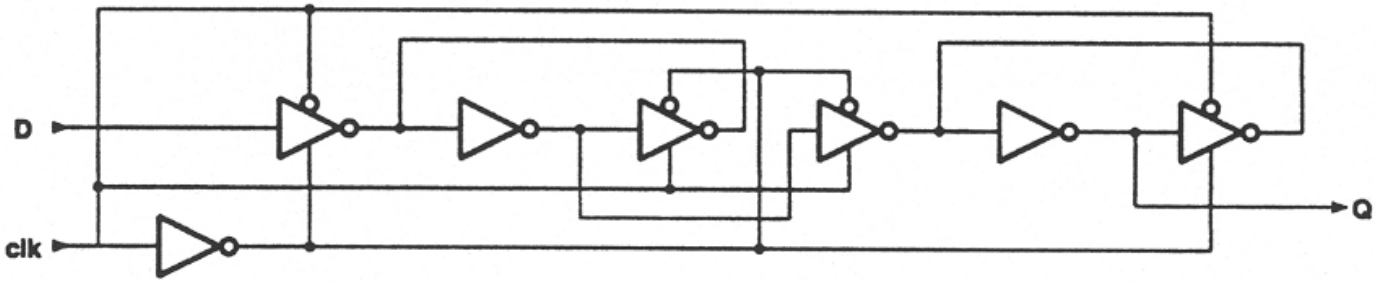
Regularity

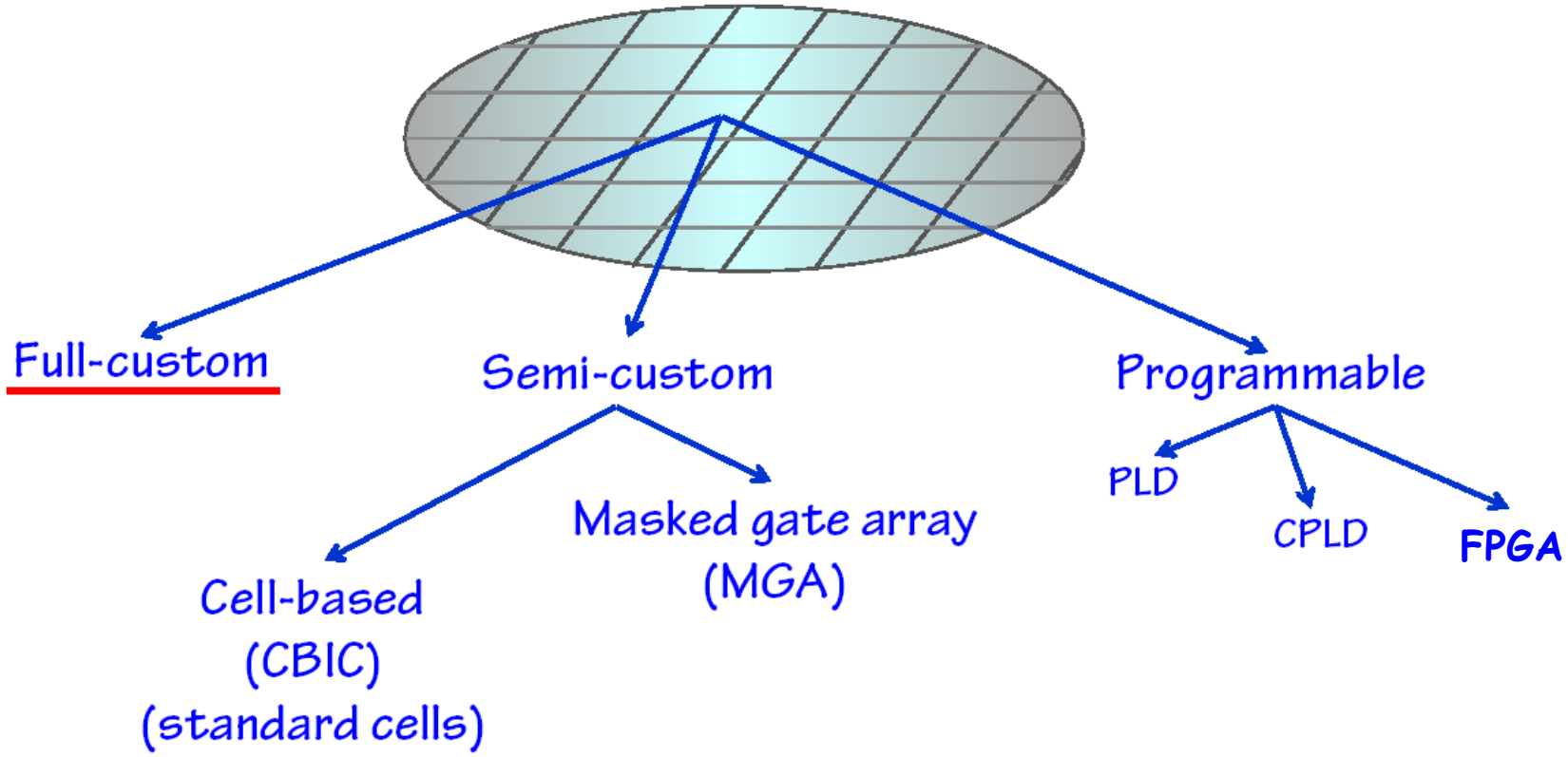


2-input MUX

DFF

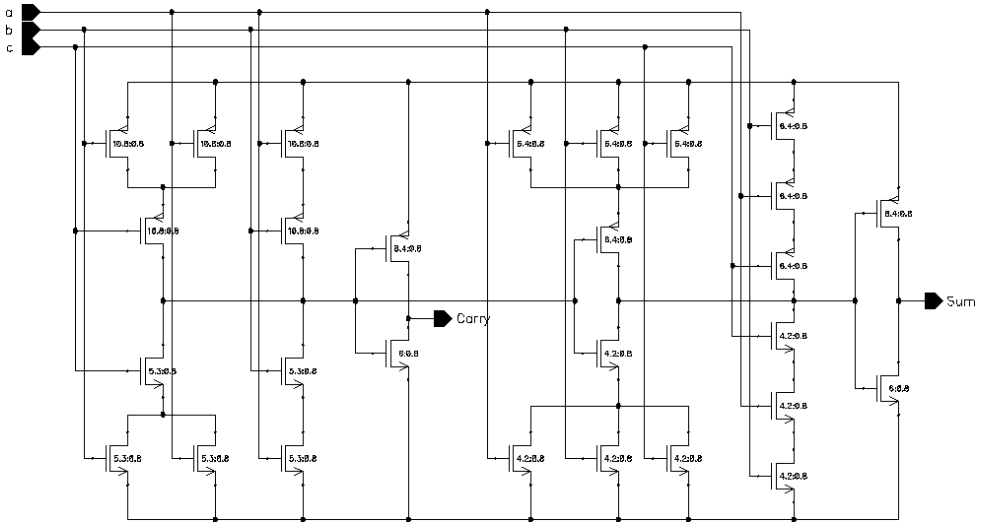


VLSI Design Styles

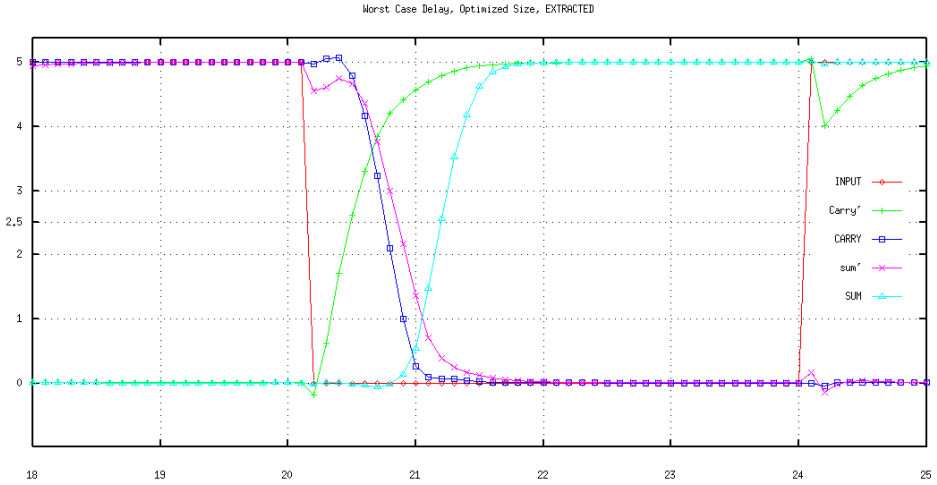


Full Custom Design

Following the partitioning, the transistor level design of the building block is generated and simulated.



The example shows a 1-bit full-adder schematic and its SPICE simulation results.



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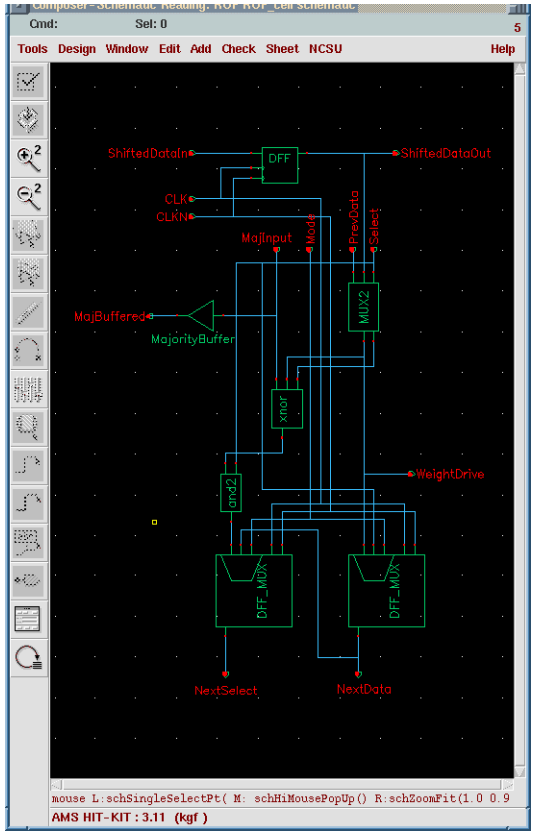
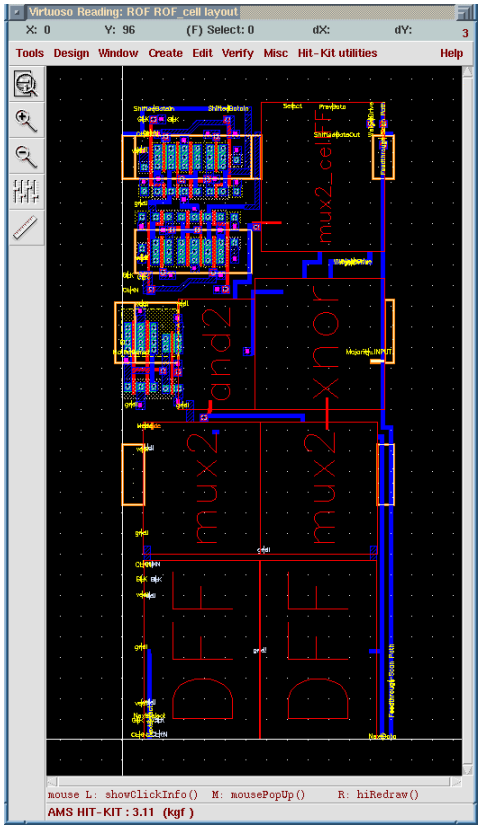
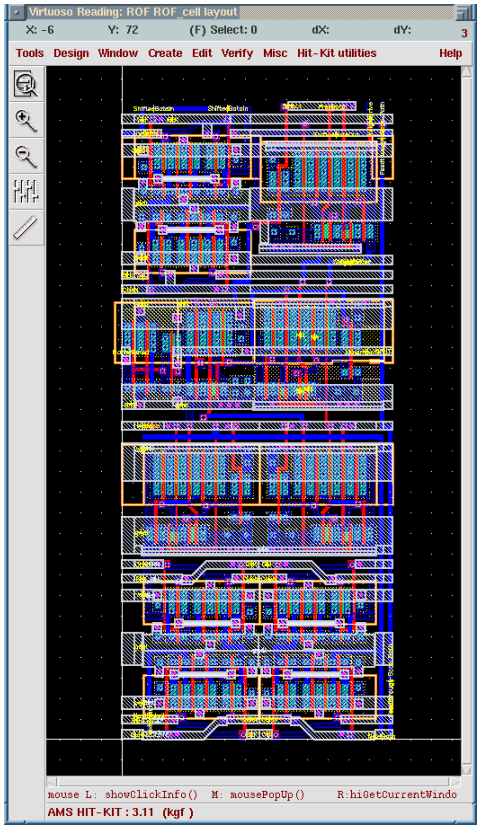
Full Custom Design

The main objective of full custom design is to ensure fine-grained regularity and modularity.







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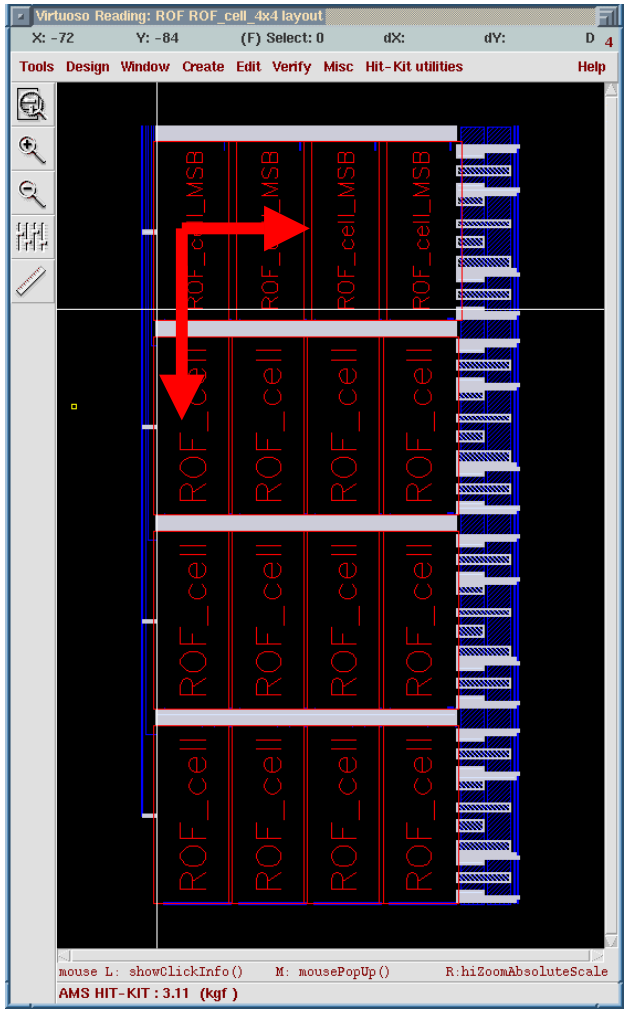
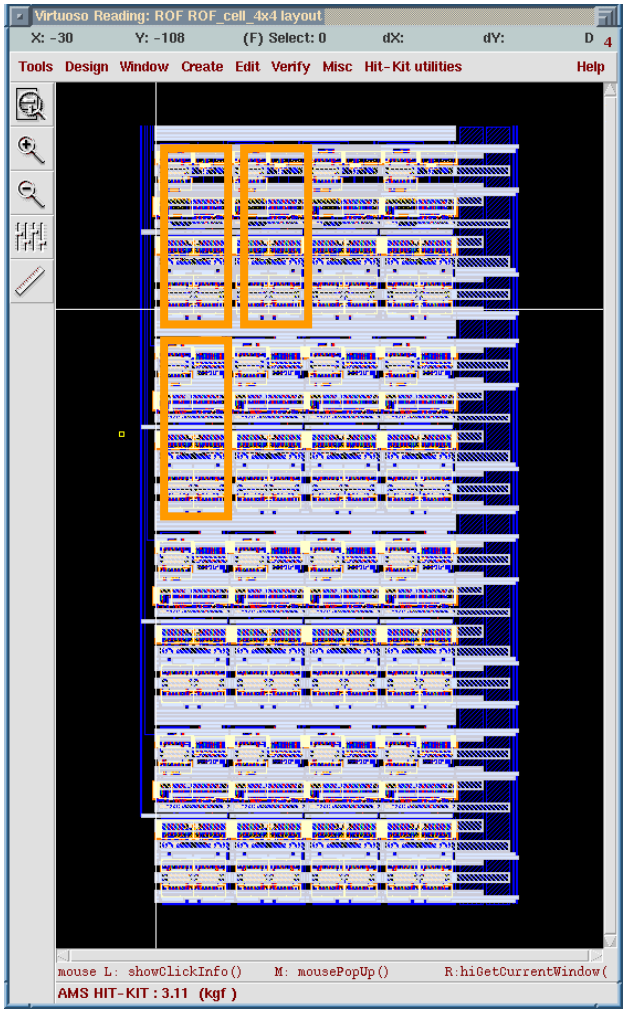
Full Custom Design



A carefully crafted full custom block can be placed both along the X and Y axis to form an interconnected two-dimensional array.

Example:

Data-path cells



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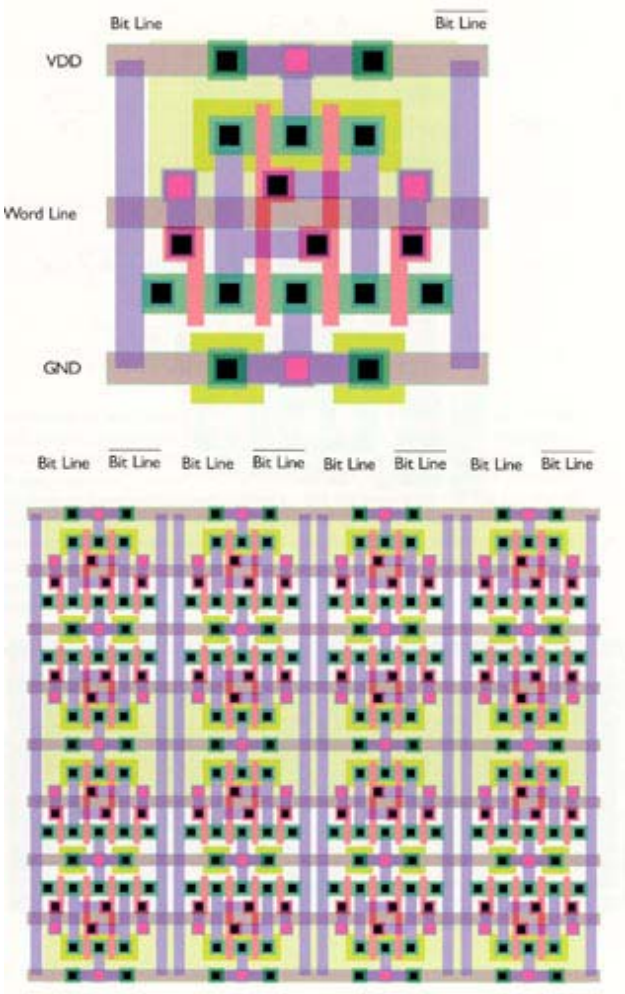
Full Custom SRAM Cell Design



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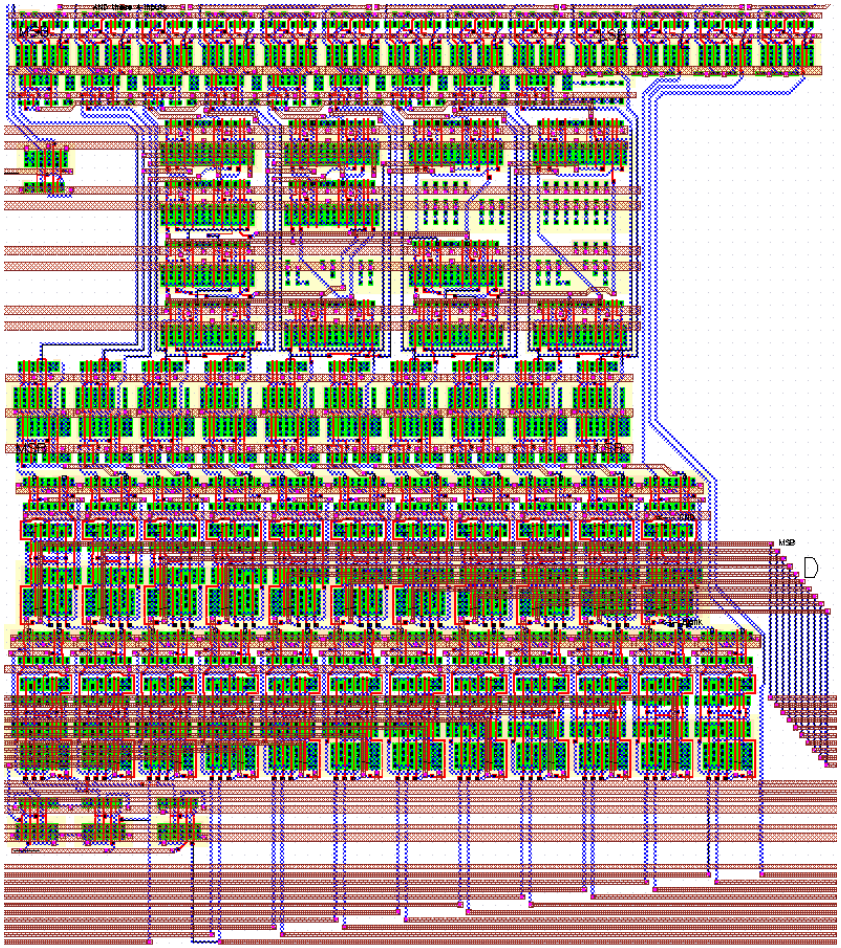
Mapping the Design into Layout



Manual full-custom design can be very challenging and time consuming, especially if the low level regularity is not well defined !

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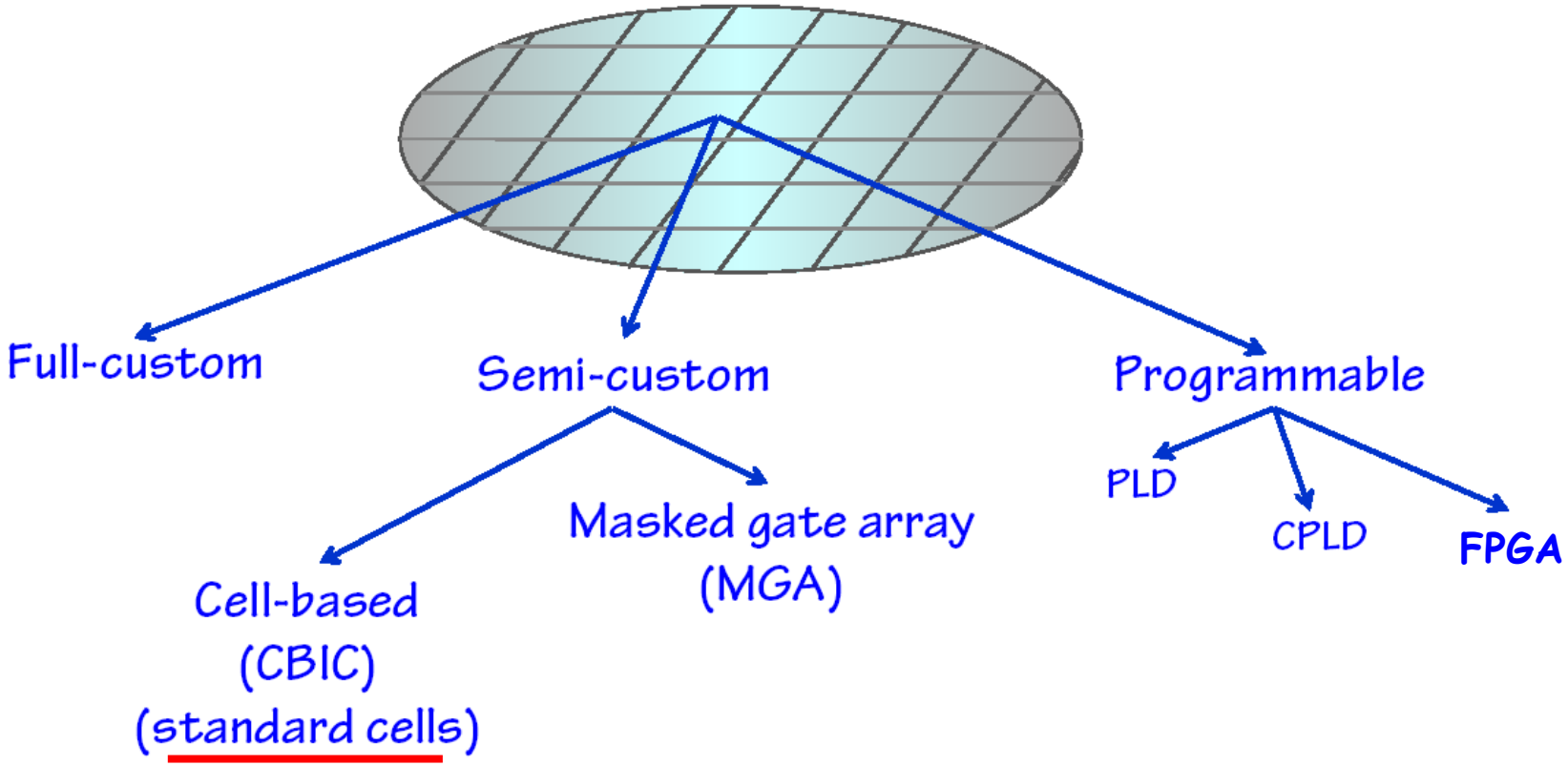
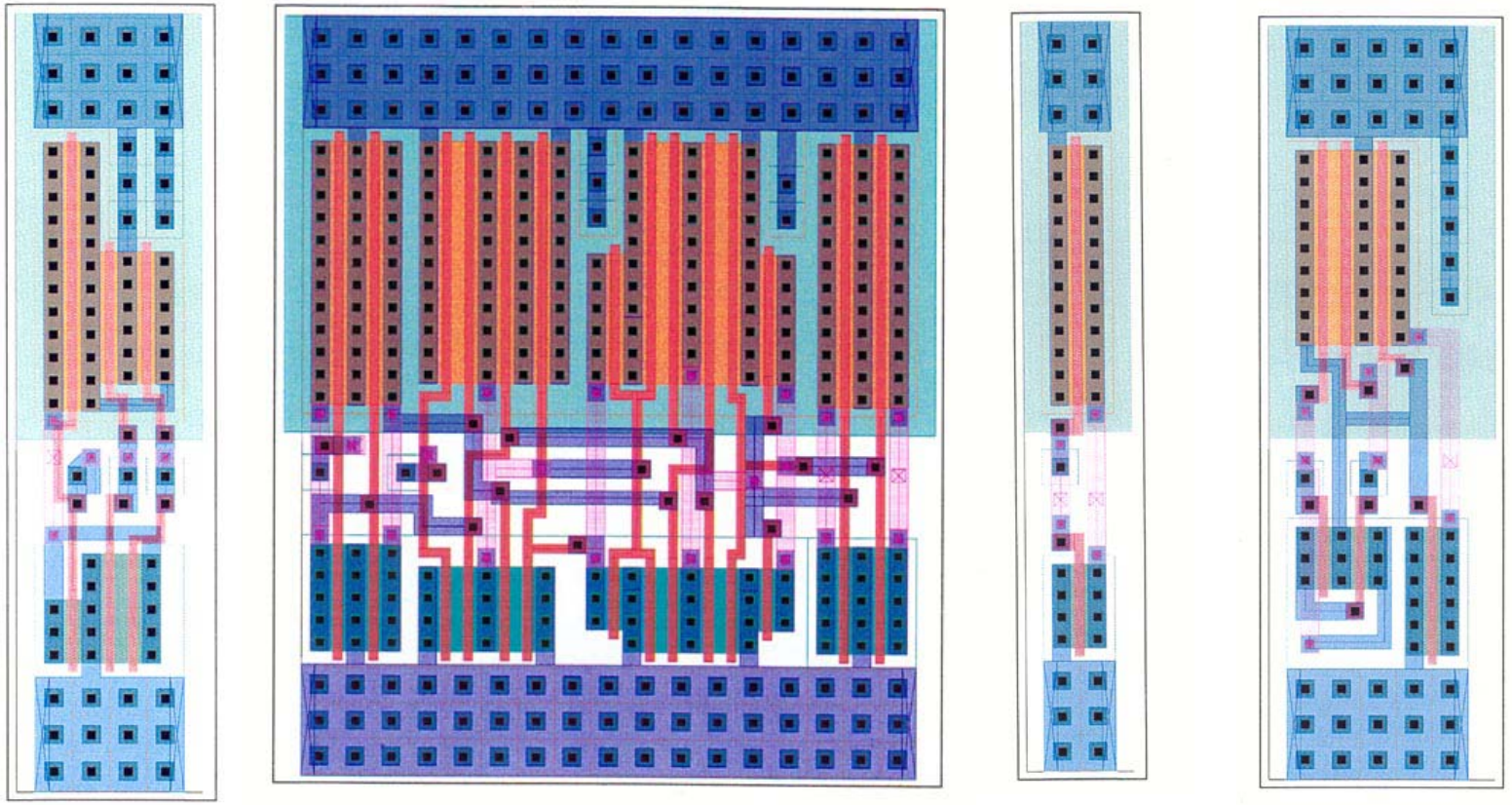
VLSI Design Styles



Standard Cells



AND DFF INV XOR

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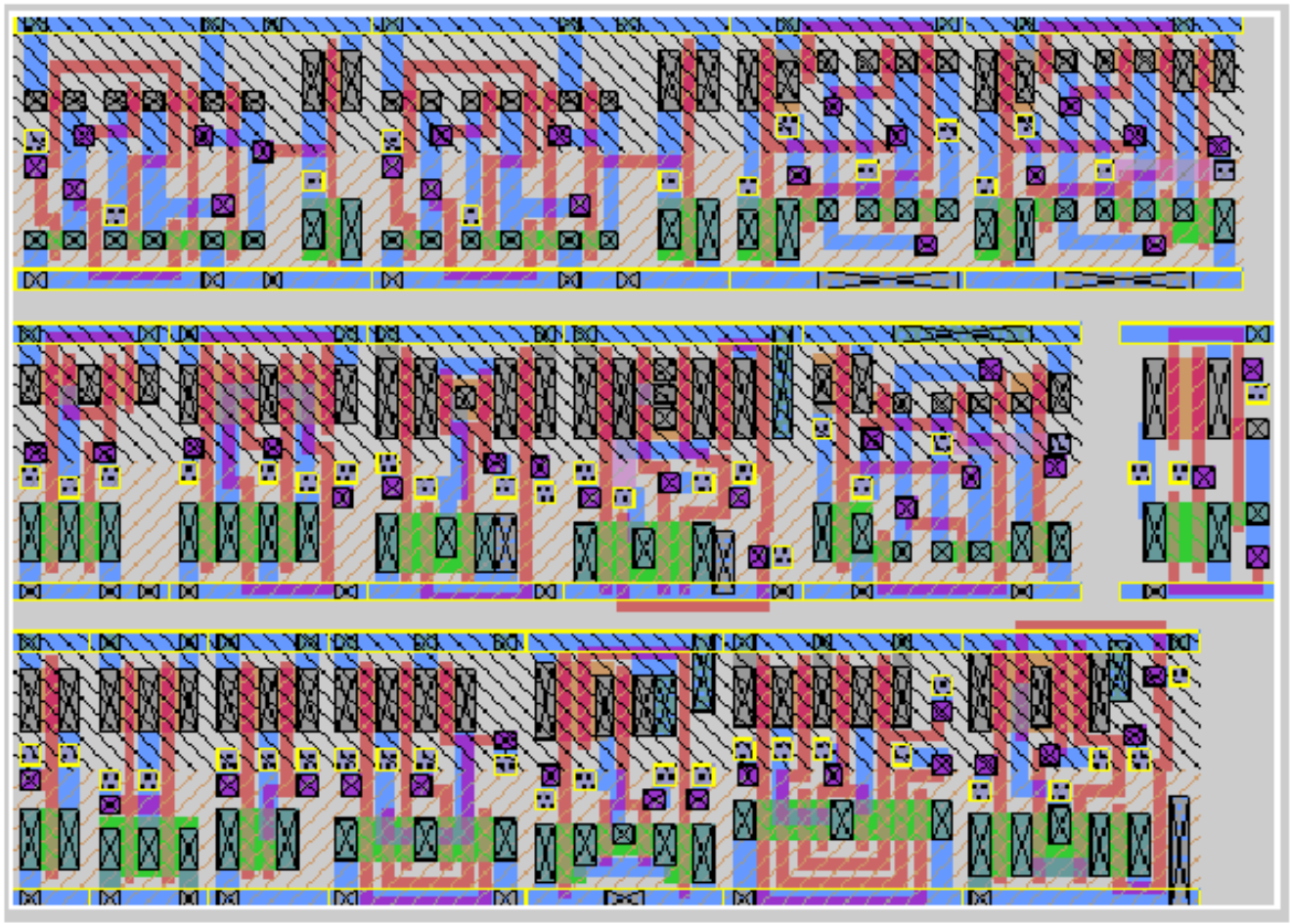
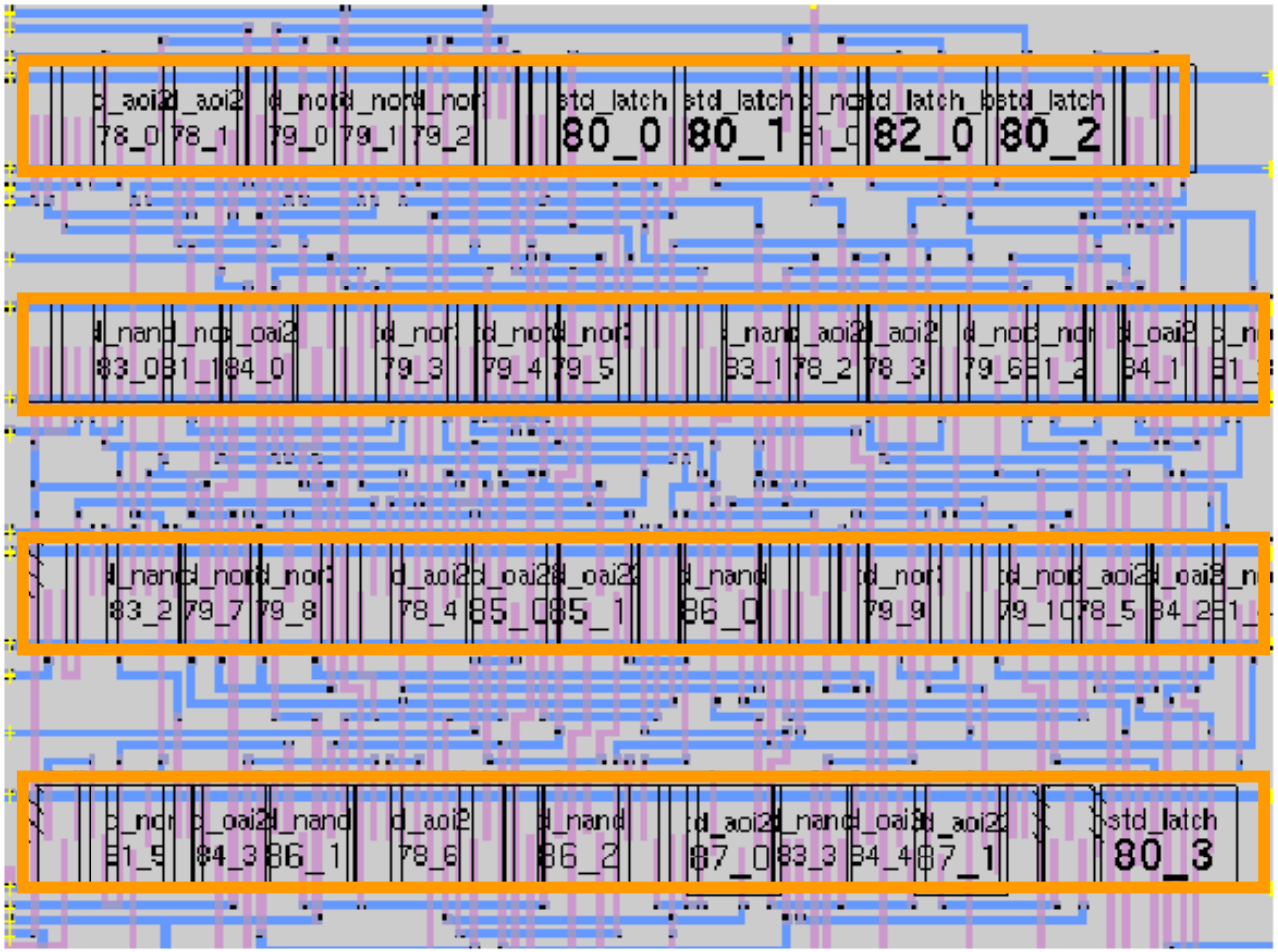
Standard Cells



Standard Cells



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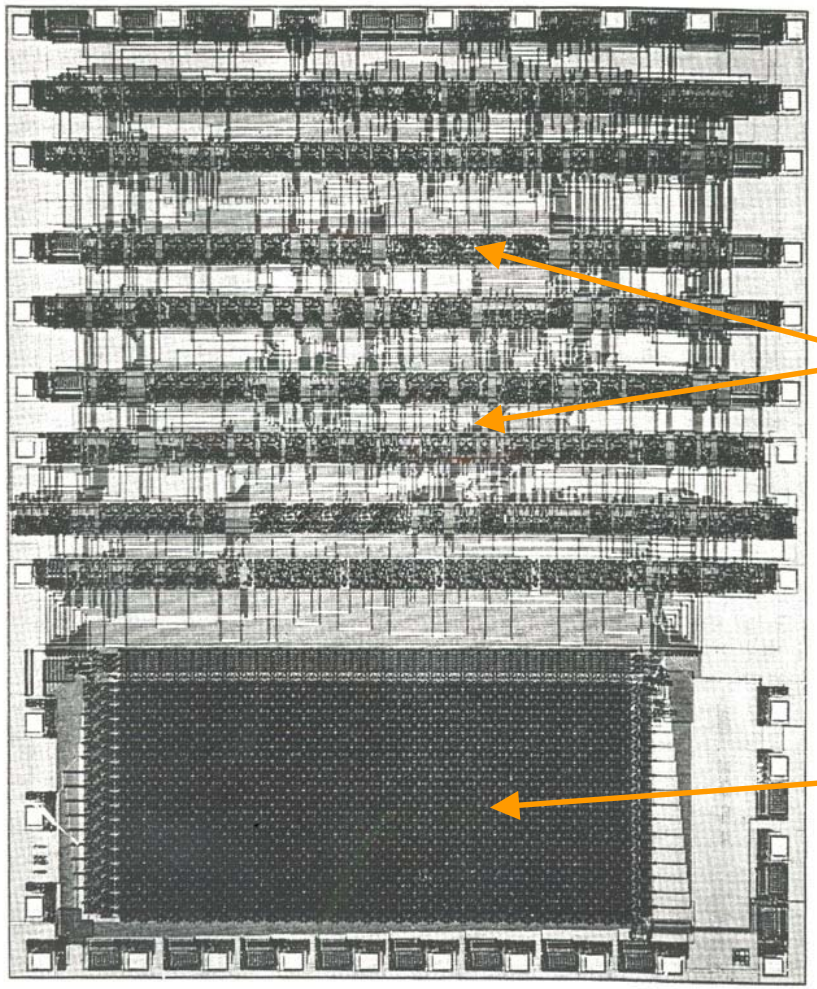
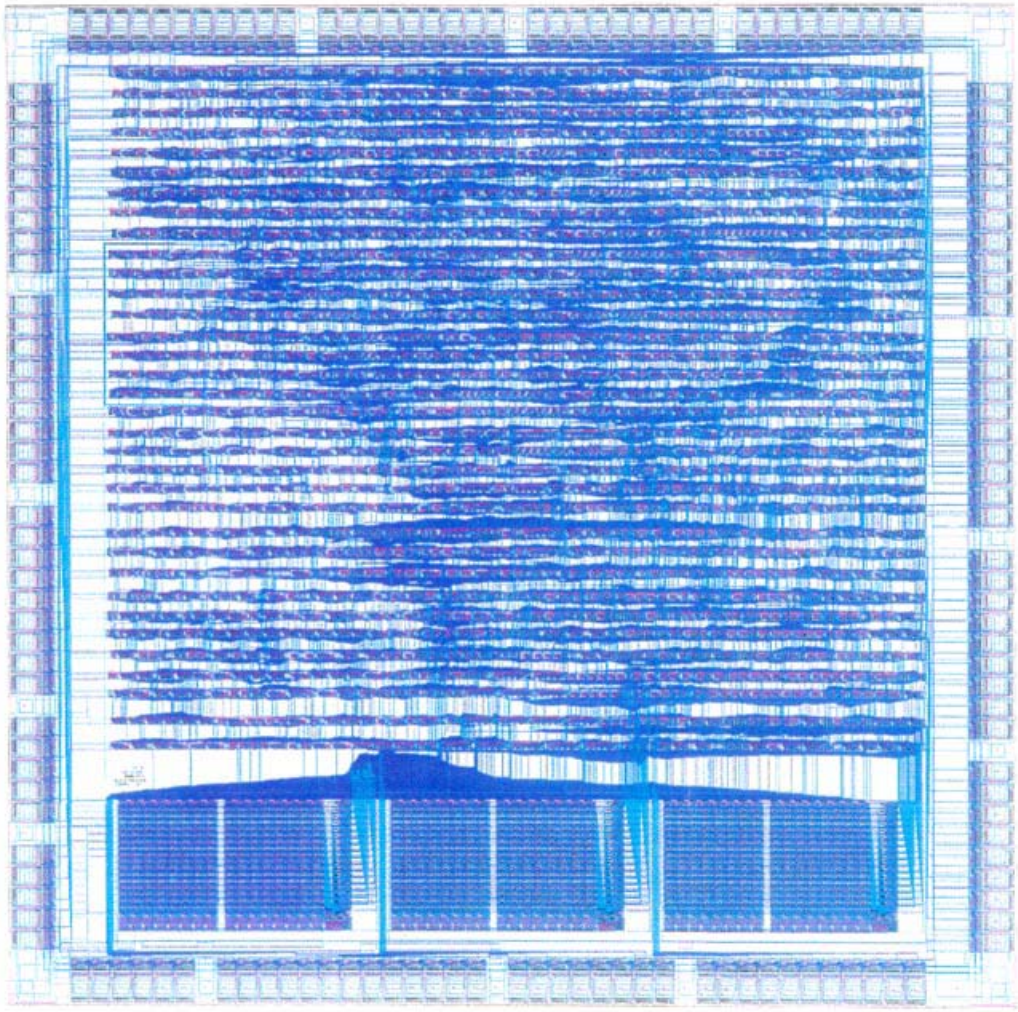
Standard Cells



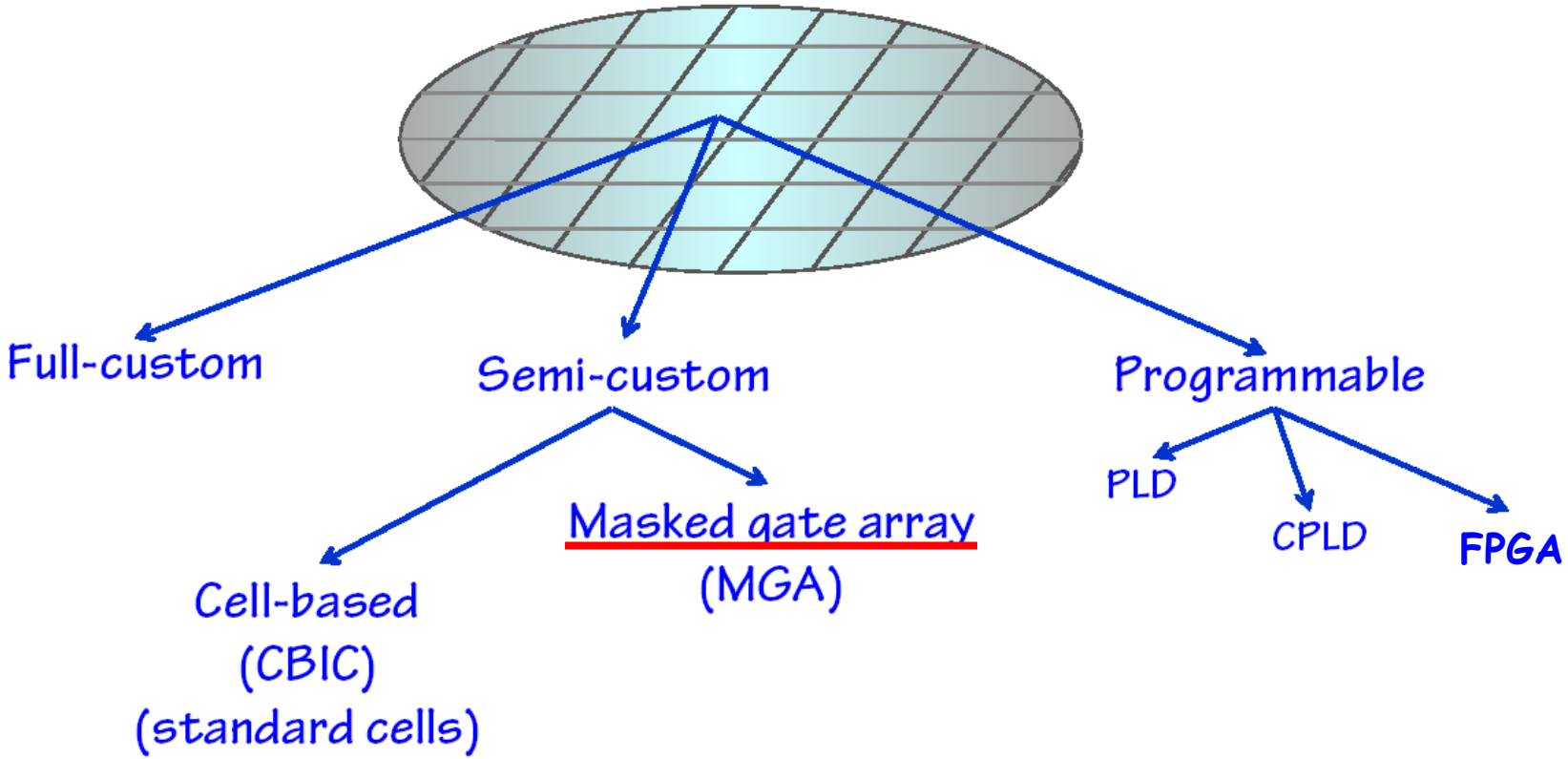
Rows of standard cells with routing channels between them

Memory array

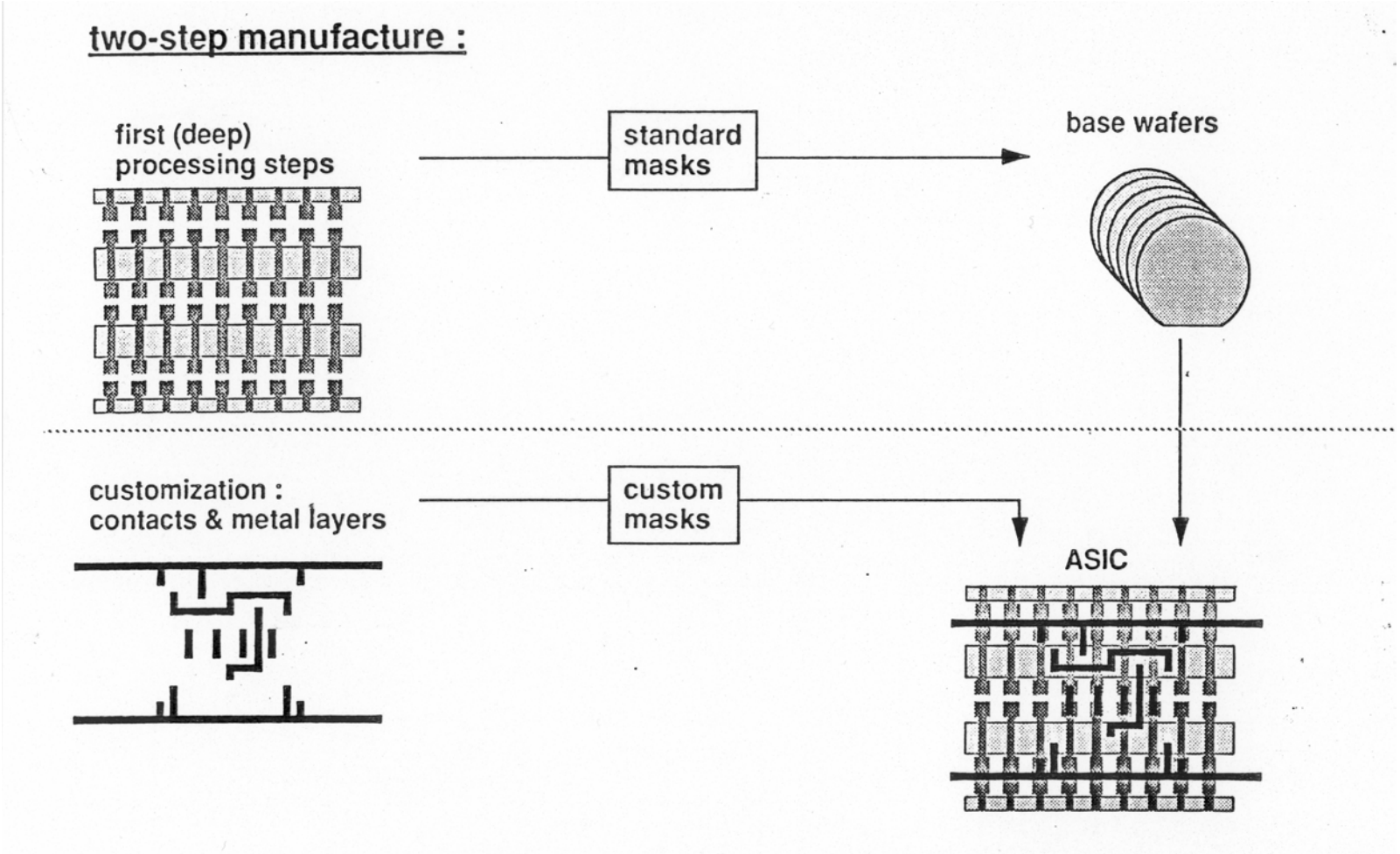
Standard Cells



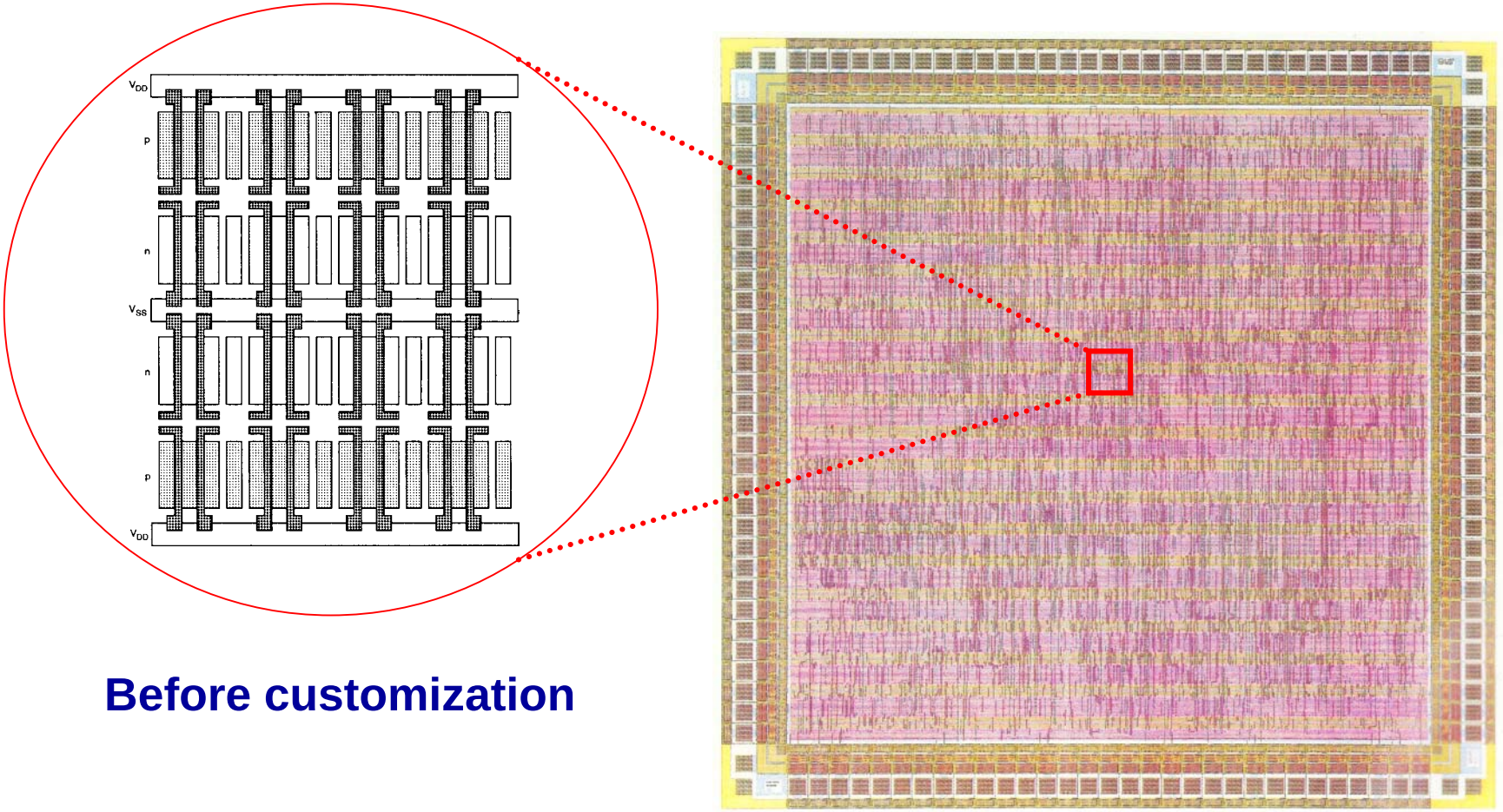
VLSI Design Styles



Mask Gate Array



Mask Gate Array



Before customization

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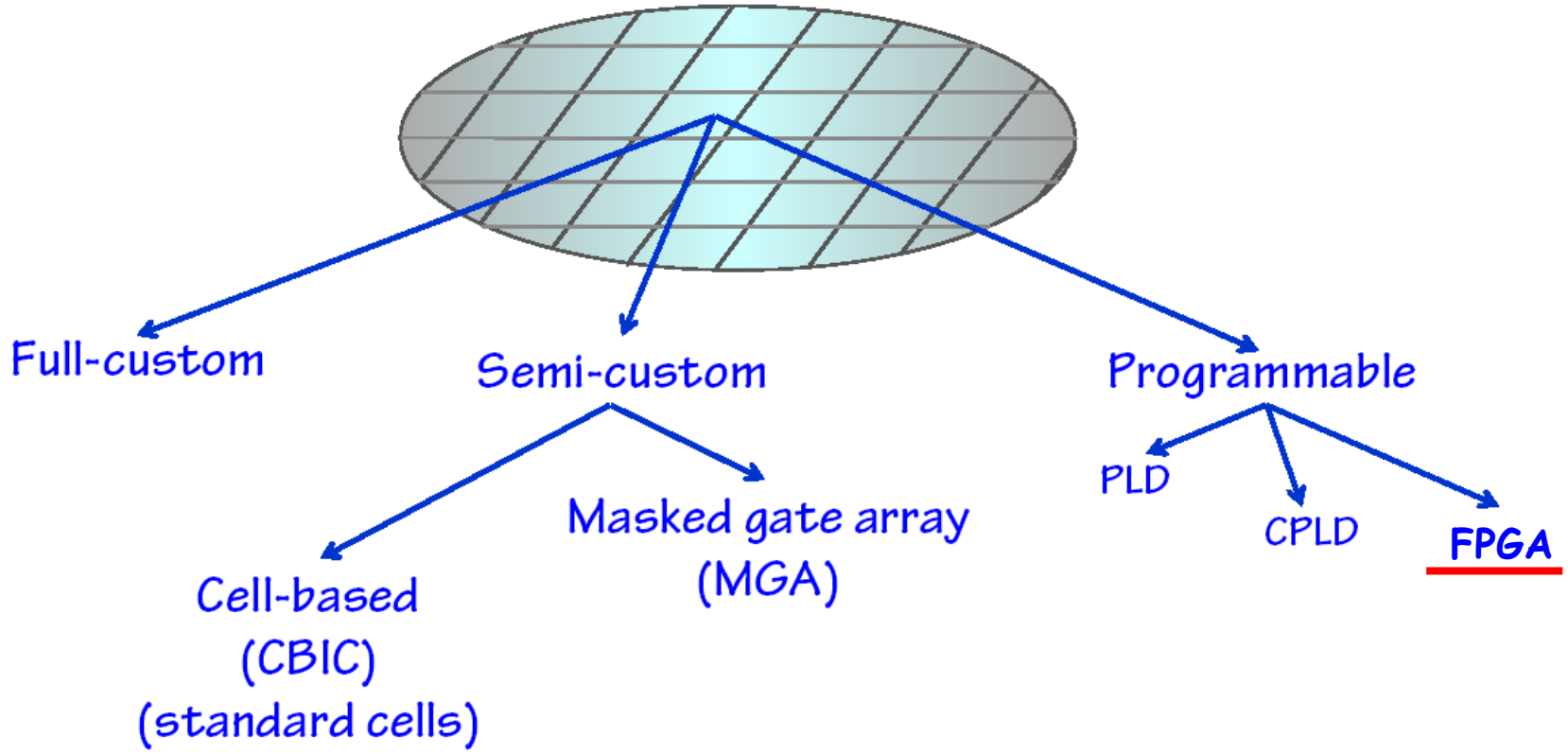
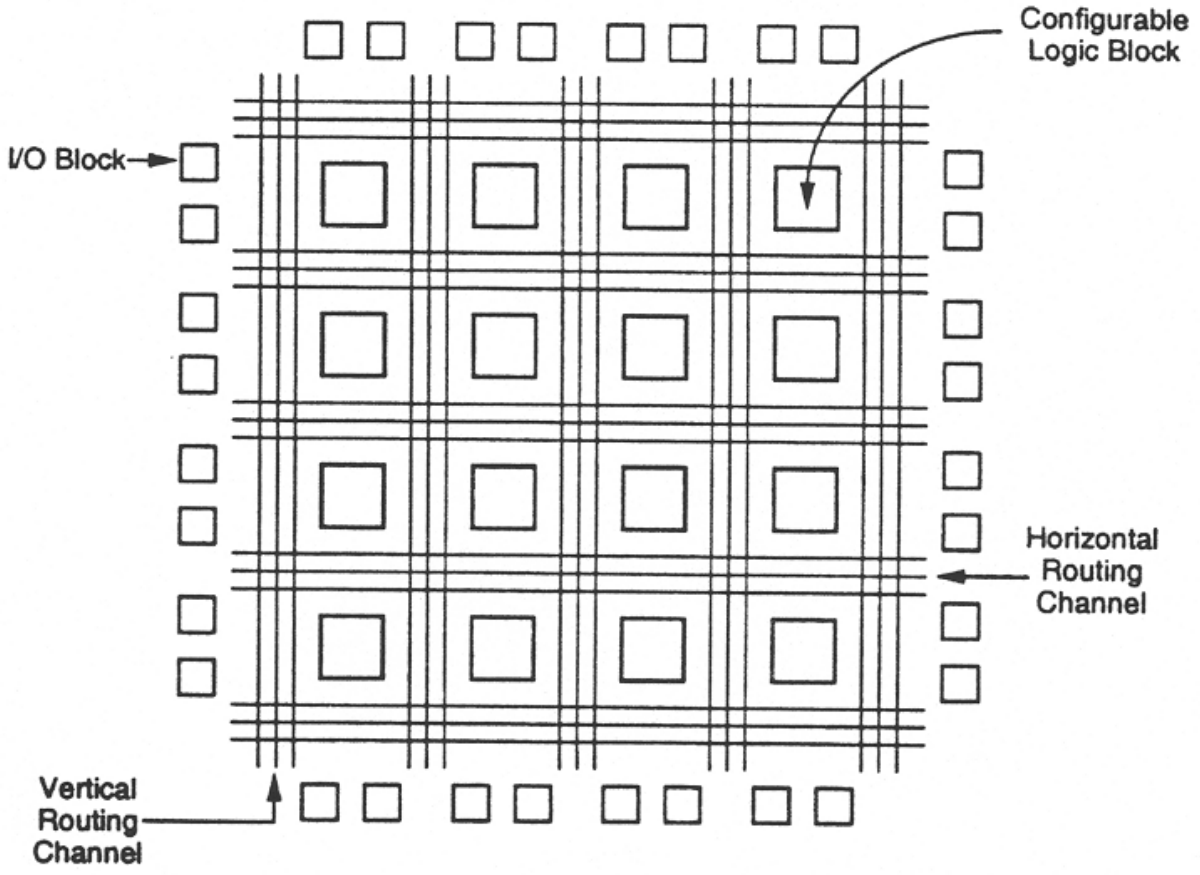
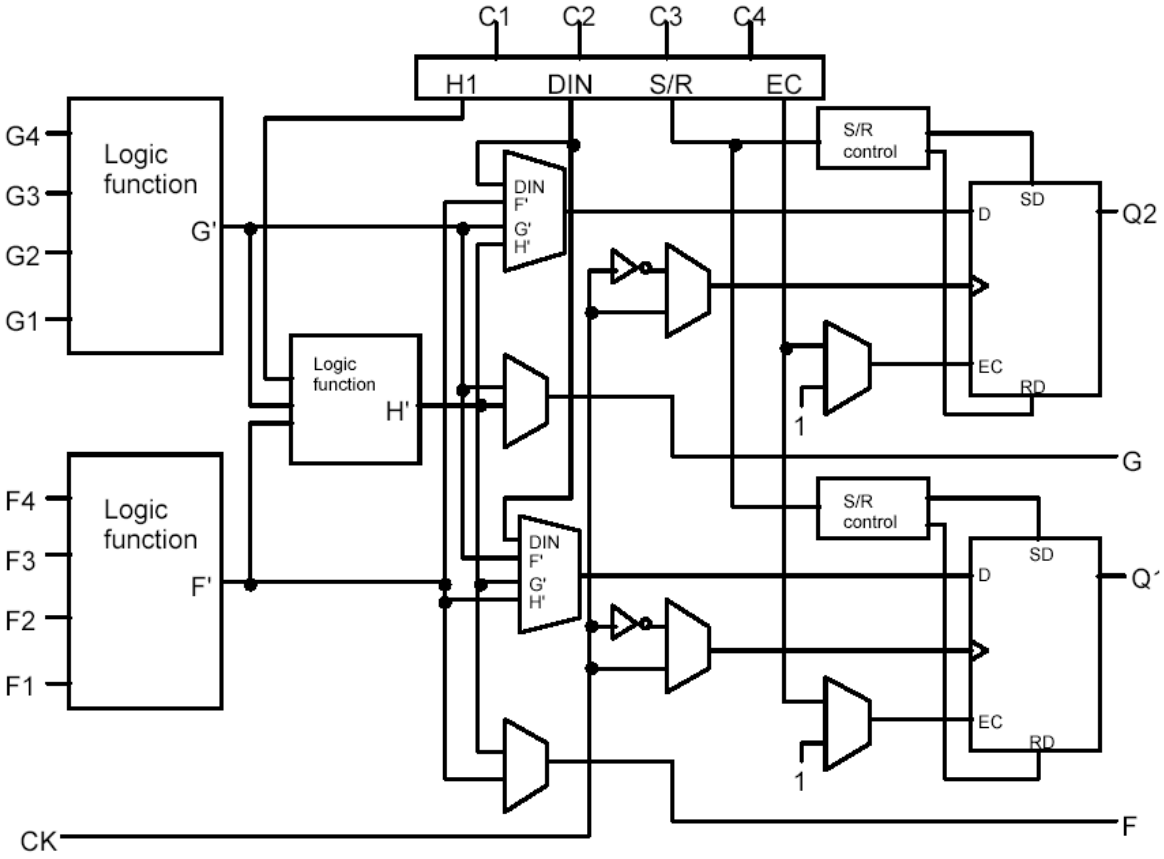
VLSI Design Styles



Field Programmable Gate Array



Field Programmable Gate Array



Internal structure of a CLB

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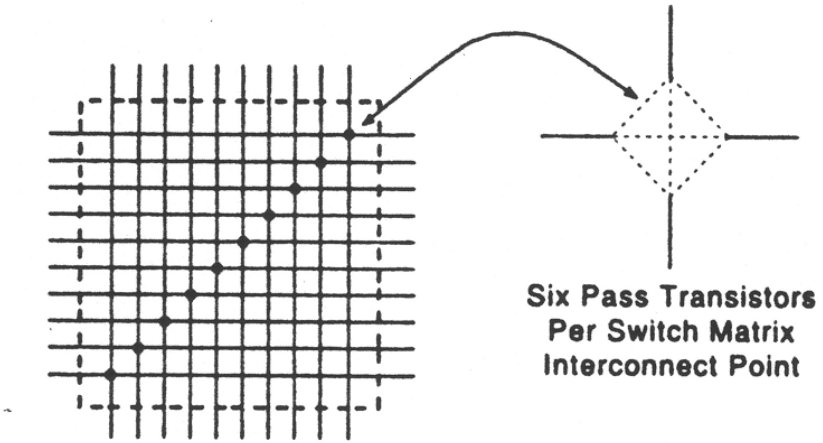
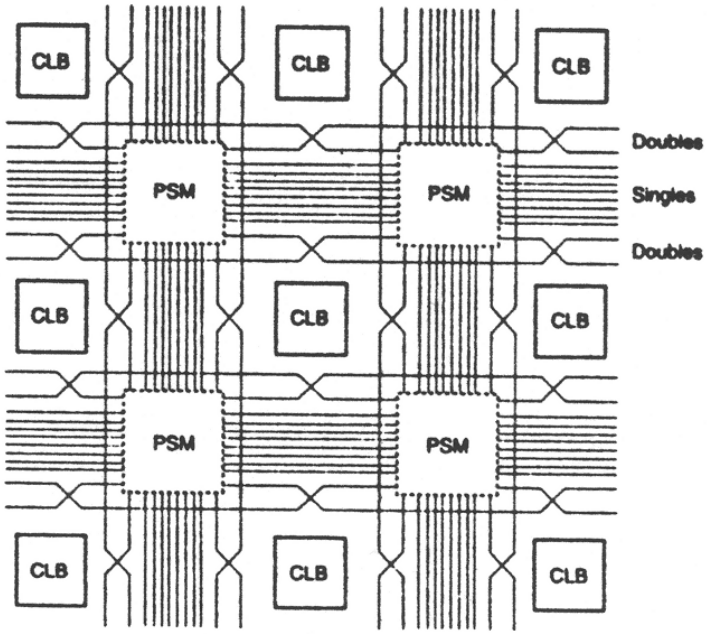
Field Programmable Gate Array





1.2 Objective and Organization of the Book

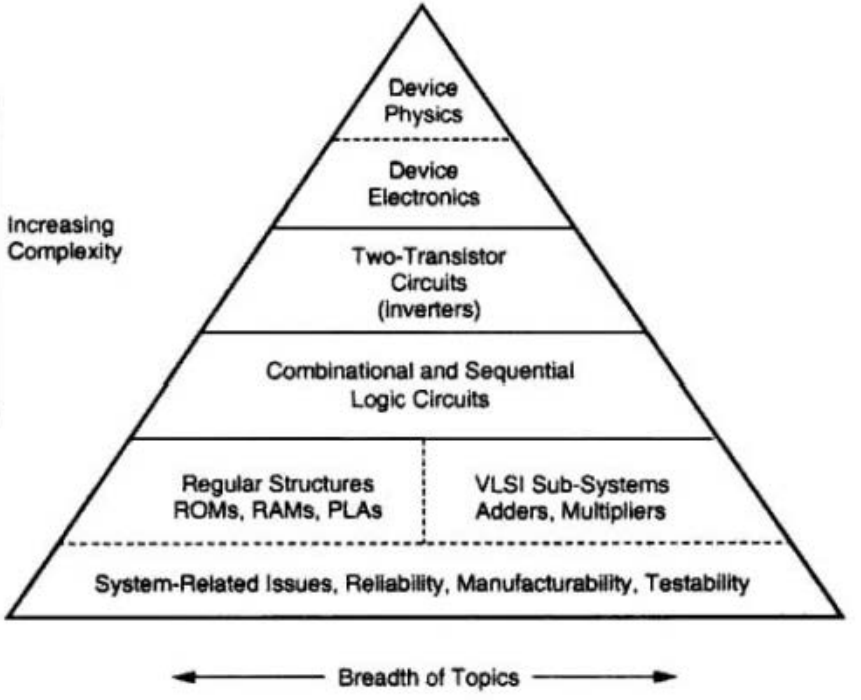


Figure 1.4. The ordering of topics covered in a typical digital integrated circuits course.

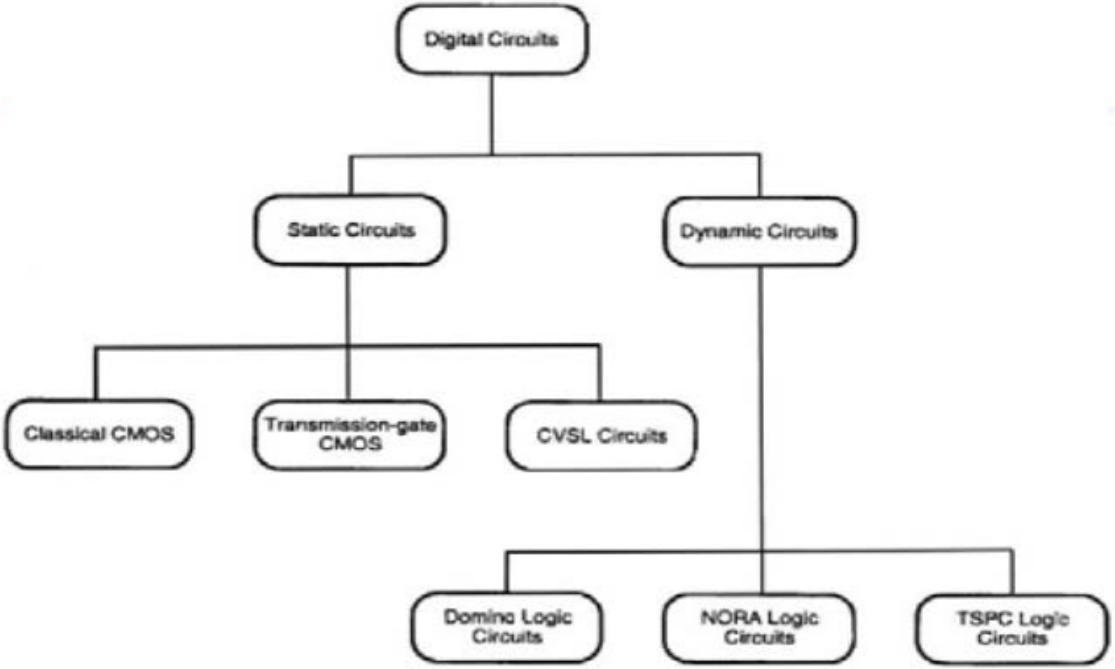


Figure 1.5. Classification of CMOS digital circuit types.

CVSL: Cascade Voltage Switch Logic
NORA: NO RAce circuits
TSPC: True-Single Phase Clock

1.3 A Circuit Design Example

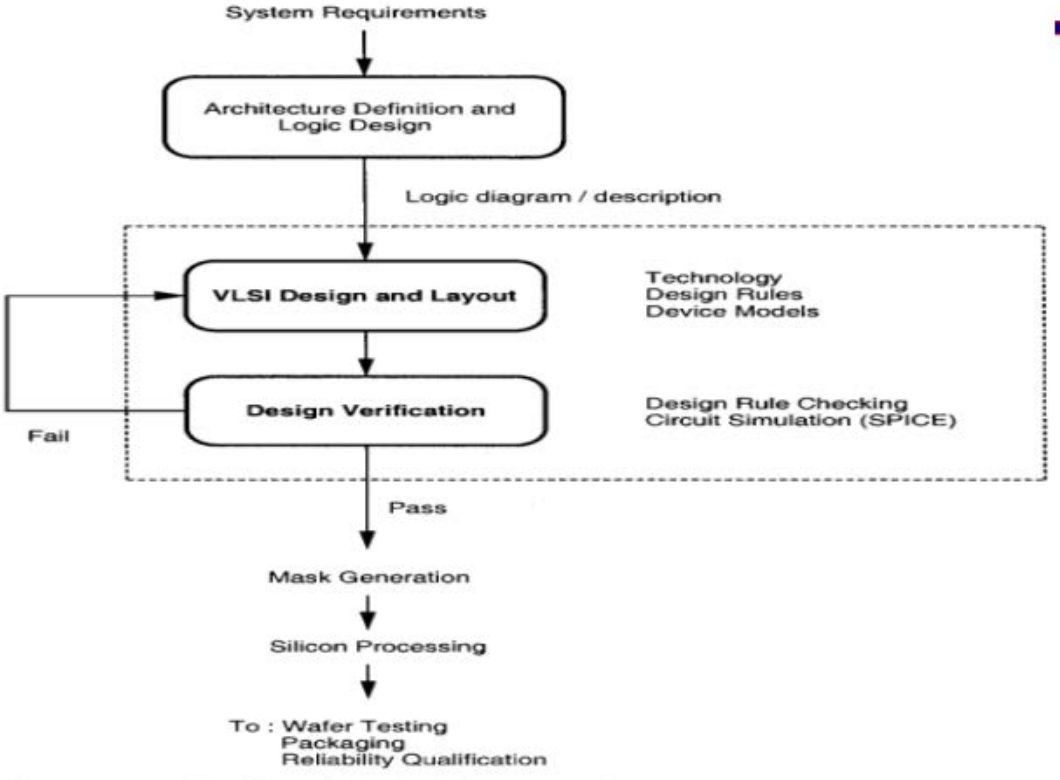
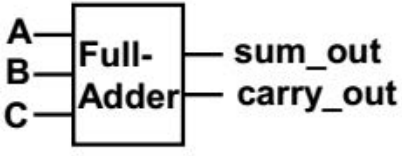


Figure 1.6 The flow of circuit design procedures.

One-bit Full-Adder Circuit Design:

Using 0.8um twin-well CMOS technology with specification:

1) Propagation delay times of sum and carry-out signals <1.2ns (worst)
2) Transition delay times of sum- and carry-out signals < 1.2ns (worst)
3) Circuit area < 1500 μm^2
4) Dynamic power dissipation (@V_{DD} = 5V and f_{max} = 20MHz) < 1mW



$$Sum\_out = A \oplus B \oplus C = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

$$Carry\_out = AB + AC + BC$$

$$Sum\_out = ABC + (A+B+C)carry\_out$$

A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

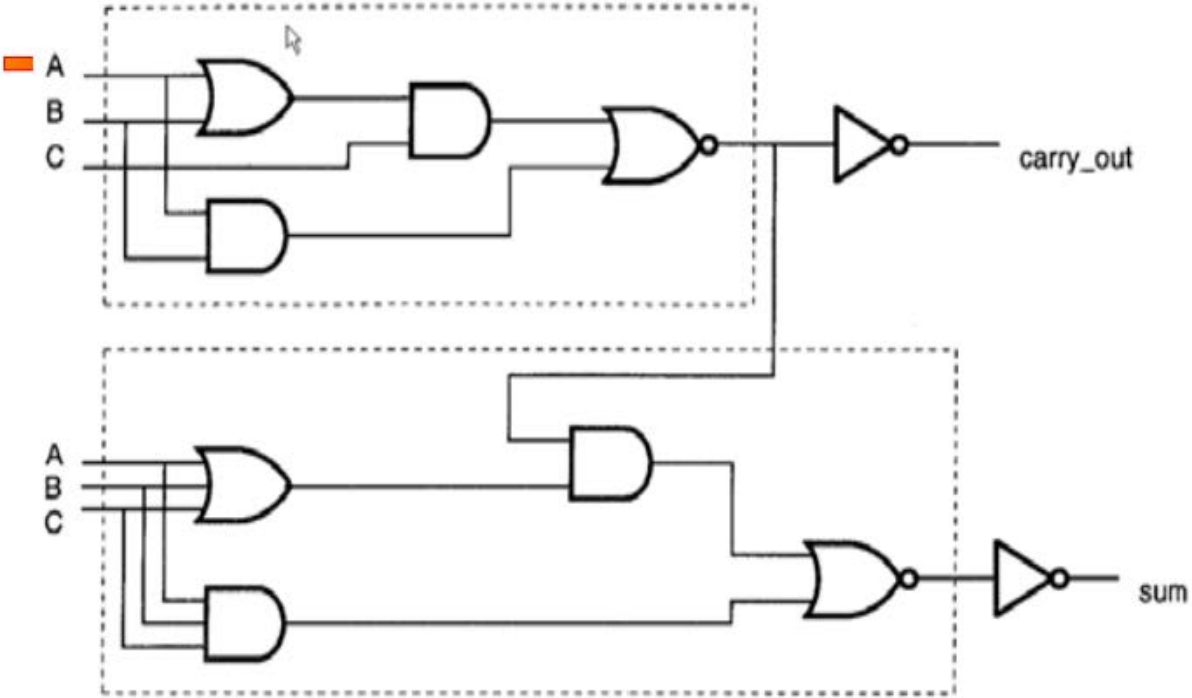


Figure 1.7 Gate-level schematic of the one-bit full-adder circuit.

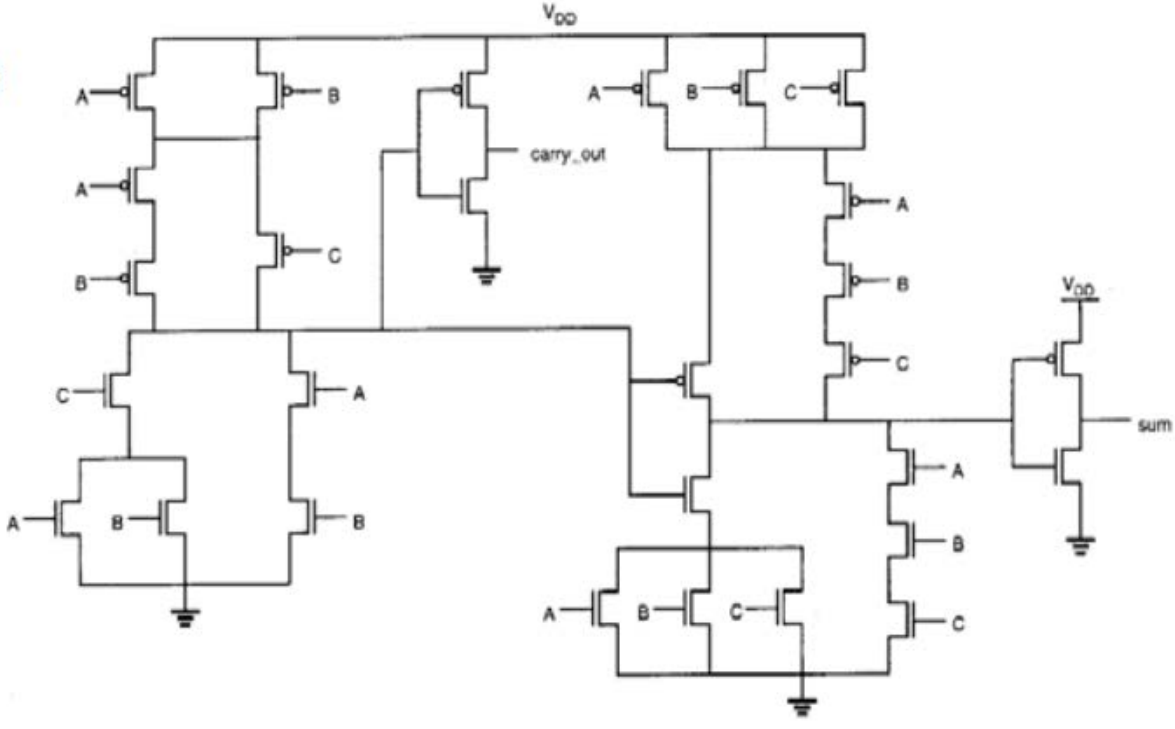


Figure 1.8 Transistor-level schematic of the one-bit full-adder circuit.

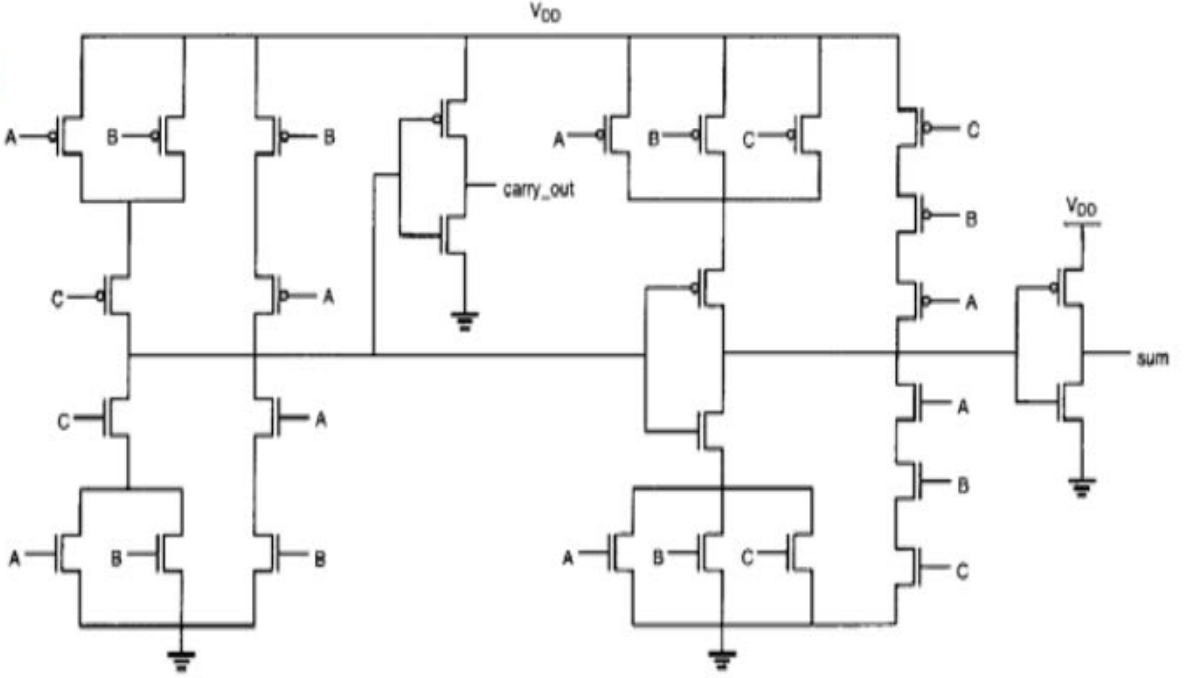


Figure 1.9 Alternate transistor-level schematic of the one-bit full-adder circuit (note that the nMOS and pMOS networks are completely symmetric).

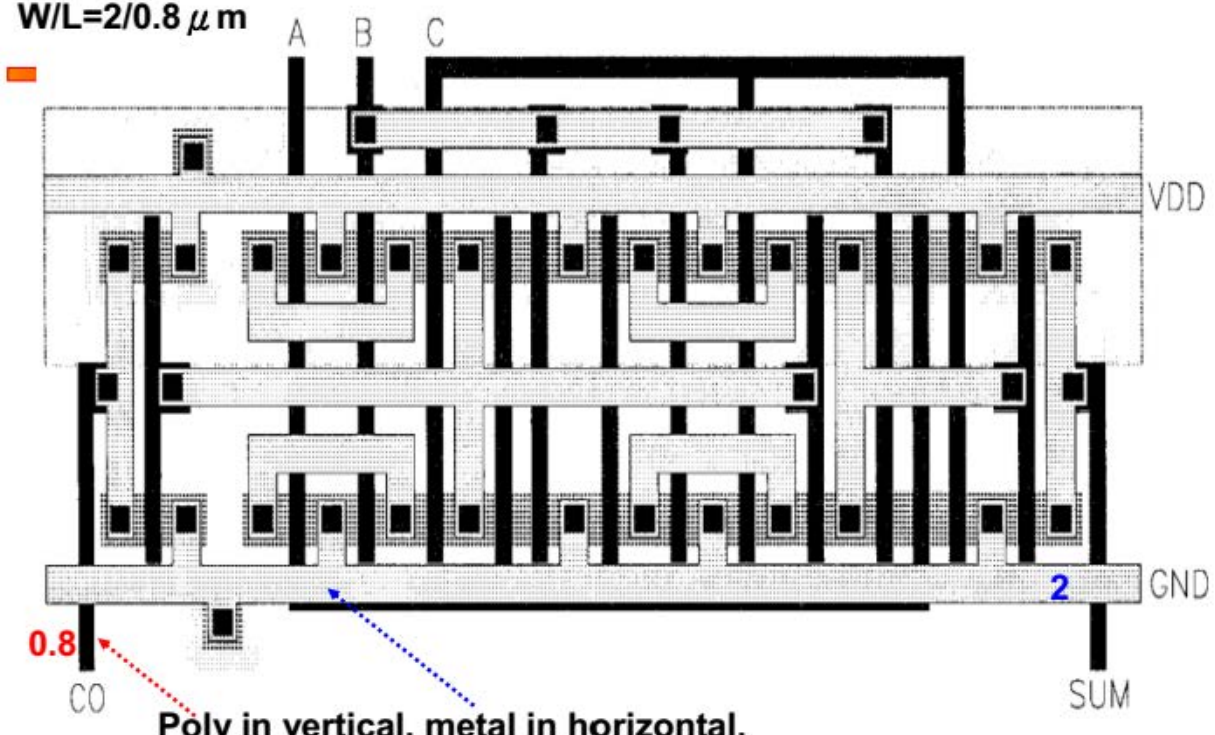


Figure 1.10 Initial layout of the full-adder circuit using minimum-size transistors.

Area = 21X54 um² = 1134 um²

SPICE simulation

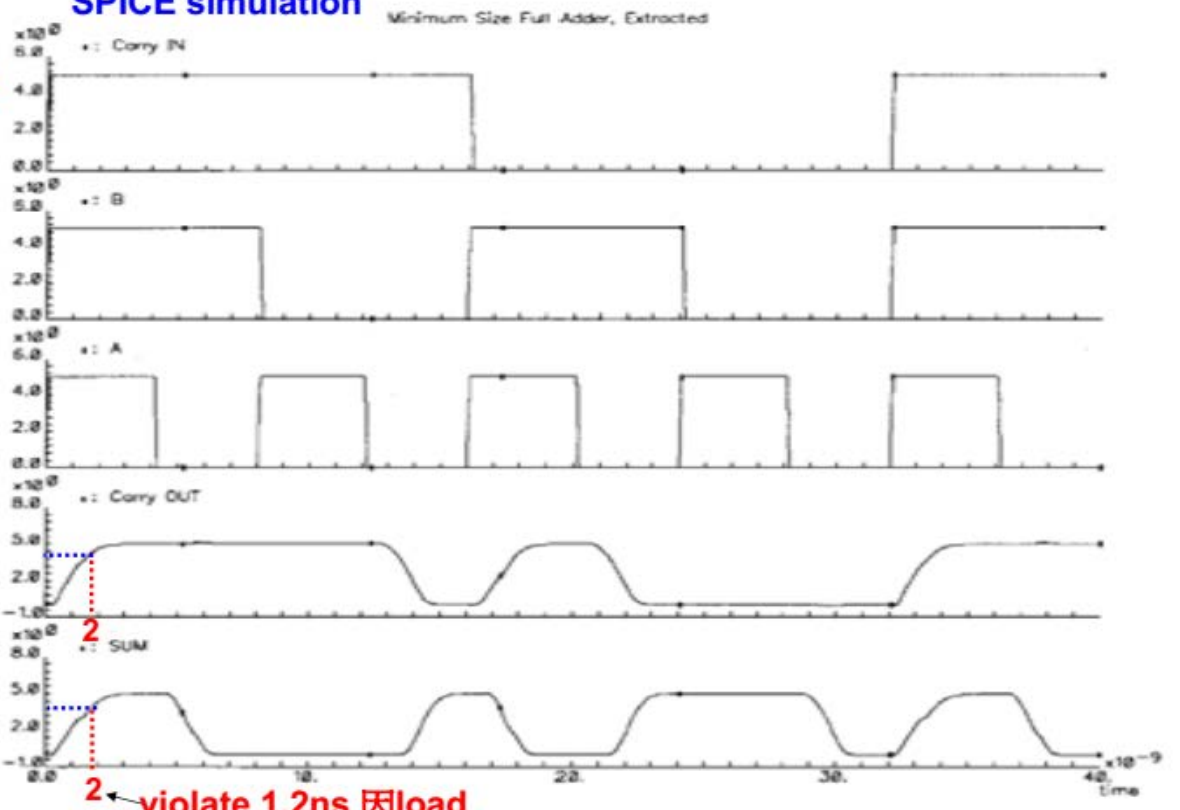


Figure 1.11 Simulated input and output waveforms of the full-adder circuit.

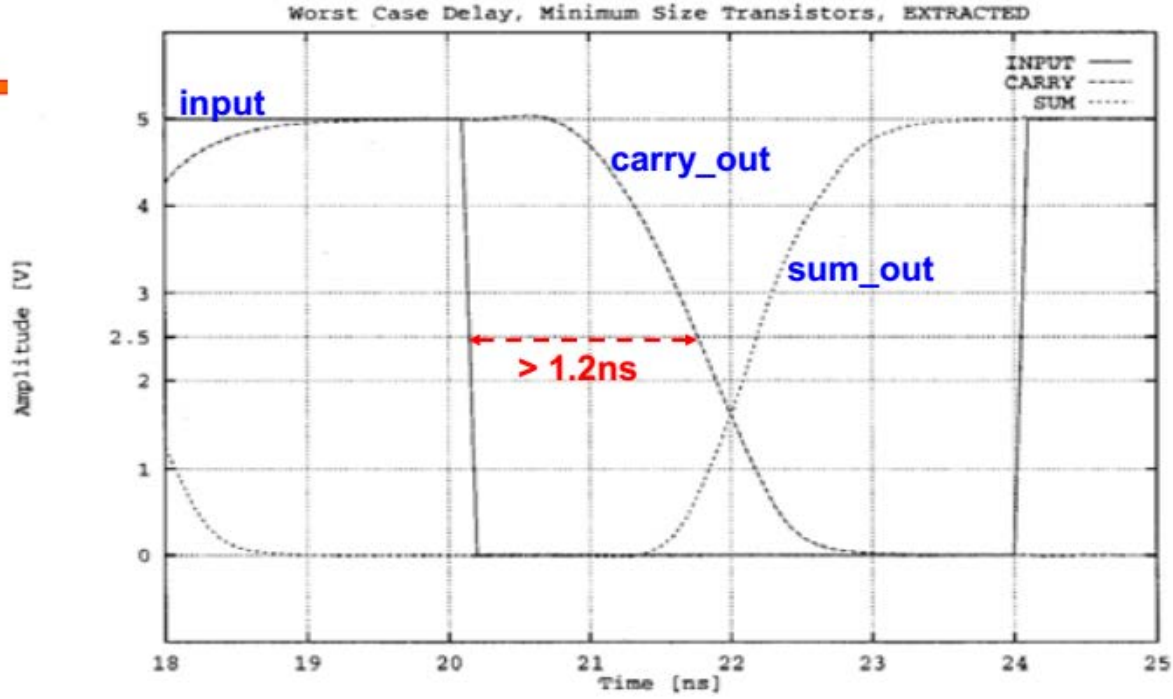
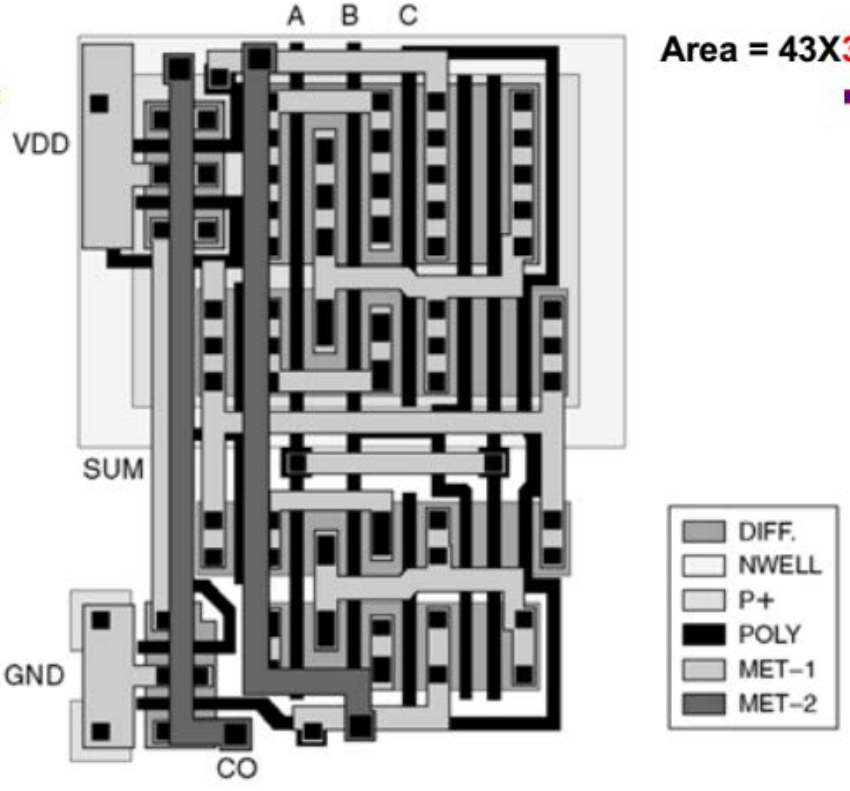


Figure 1.12 Simulated output waveforms of the full adder circuit with minimum transistor dimensions, showing the signal propagation delay during one of the worst-case transitions.



Area = 43X30 um² = 1290 um²

Figure 1.13 Modified layout of the full-adder circuit, with optimized transistor dimensions.

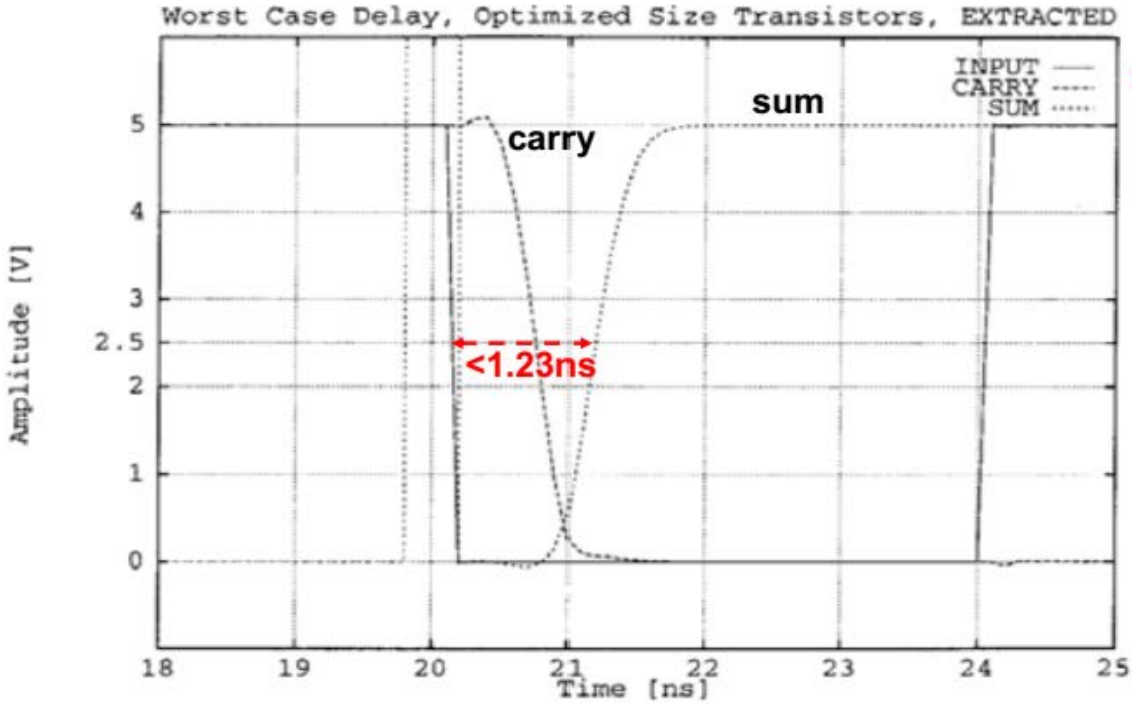


Figure 1.14 Simulated output waveforms of the full-adder circuit with optimized transistor dimensions, showing the signal propagation delay during the same worst-case transition. **Power dissipation = 460 μW**

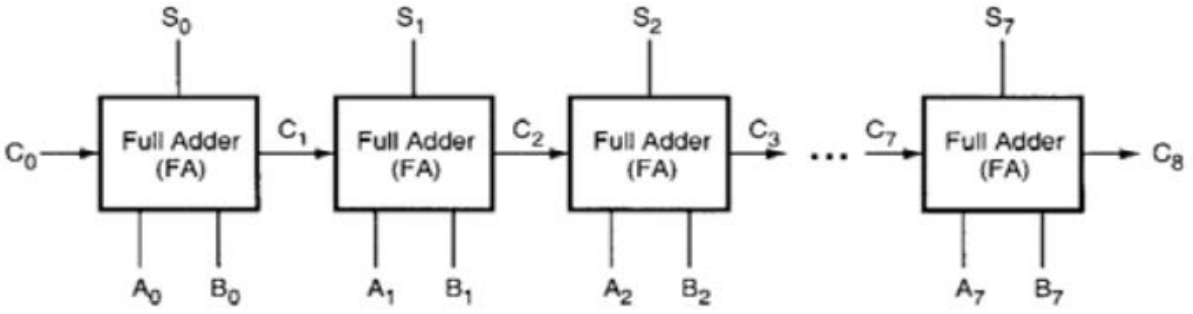


Figure 1.15 Block diagram of a carry ripple adder chain consisting of full adders.

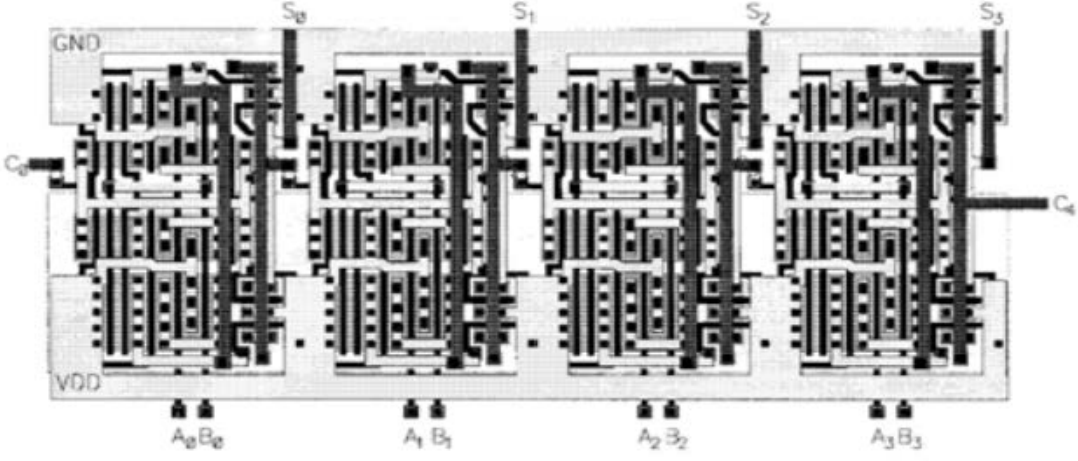


Figure 1.16 Mask layout of the 4-bit carry ripple adder array.

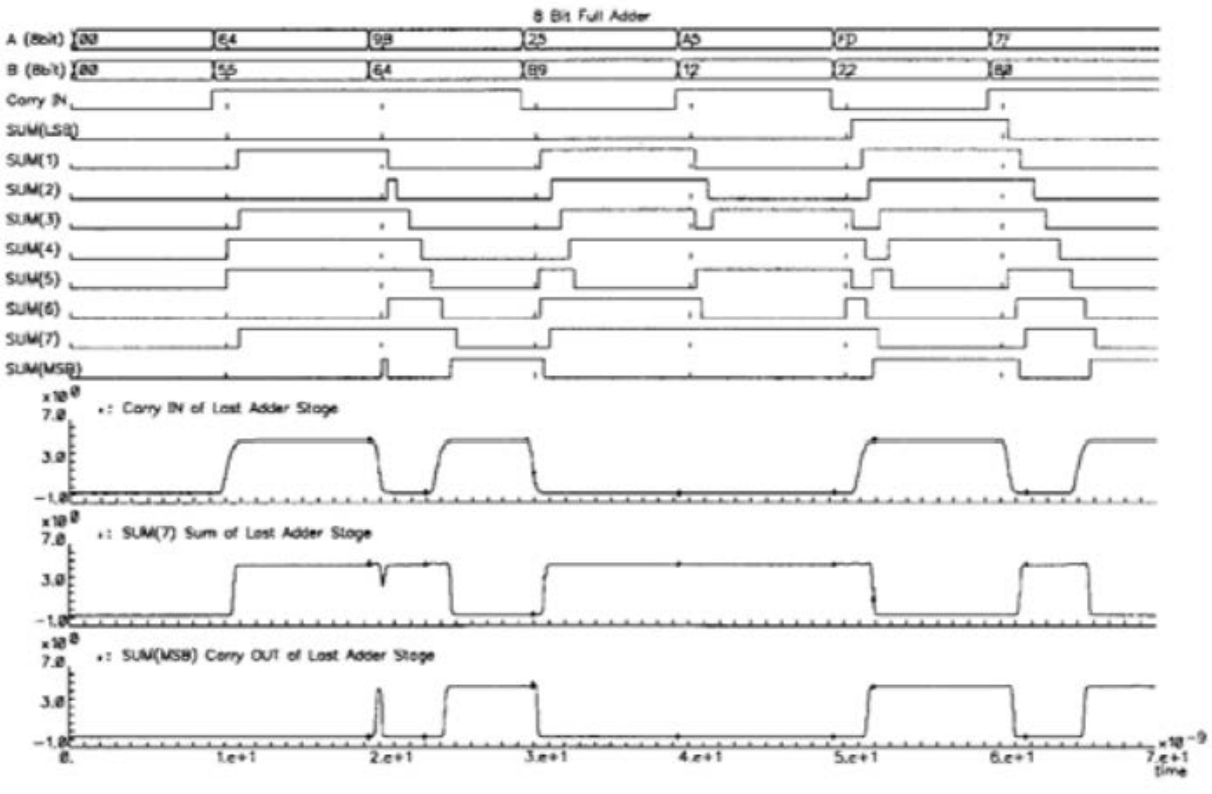


Figure 1.17 Simulated input and output waveforms of the 8-bit carry ripple adder circuit, showing a maximum signal propagation delay of about 7 ns.