



# FABRICATION OF CMOS INTEGRATED CIRCUITS

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# Outline

- ▣ Overview of CMOS Fabrication Processes
- ▣ The CMOS Fabrication Process Flow
- ▣ Design Rules

- ▣ Reference:

Uyemura, John P. "Introduction to VLSI circuits and systems." (2002).



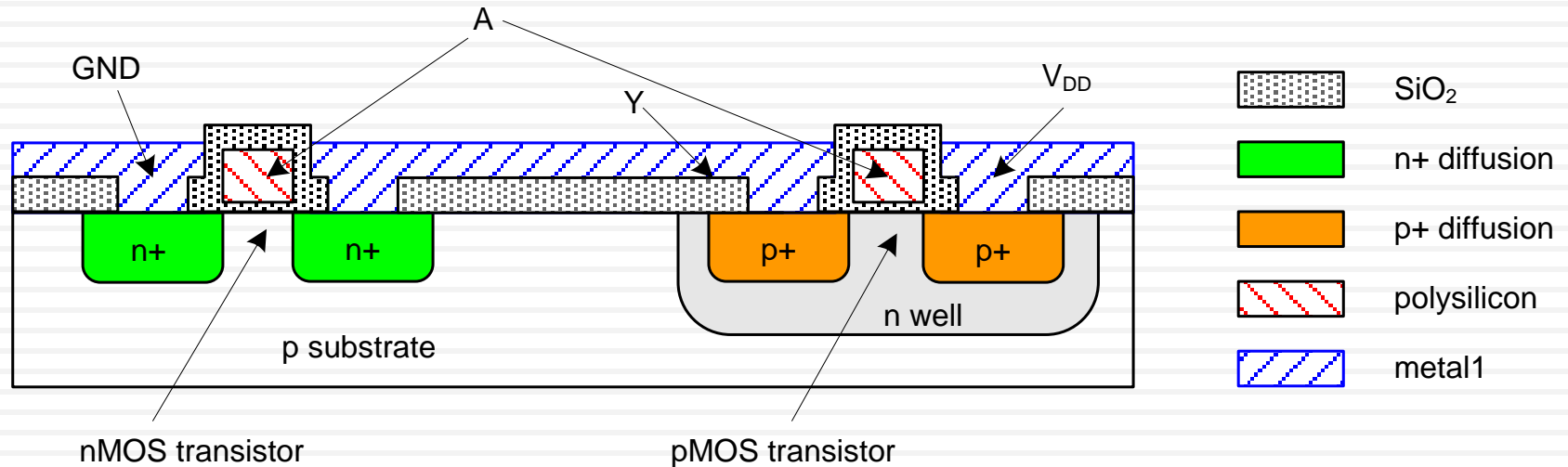
# CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process



# Inverter Cross-section

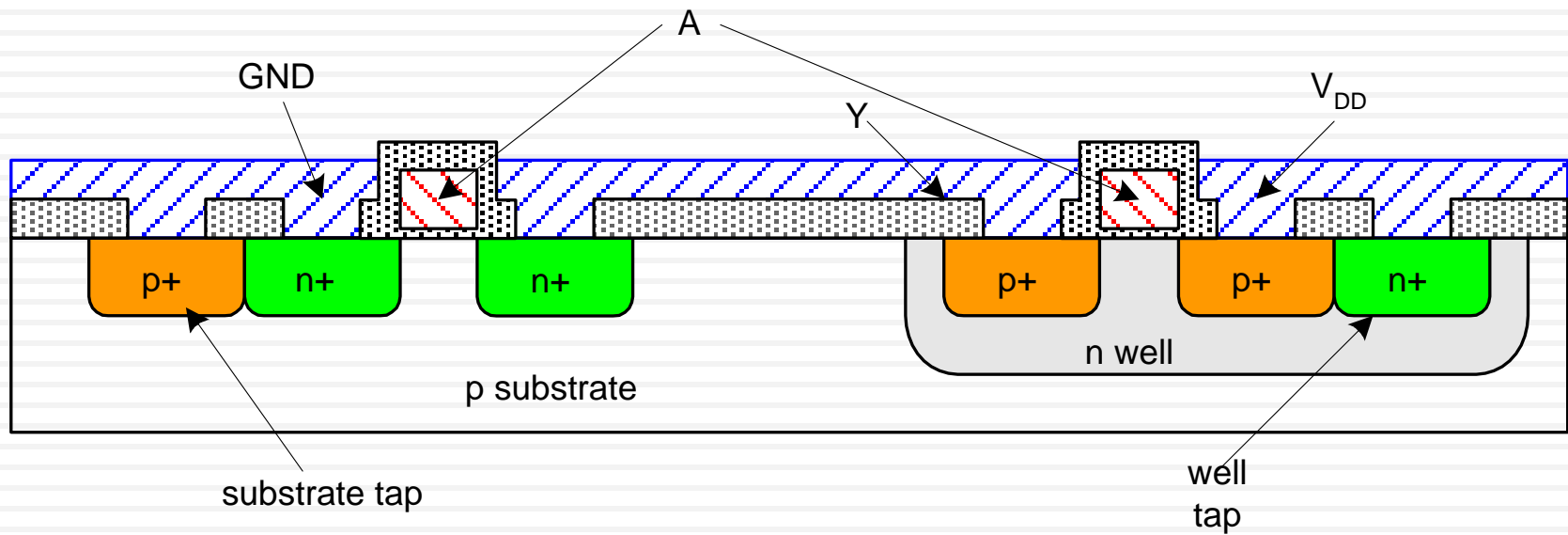
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors





# Well and Substrate Taps

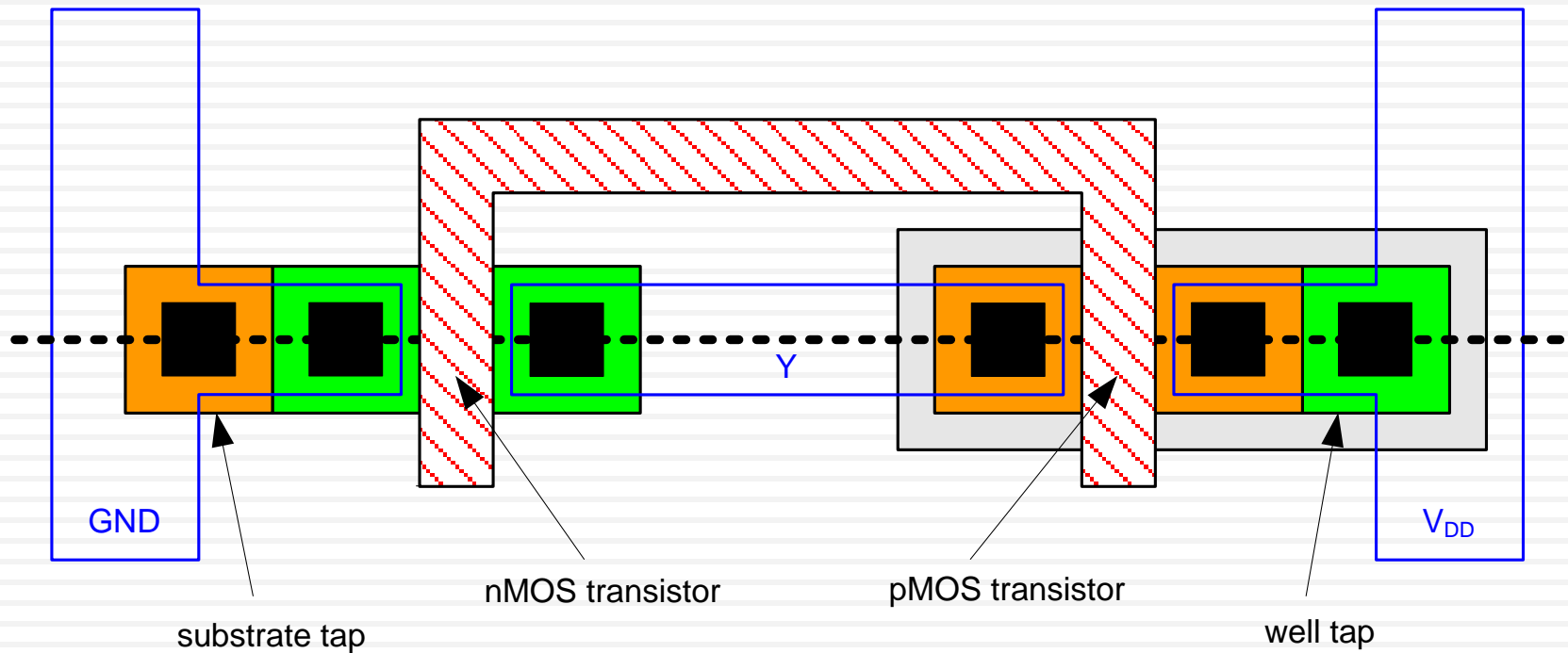
- Substrate must be tied to GND and n-well to  $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps





# Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line

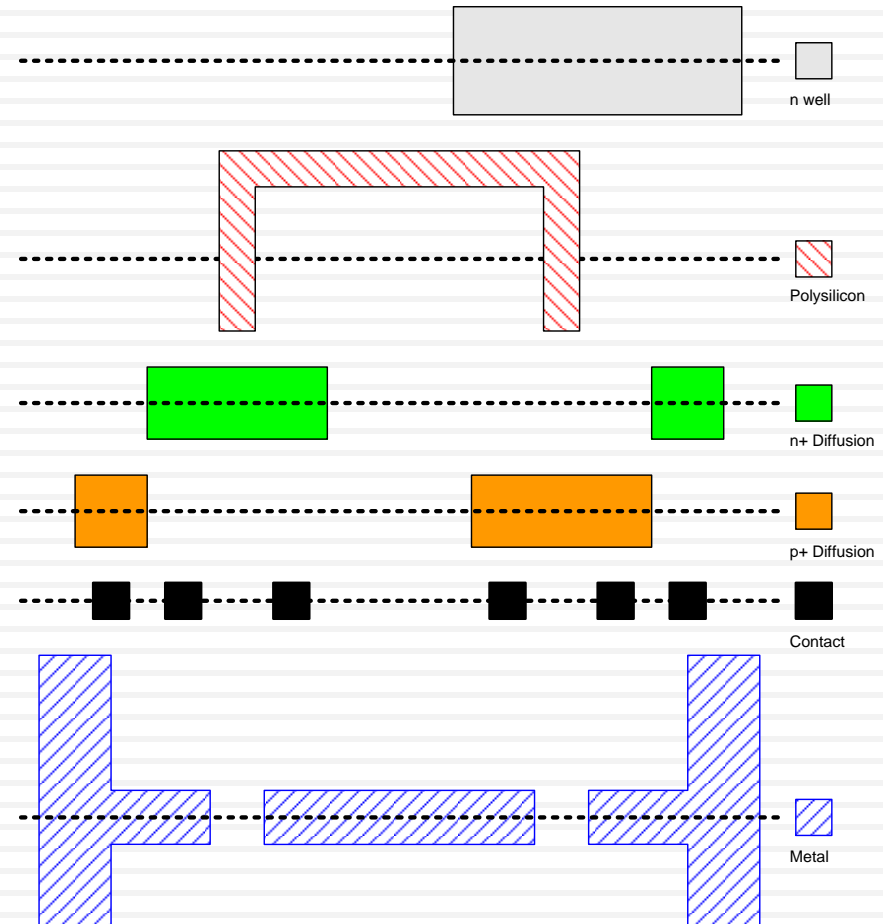




# Detailed Mask Views

## □ Six masks

- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal





# Outline

- ▣ Overview of CMOS Fabrication Processes
- ▣ **The CMOS Fabrication Process Flow**
- ▣ Design Rules





# Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields



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Business Machines Corporation.  
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# Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - ▣ Cover wafer with protective layer of  $\text{SiO}_2$  (oxide)
  - ▣ Remove layer where n-well should be built
  - ▣ Implant or diffuse n dopants into exposed wafer
  - ▣ Strip off  $\text{SiO}_2$

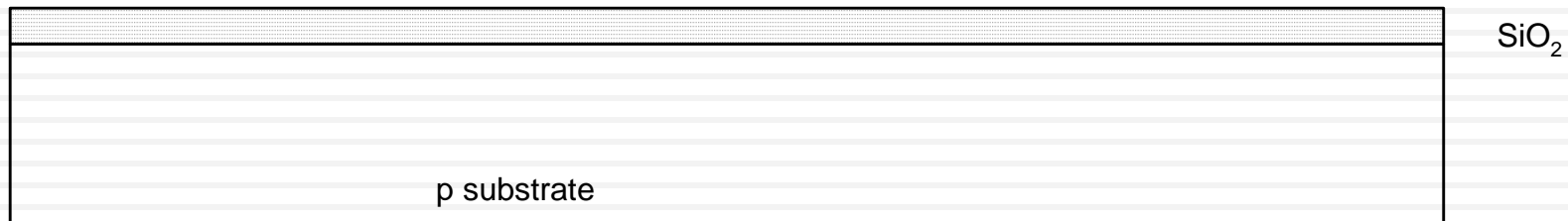


p substrate



# Oxidation

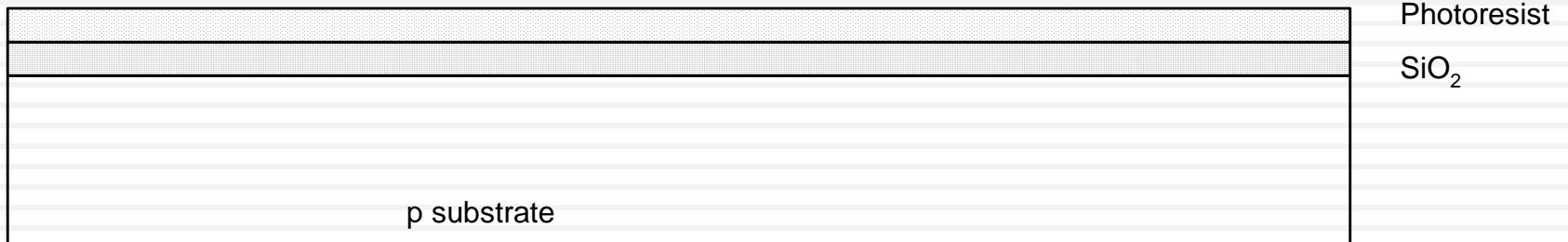
- Grow  $\text{SiO}_2$  on top of Si wafer
  - ▣ 900 – 1200 C with  $\text{H}_2\text{O}$  or  $\text{O}_2$  in oxidation furnace





# Photoresist

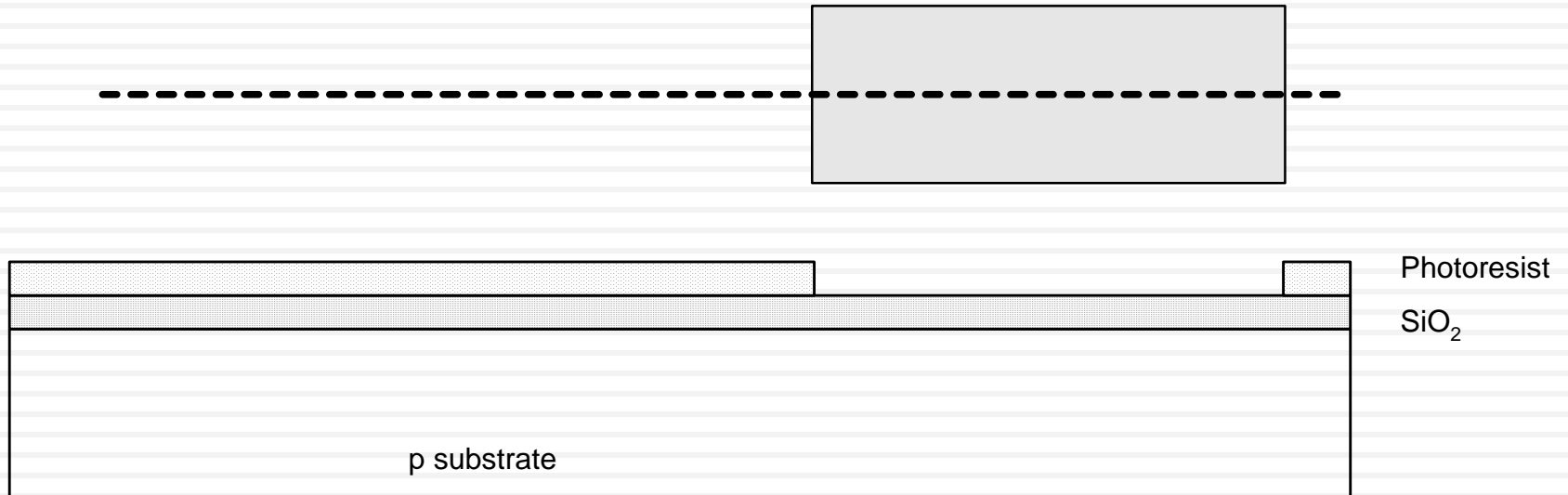
- Spin on photoresist
  - ▣ Photoresist is a light-sensitive organic polymer
  - ▣ Softens where exposed to light





# Lithography

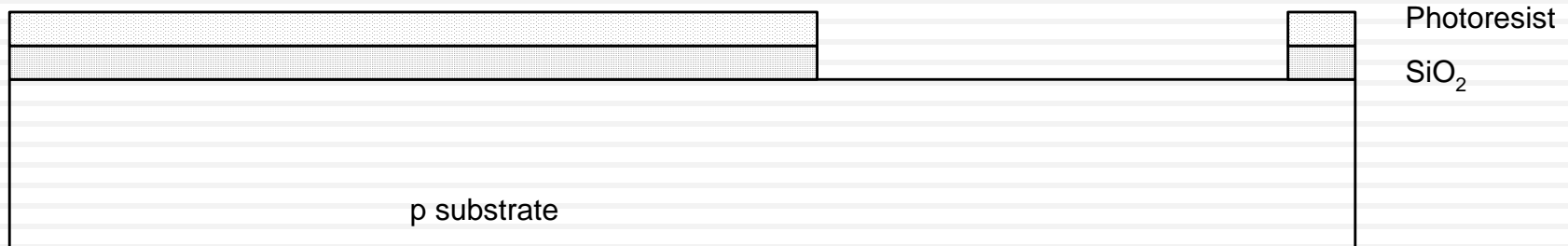
- Expose photoresist through n-well mask
- Strip off exposed photoresist





# Etch

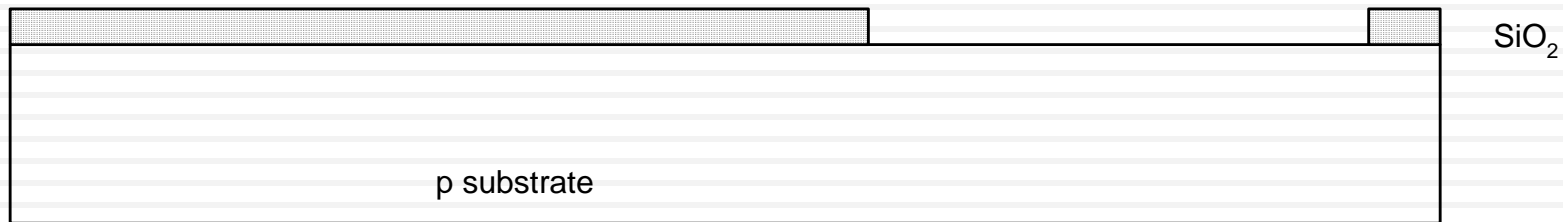
- Etch oxide with hydrofluoric acid (HF)
  - ▣ Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed





# Strip Photoresist

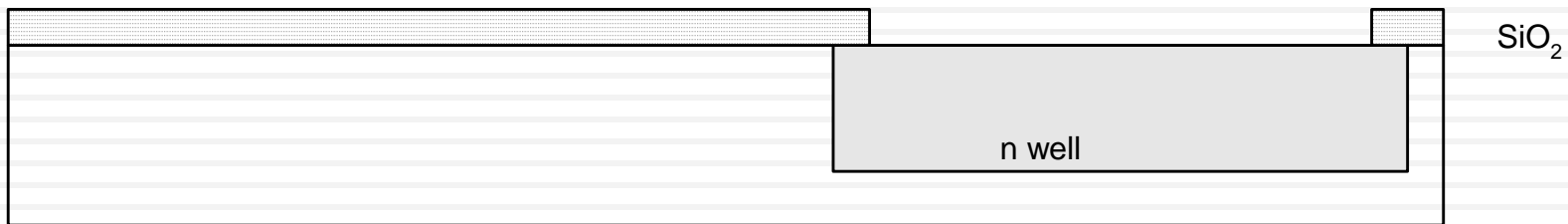
- Strip off remaining photoresist
  - ▣ Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step





# n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - ▣ Place wafer in furnace with arsenic gas
  - ▣ Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - ▣ Blast wafer with beam of As ions
  - ▣ Ions blocked by  $\text{SiO}_2$ , only enter exposed Si

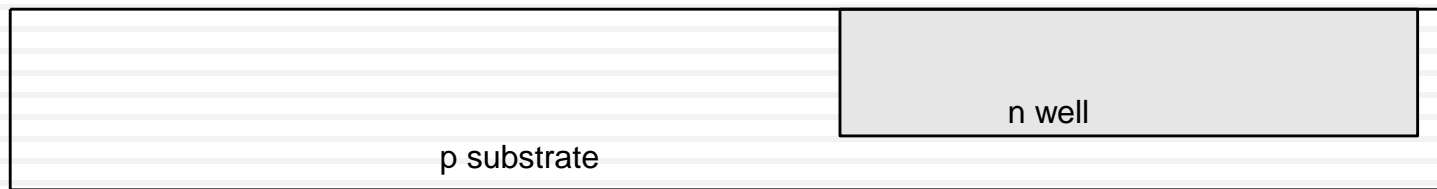






# Strip Oxide

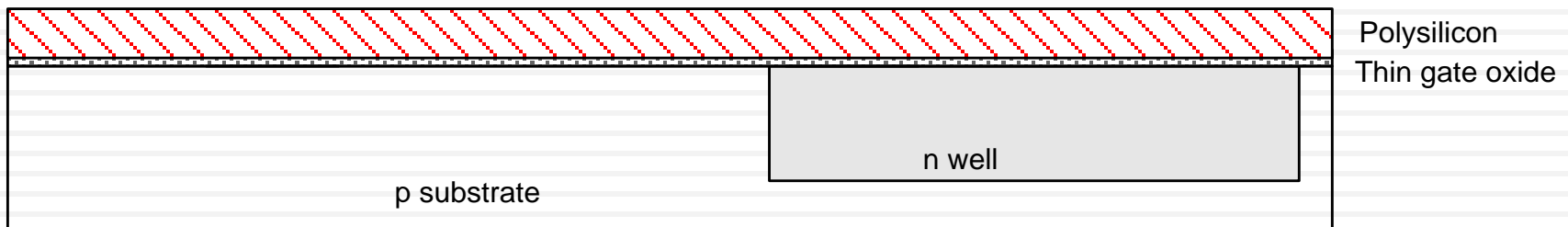
- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps





# Polysilicon

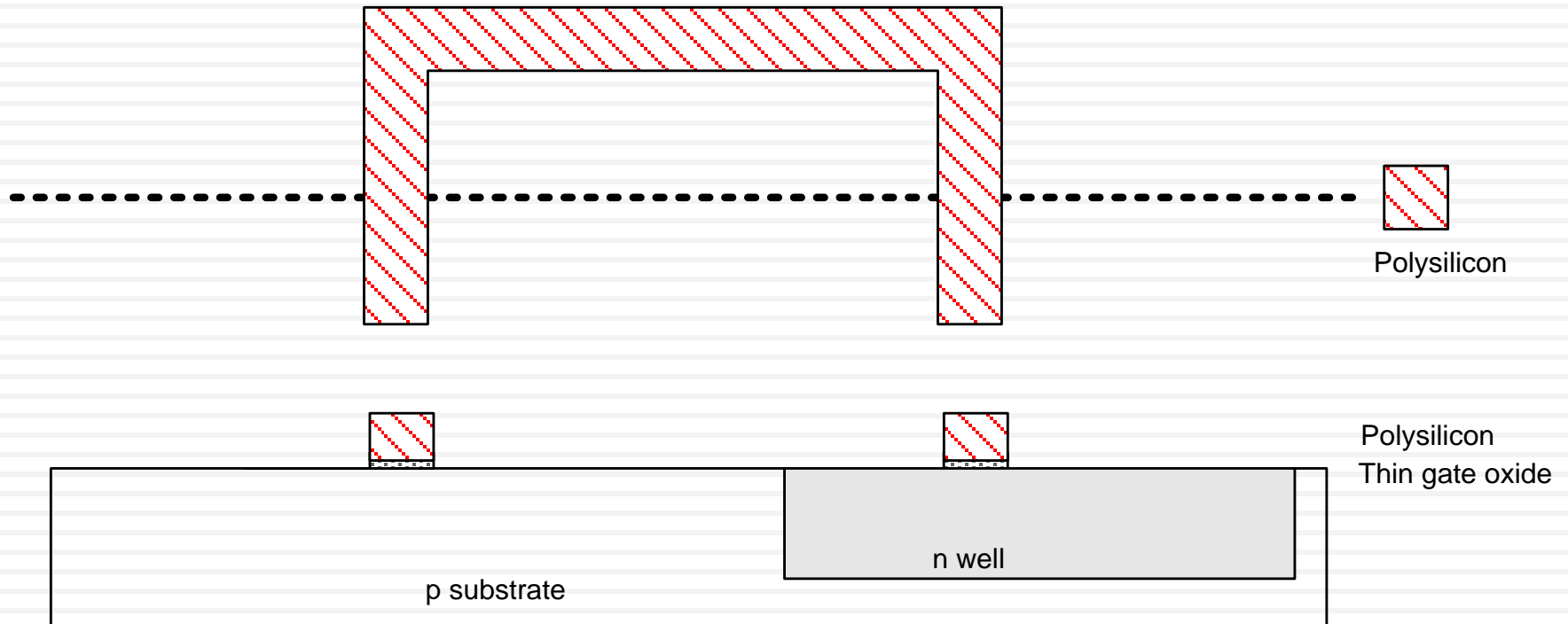
- Deposit very thin layer of gate oxide
  - ▣  $< 20 \text{ \AA}$  (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - ▣ Place wafer in furnace with Silane gas ( $\text{SiH}_4$ )
  - ▣ Forms many small crystals called polysilicon
  - ▣ Heavily doped to be good conductor





# Polysilicon Patterning

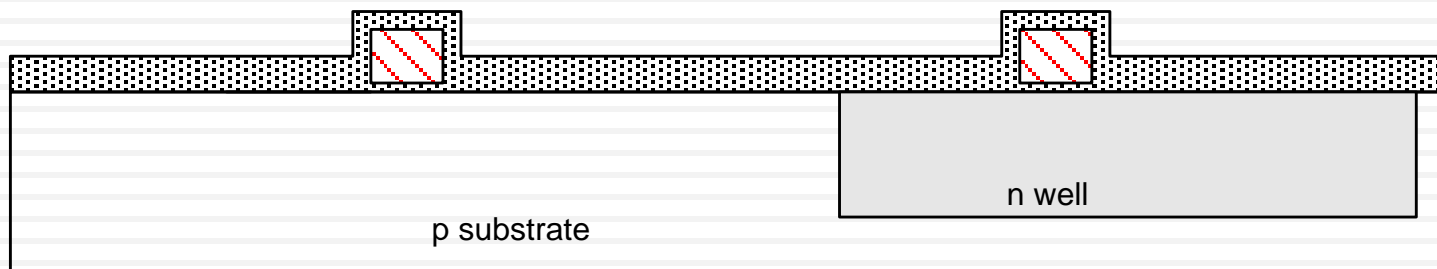
- Use same lithography process to pattern polysilicon





# Self-Aligned Process

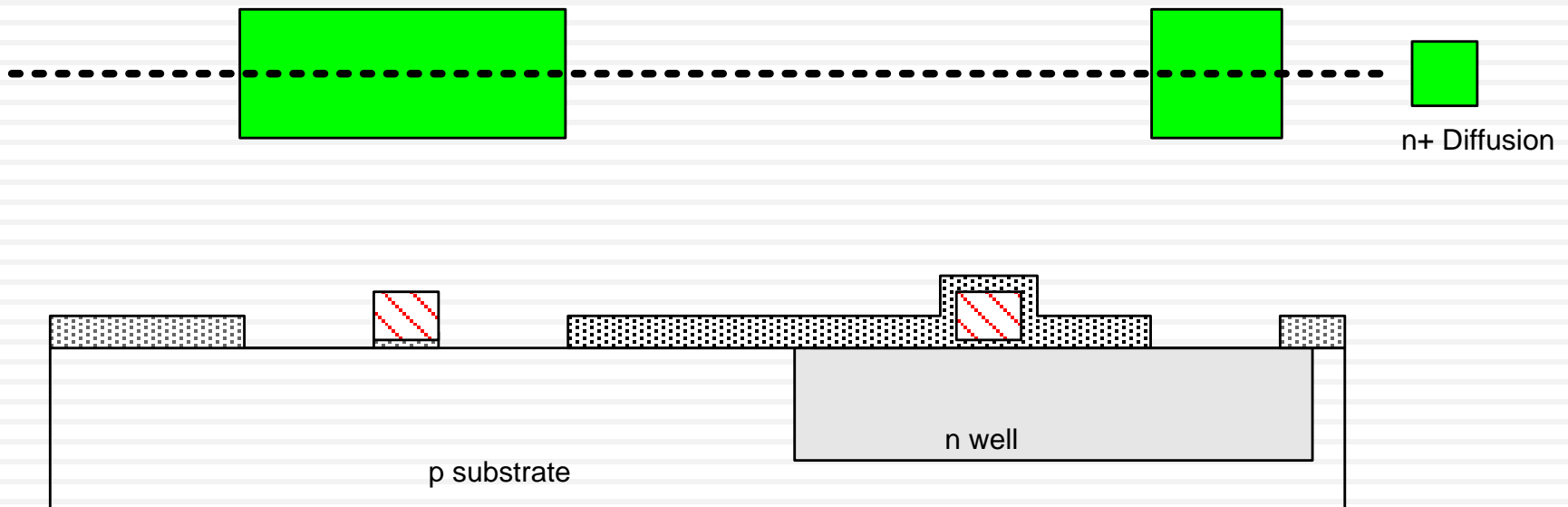
- Use oxide and masking to expose where  $n^+$  dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact





# N-diffusion

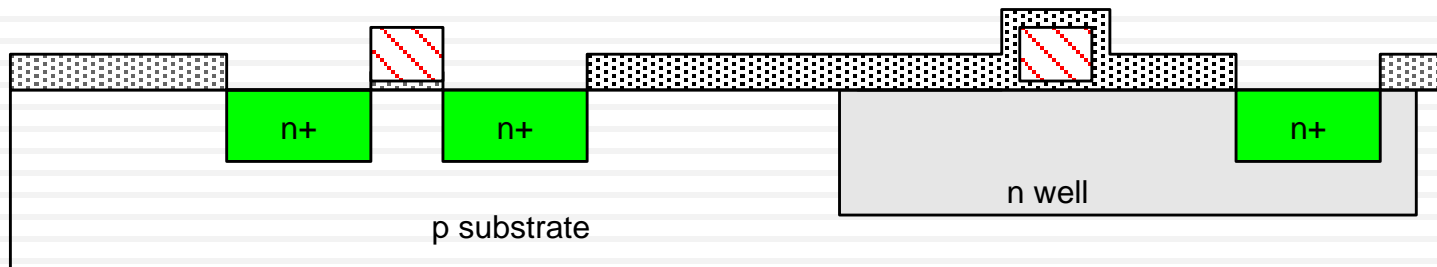
- Pattern oxide and form n<sup>+</sup> regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing





## N-diffusion cont.

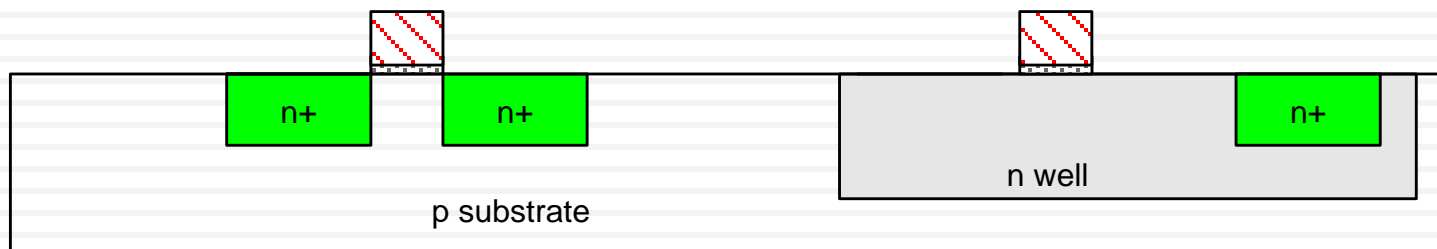
- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion





# N-diffusion cont.

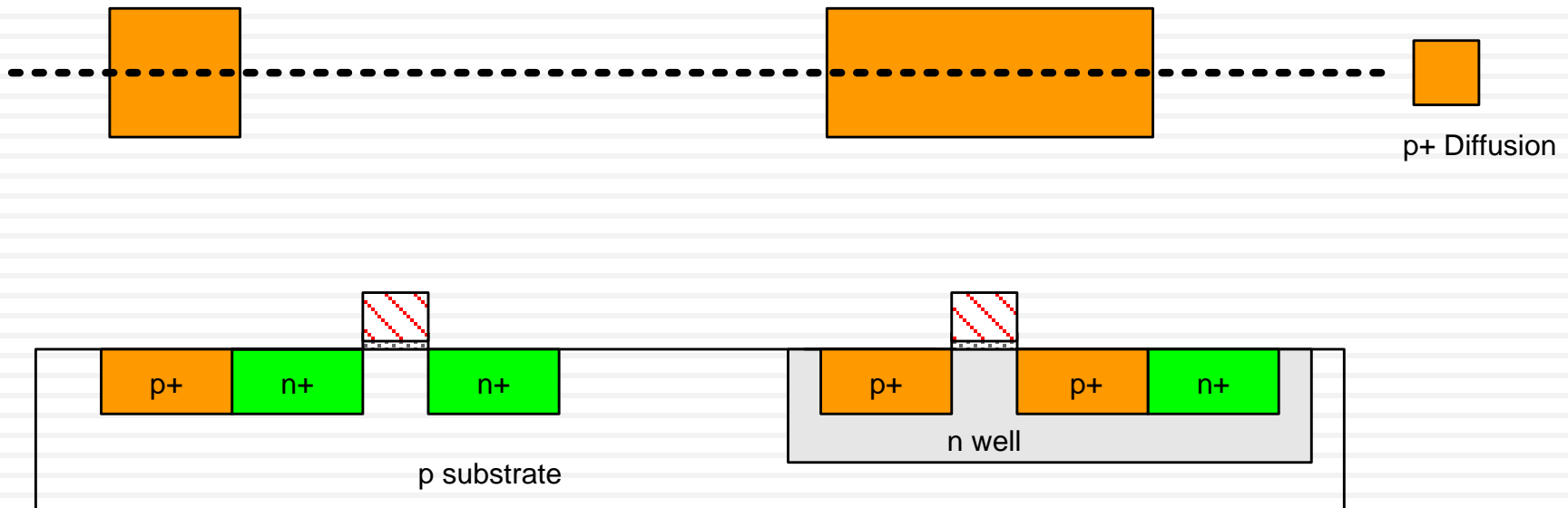
- Strip off oxide to complete patterning step





# P-Diffusion

- Similar set of steps form  $p^+$  diffusion regions for pMOS source and drain and substrate contact

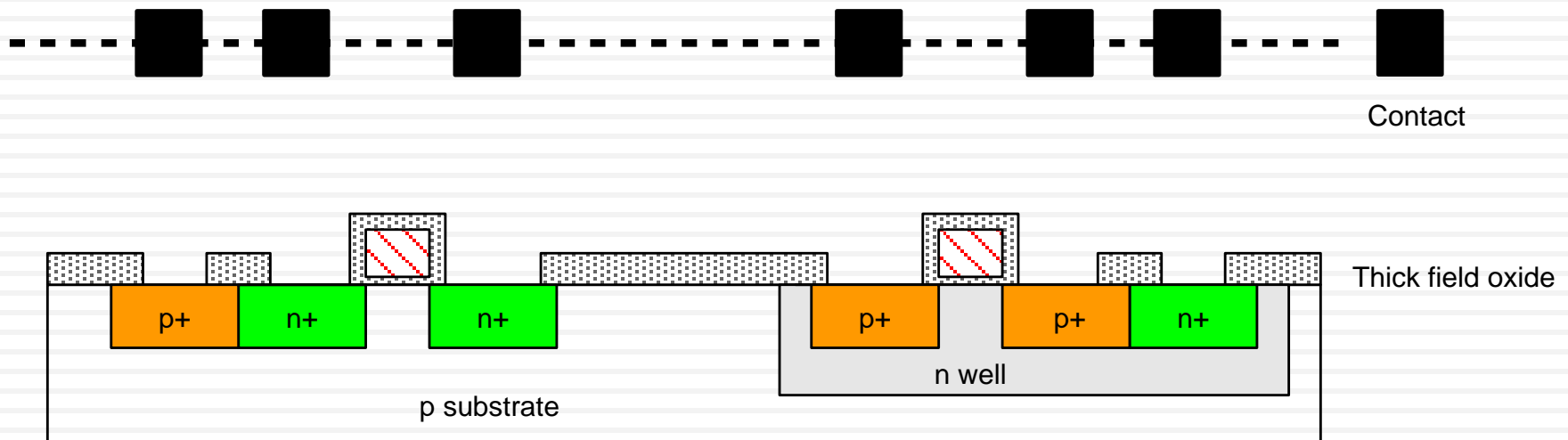






# Contacts

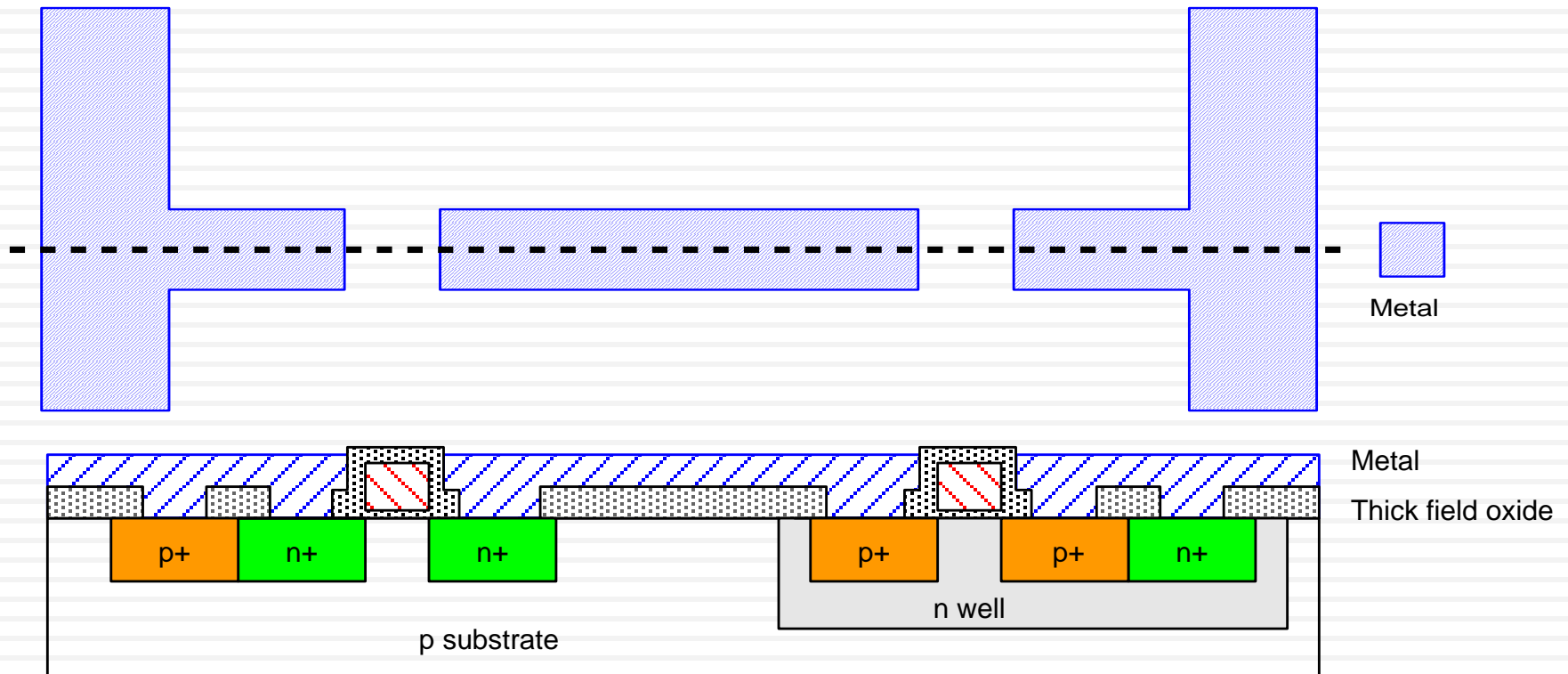
- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed





# Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires





# Outline

- ▣ Overview of CMOS Fabrication Processes
- ▣ The CMOS Fabrication Process Flow
- ▣ **Design Rules**



# Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size  $f$  = distance between source and drain
  - ▣ Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of  $\lambda = f/2$ 
  - ▣ E.g.  $\lambda = 0.3 \mu\text{m}$  in  $0.6 \mu\text{m}$  process



# Design Rules

- Design rules (DRs) are a set of geometrical specifications that dictate the design of the layout masks
- Such rules provide numerical values for minimum dimensions, line spacing, and other geometrical quantities
- DRs are derived from the limits on a specific processing line and must be followed to insure functional structures on the fabricated chip
- There are given numerical values in the DR listing; violating these values may lead to failure. In our notation
  - w = minimum width specifications
  - s = minimum spacing value
  - d = generic minimum distance



## Design Rules (2)

- DRs have units of length (usually  $\mu\text{m}$ )
- DRs change with the fabrication technology
- The popularity of VLSI fabrications has introduced the concept of the silicon foundry
- A foundry allows designers to submit designs using a state-of-the-art process
- Most foundry operations allow the submission of designs using a simpler set of design rules that can be easily scaled to different processes
- These are called lambda design rules where all DRs are expressed in terms of lambda ( $\lambda = \frac{1}{2} L_{Gate}$ )



# Why Design Rules

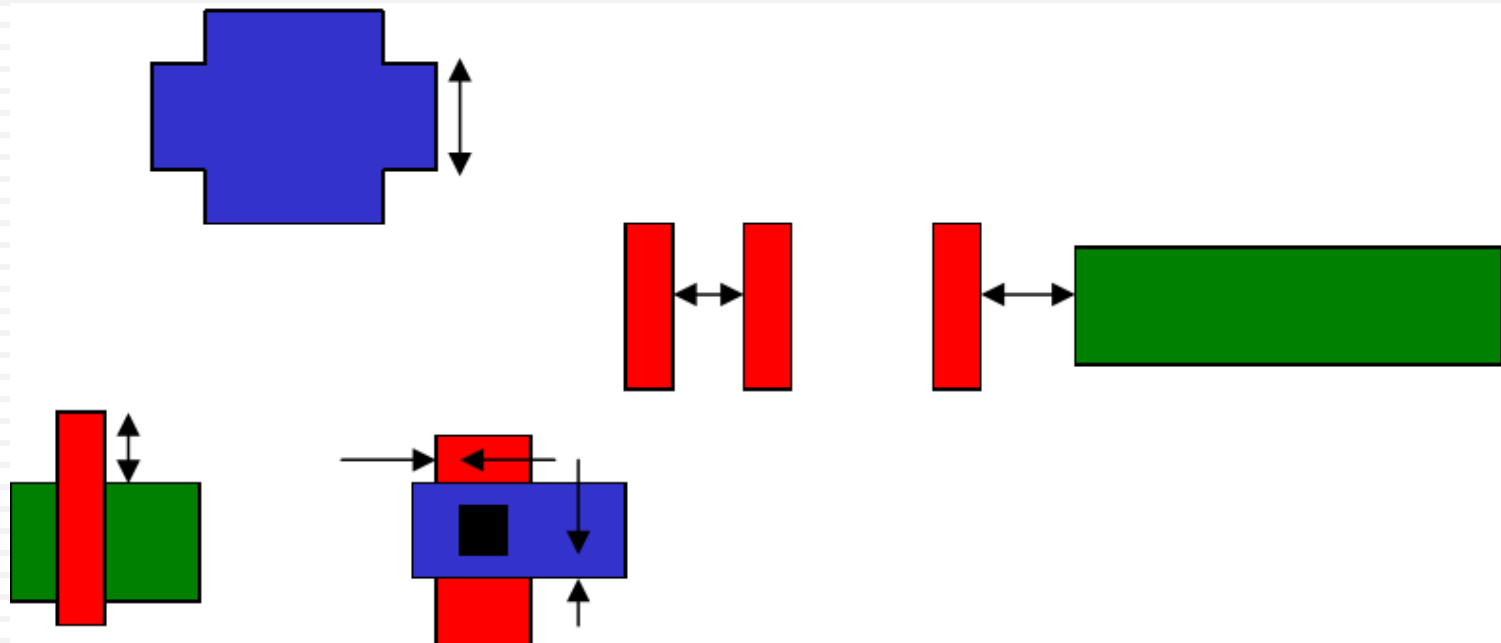
- Why do VLSI technology have Design Rules
  - fabrication process has minimum/maximum feature sizes that can be produced for each layer
  - alignment between layers requires adequate separation (if layers unconnected) or overlap (if layers connected)
  - proper device operation requires adequate separation
- “Lambda” Design Rules
  - lambda,  $\lambda$ , = 1/2 minimum feature size, e.g., 0.6 $\mu\text{m}$  process  $\rightarrow$   $\lambda=0.3\mu\text{m}$
  - can define design rules in terms of lambdas
    - allows for “scalable” design using same rules



# Design Rule Types

## □ Basic Rules

- minimum width
- minimum spacing
- Surround
- Extension

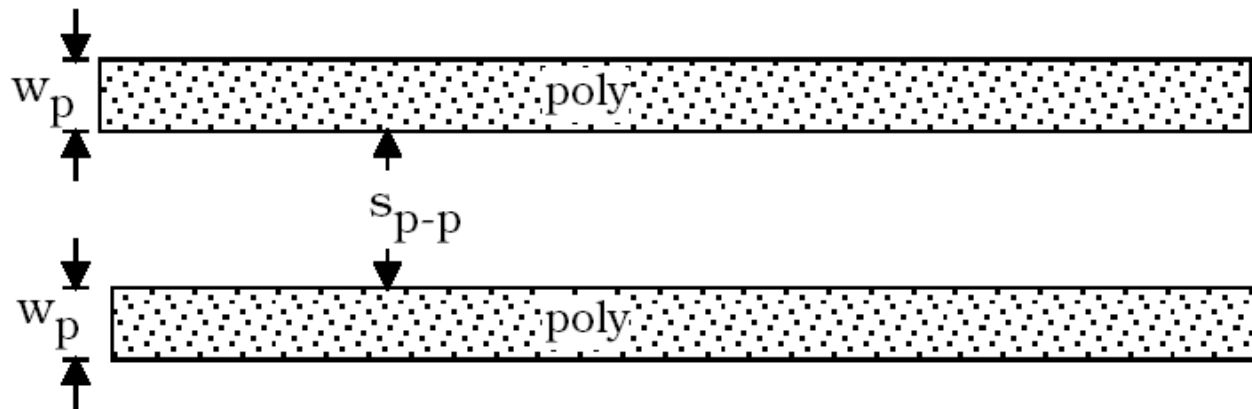






# Spacing and Width Design Rules

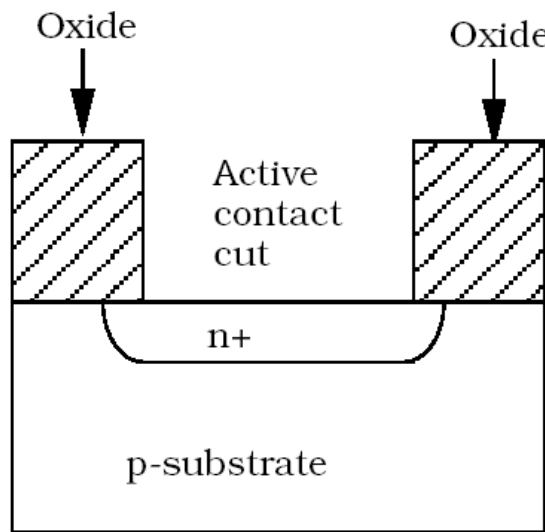
- Example of minimum spacing and width rules (poly)



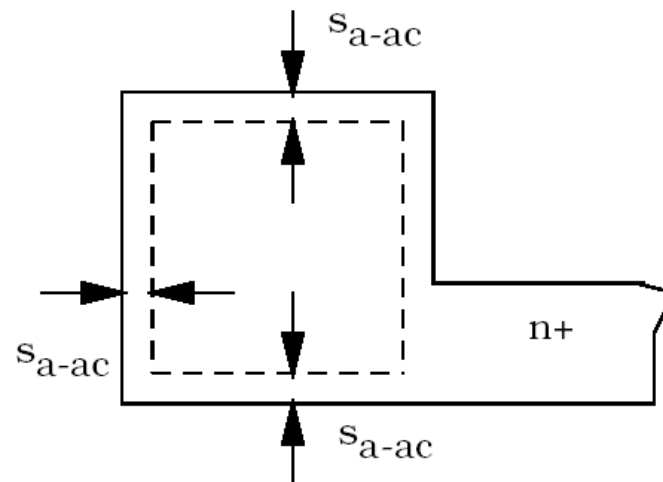


# Surround Design Rules

- Example of a surround rule (an active contact)
- This rule guards against a misaligned contact cut patterns during the lithographic exposure setup



(a) Side view

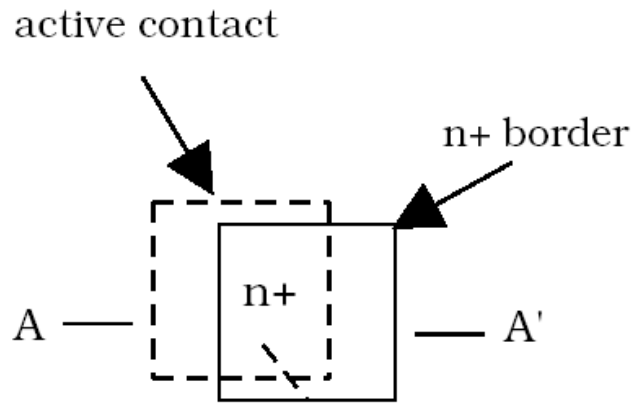


(b) Surround rule

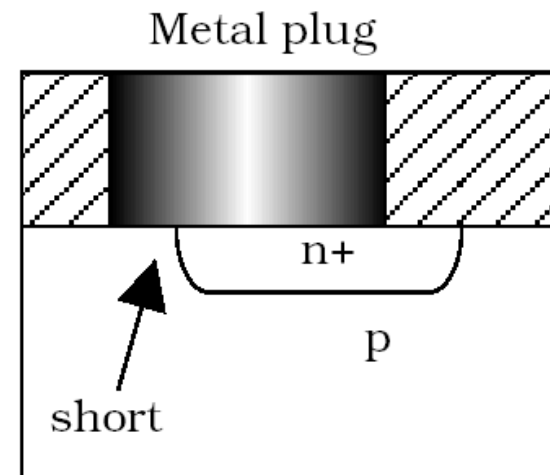


## Surround Design Rules (2)

- The accuracy of photolithography is the main factor that can lead to misalignment problems
- Figure shows a potential problem with active contacts due to misalignment



(a) Top view

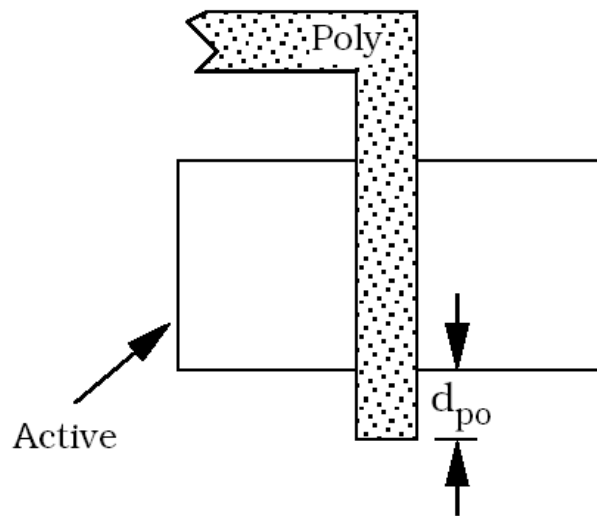


(b) Side view along A-A'

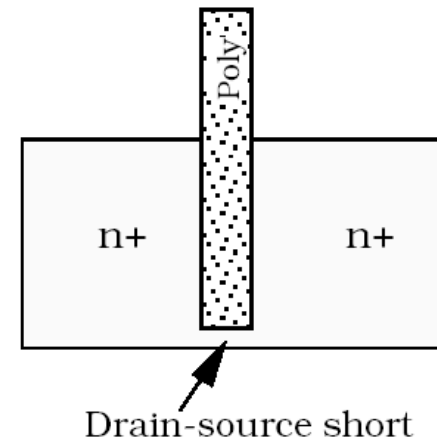


# Extension Design Rules

- Extension-type design rules also tend to be based on misalignment problems
- Figure shows the extension distance rule for polysilicon gate and a potential misalignment failure



(a) Gate overhang DR

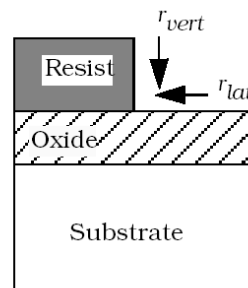


(b) Misalignment failure

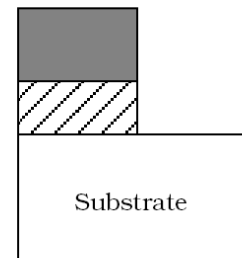


# Physical Limitations

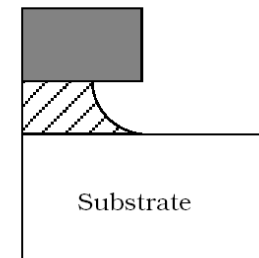
- Some geometrical design rules originate from physical considerations such as
  - The linewidth limitation of an imaging system
    - The reticle shadow projected to the surface of the photoresist does not have sharp edges due to optical diffraction
    - For example, a lightwave with an optical wavelength of  $\lambda$  cannot accurately image a feature size much less than  $\lambda$
  - The etching process introduces another type of problem as shown in Figure



(a) Resist pattern



(b) Pure anisotropic etch

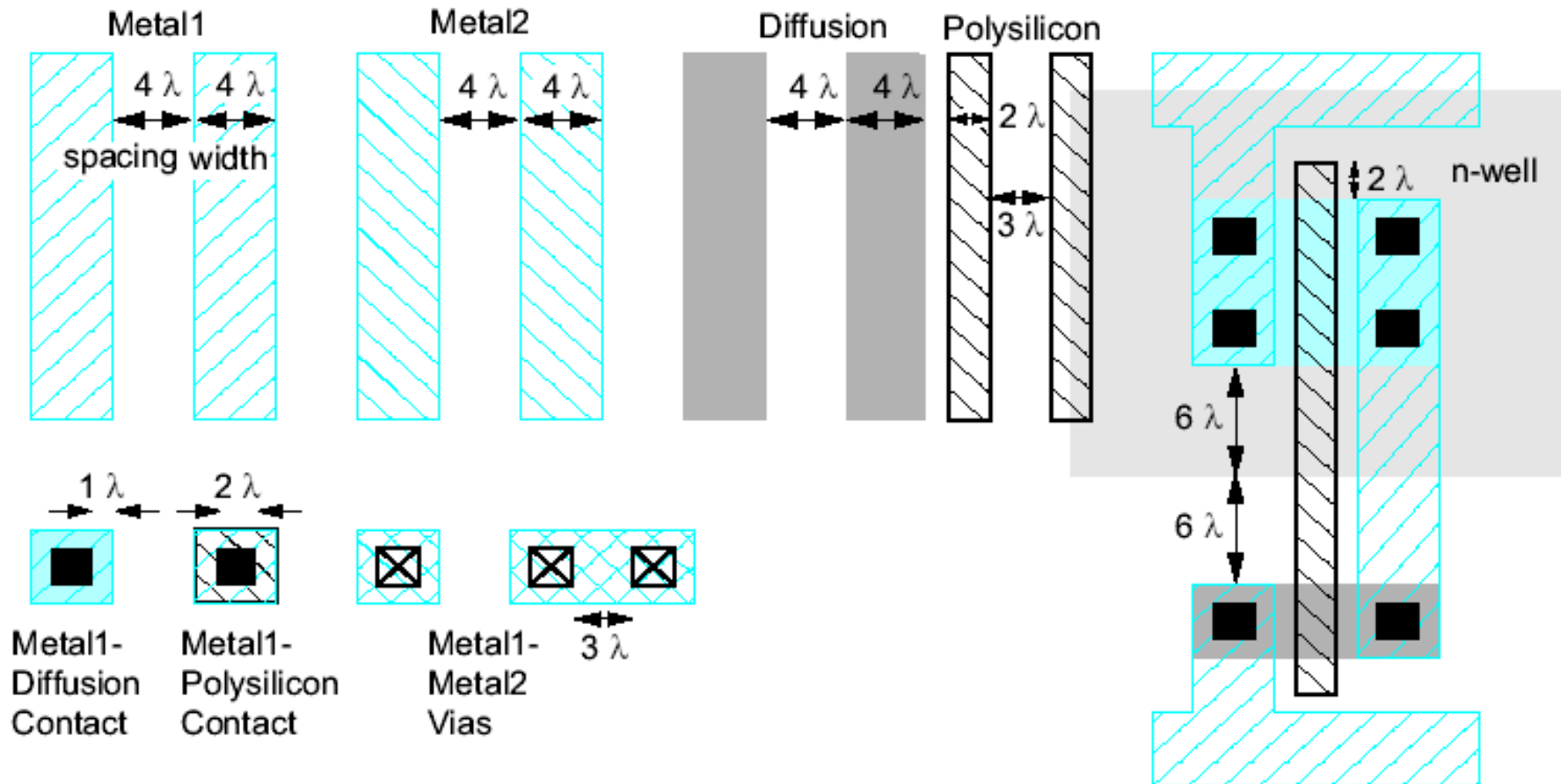


(c) Isotropic etch



# Simplified Design Rules

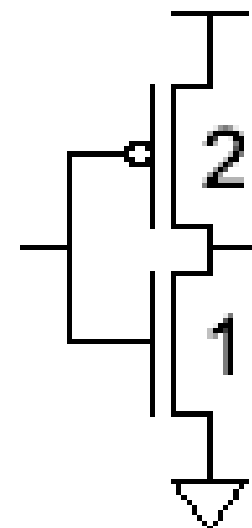
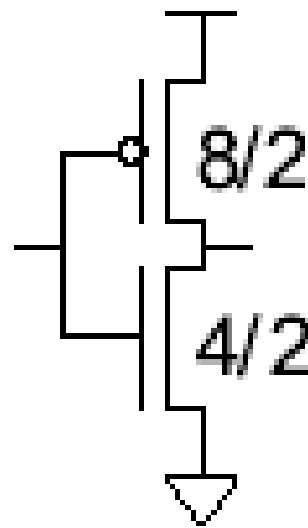
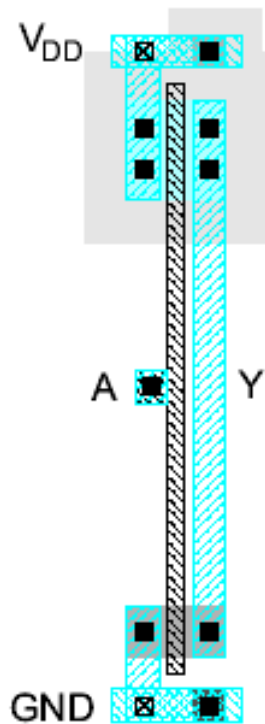
- Conservative rules to get you started





# Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is  $4\lambda / 2\lambda$ , sometimes called 1 unit
  - In  $f = 0.6 \mu\text{m}$  process, this is  $1.2 \mu\text{m}$  wide,  $0.6 \mu\text{m}$  long





# About these Notes

- The lecture notes are developed using the Uyemura VLSI book and Harris lecture notes of the CMOS VLSI Design book.