Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE431: Digital Integrated Circuits
Course Design Project

Objectives:

In this project, we will use Tanner EDA tools to design and analyze a 4-bit ripple-carry adder circuit. Figure 1 shows the design flow and the tools used in each stage. A tutorial of using the Tanner EDA tools is attached to the project document.

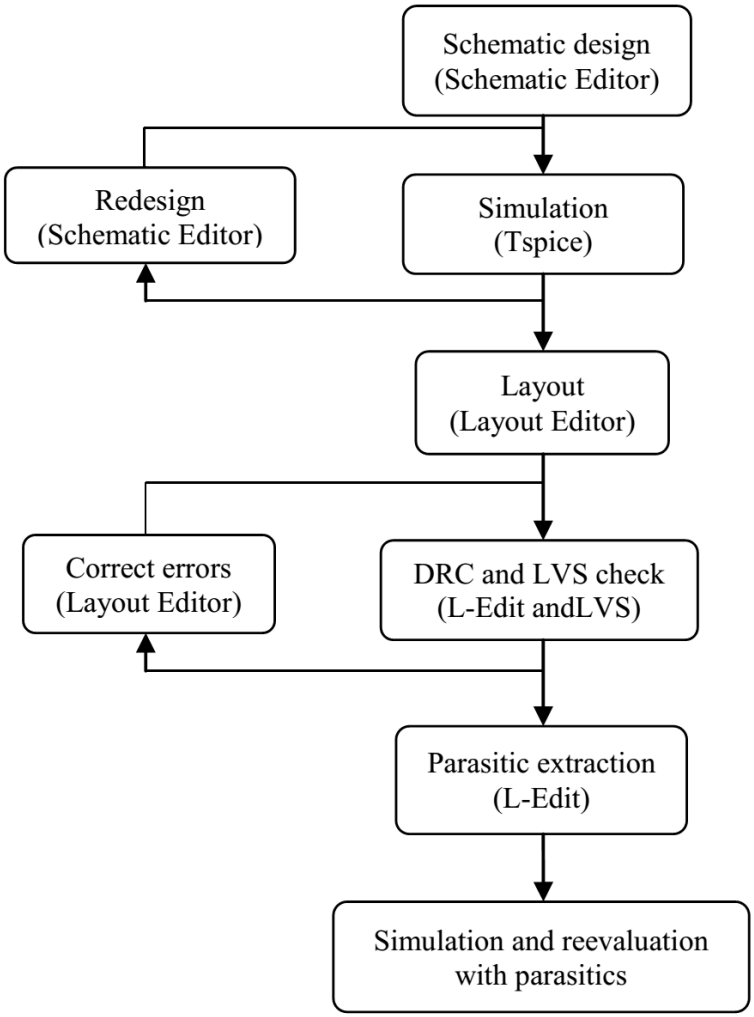

Figure 1: Tanner EDA design flow chart

Requirements:

The following requirements must be considered in this project:

1. You are required to design a 4-bit ripple carry adder shown in Figure 2. Use the 2µm MOSIS CMOS technology in your design. The building block of the design is a 1-bit Full Adder circuit constructed as a 24- transistor mirror shown in Figure 3.
2. You are required to calculate the size of each transistor in the full adder circuit to minimize the input to output delay. Given that the critical path in the ripple carry adder is well defined (carry propagation path), the design effort needs to be spent on reducing the carry propagation delay of the full adder (C_i to C_o delay).
3. The optimization goal for the ripple carry adders is to obtain the least delay and layout area simultaneously. The carry propagation path of the full adder is composed of the pull down network of MN1, MN2, and MN3, and the pull up network of MP1, MP2, and MP3 (Figure 3). The full adder is required to operate at a target frequency of 100 MHz for this project. The optimization should be performed with proper loading of the full adder carry output (C_o). For proper loading, two identical Full Adders (FA) need to be cascaded where the second FA acts as the load of the first FA.
4. Once the full adder schematic design is optimized, then the layout of the full adder is designed using the custom layout tool. For layout, the stick diagram shown in Figure 4 is used. When performing layout, the design goal is to minimize layout area by minimizing spacing and wire dimensions. Design Rule Check (DRC) is performed on the layout to remove any design rule violations. The Layout Versus Schematic (LVS) check is also performed to ensure the layout matches the schematic.
5. Once the design of the full adder is finished (both schematic and layout) then a symbol view for the full adder schematic is created. This allows hierarchical design where in the next level a new schematic view is created for the 4-bit ripple carry adder and four instances of the FA symbol are placed and cascaded to form the four-bit adder. Similarly the layout of the four-bit adder is obtained by creating four instances of a FA layout and cascading them.
6. Finally, DRC and LVS need to be performed on the four-bit adder design for verification. The last step is to extract parasitics from the layout of the 4-bit adder and add the parasitics to the schematic of the 4-bit adder for post layout simulation. The post layout simulation is performed to obtain the 4-bit adder carry propagation delay and the power consumption.

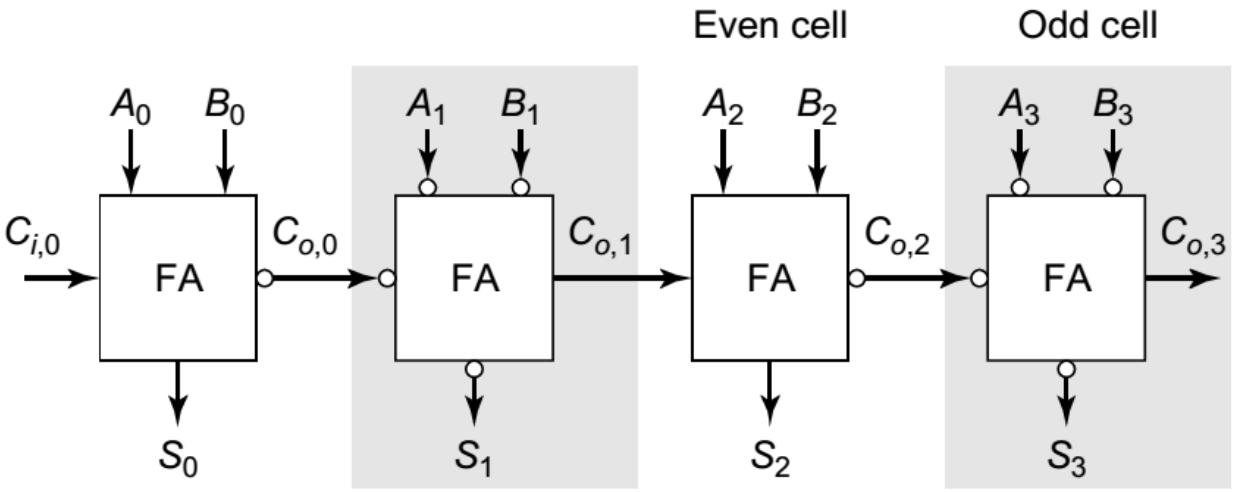

Figure 2: 4-bit ripple carry adder

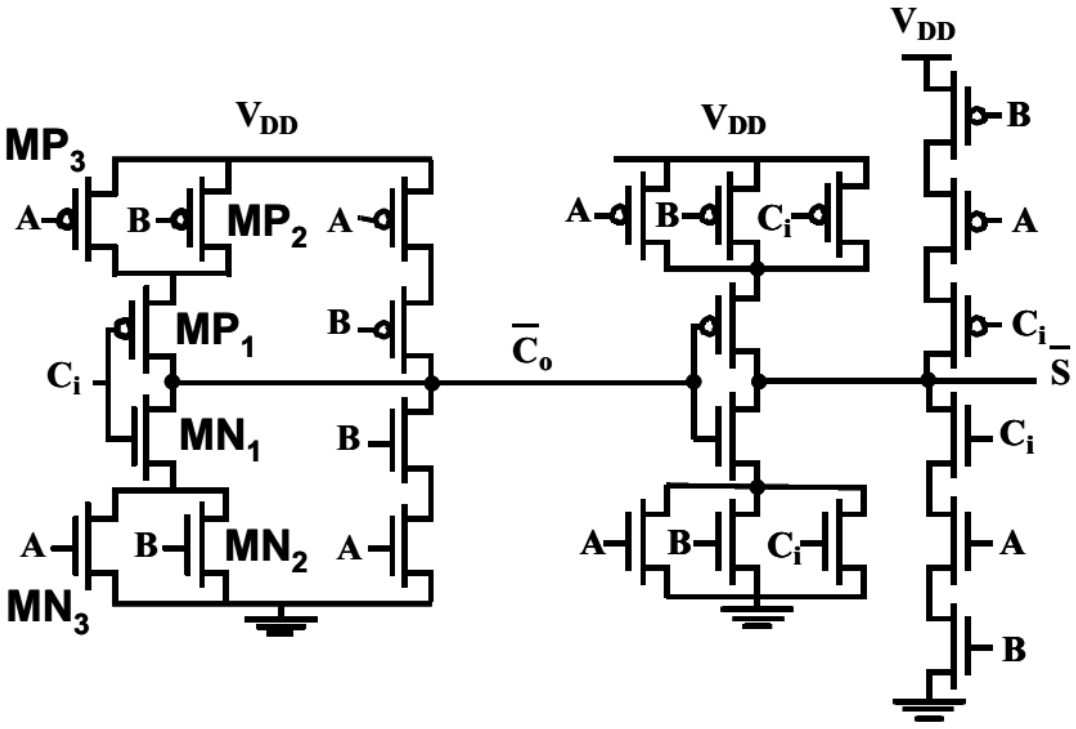

Figure 3: 1-bit Mirror full adder schematic

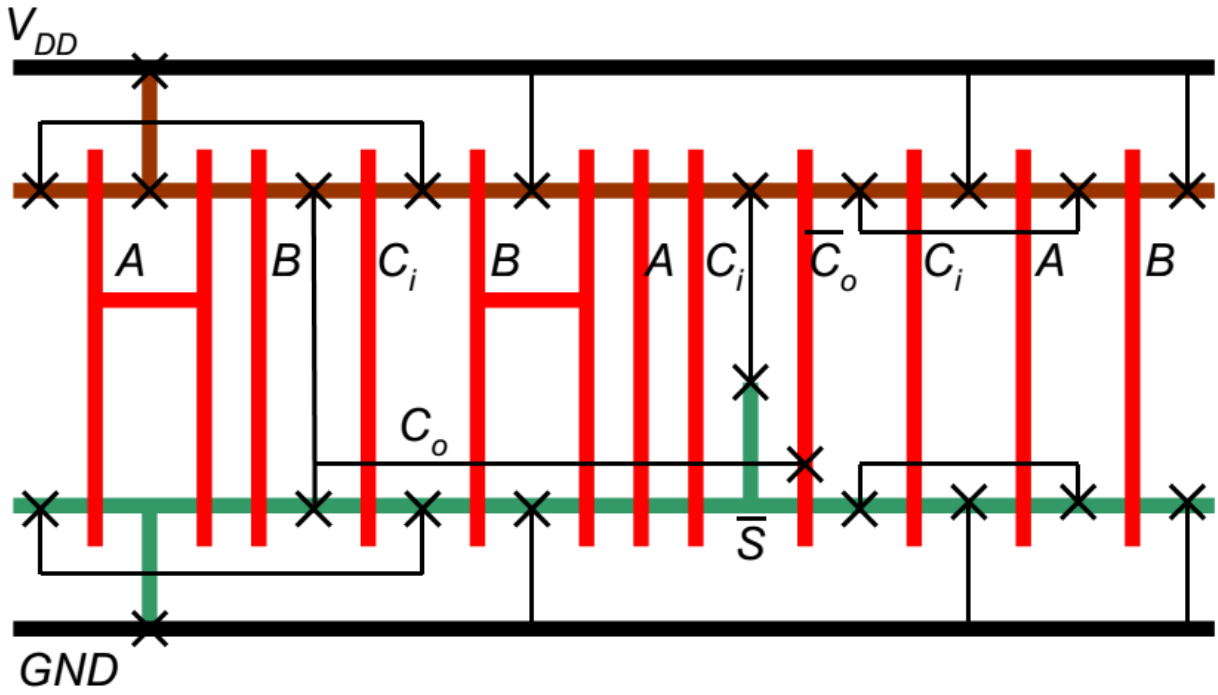

Figure 4: Stick diagram for layout of mirror full adder

References:

1. Lyons, Eli, et al. "Full-custom design project for digital VLSI and IC design courses using synopsys generic 90nm CMOS library." *Microelectronic Systems Education, 2009. MSE'09. IEEE International Conference on*. IEEE, 2009.