Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE431: Digital Integrated Circuits
Lab 3: CMOS Combinational Logic Gates

Introduction:

The experiment is to design a 2-input CMOS NAND gate based on the CMOS inverter and study its characteristics. Using the properties of the inverter we are able to create a network of NMOS and PMOS transistors to create logic [Figure 1]. This allows the creation of any of the logic gates, to illustrate we build a NAND gate. This gate is an important one because this is a universal gate, meaning we can create any logic function using only this gate. Its logic function is $\overline{A.B}$, which is what the design must satisfy [Table 1].

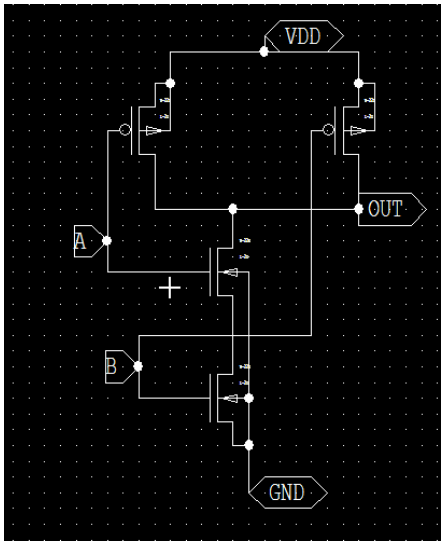

Figure 1

Table 1

A	B	NAND
1	0	1
1	1	1
0	0	1
0	1	0

The experiment will also analyze the "worst case" scenario in which the propagation delay is extended because of the conditions the PMOS and NMOS are interacting.

Procedures:

The NAND gates is composed of a pull up and pull down network, composed of PMOS and NMOS transistors respectively. When designed in the NAND manner the width of the PMOS channel is larger than that of the NMOS, causing the gate to not have a desired VDD/2 threshold. This led to the sizing of the NMOS network to match the PMOS and have an equal voltage drop across the two networks.

The NAND gate accepts two inputs and with their combinations the NAND gate turns on or off the NMOS and PMOS, creating paths to VDD or ground hence creating the logic. Because these are networks that interact with each other, there is cases where the networks in parallel and its components are not all on or off at the same time causing the "worst case" scenario. This is when the path of the current through a network is giving the correct logic, but because of the input combinations not all the transistors are operating, causing smaller channels or longer paths. When such case occurs it is identified as the "worst case" because the propagation delay is increased, which is not desirable. For this design the worst case condition is when one of the PMOS transistors is on and the other off lowering the width of the channel.

The procedures involved

- Design a static 2 input CMOS NAND gate on S-edit as shown in figure 1, then generate the netlist on T-SPICE.
- Then it had to be tested for the logic functionality of the design so it satisfies the NAND gate properties. (We have two inputs use two input pulse waves see figure 1 and the following paragraph will illustrate more).
    - For input A, add an input pulse source with period of 200ns.
    - For input B, add an input pulse source with period of 100ns.
- Size each gate such that NMOS and PMOS pull strength for both networks match for the "worst case" delay. (See lecture notes).
- Then, simulate the Voltage Transfer Characteristic (VTC) of the design to verify the functionality of the switching. (By connecting all the inputs together, acts as an inverter).
- Finally, draw the layout for the NAND gate using L-Edit and run LVS to verify your layout. (refer to lab 2 for LVS setup)
- Repeat the previous steps for NOR gate.

Notes:

- The simulation is to be done on T-SPICE. Varying the transistor sizes can be done directly on the netlist. You will need the sizes of the standard inverter designed in lab 2 where the optimum $W_p = 28$ µm and $W_n = 6$ µm to achieve $V_{th} = 2.5$ V (note that this is the size for the inverter not the NAND gate).

- It is preferable that the layout is done with sharing the diffusion.
- Use ml5_20.md as a technology file for the simulation and LVS.

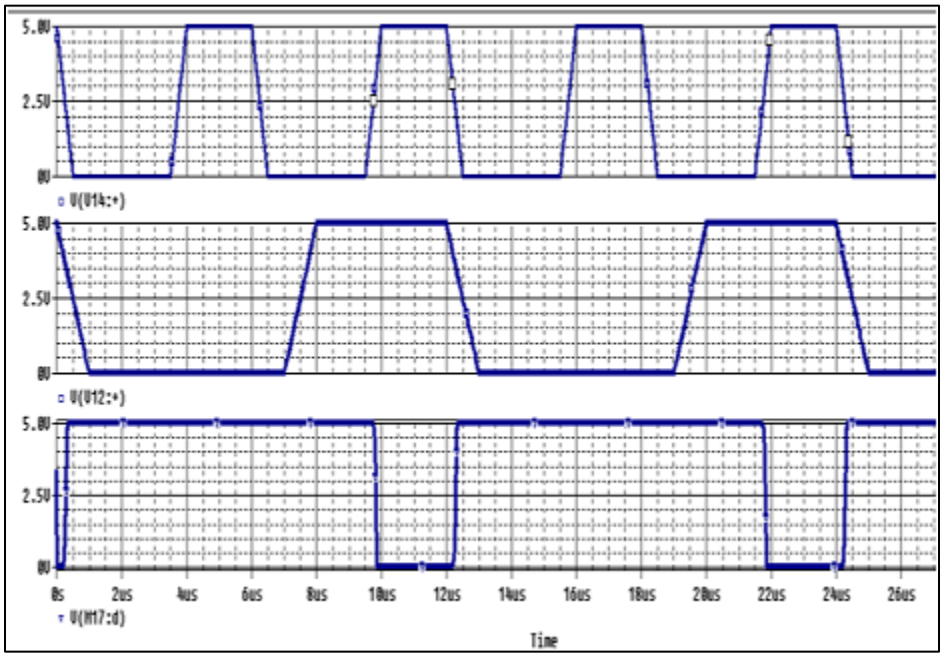

Figure 2 – Input patterns

Reference:

Christian Gil, Edgar Siles, “CMOS Digital Electronics Laboratory Notes”, California State University, Northridge.