

Alexandria University Faculty of Engineering Electrical Engineering Department

EE 431 Digital Integrated Circuits Lab#1: Physical Design and Layout of CMOS Inverter

Objectives

Upon the completion of this Lab, you should be able to:

- 1. Use L-edit software to lay out basic CMOS digital circuits,
- 2. Use T-spice software to analyze static and dynamic characteristics of CMOS digital circuits.

Requirements

You are required to draw the vertical and horizontal layouts for the minimum sized symmetric CMOS inverter using the 2um MOSIS CMOS technology and compare between the two layouts in terms of the used area, power consumption, DC characteristics, and propagation delays. Both inverters should have the same dimensions. The following sections provide the detailed procedures to draw the layout of the vertical CMOS inverter using L-edit.

Manual Layout

- Copy the following files into your directory Technology setup files for MOSIS/Orbit n-well 2.0 micron process. (Technology
 = SCNA, LAMBDA = 1.0 micron) C(tanner/ledit83/samples/tech/mosis/morbn20.
- 2. Launch L-Edit

3. Create New File. Create new files by choosing **File > New**, which opens the **New**

File dialog:

File type:	OK
Layout Text	Cancel
Copy TDB setup from file:	
Layout2	Browse
<empty></empty>	
Layout1	
Layout2	

4. Replacing the Setup.

File > Replace Setup transfers setup information from a file (the *source* file) to the current file (the *destination* file).

From file:		OK
F:\TA\ece755\Tutorial\L	EDITTut\morbn20. Browse	Cancel
Layers Layers Replace Merge CIF names GDS II Wire settings	Design Technology Maintain physical size Rescale Draw Selection Palette Grid Show/Hides Yref files Properties	Uncheck Al
SPR Core setup	Extract IC Cross-Section Pad route setup Place and Route configuration	

5. Under Setup -> Design

The chosen technology units should be lambda It should be 1 internal unit for 1/1000 lambda The lambda value should be 1 microns

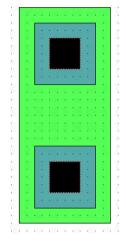
Grid -> Grid Display -> Displayed Grid 0.5 locator units

Setup Design	X Setup Design X
Technology Grid Selection Drawing Curves Xref files	Technology Grid Selection Drawing Curves Xref files
MOSIS/ORBIT 2.0u SCNA Technology units O Microns O Millimeters O Microns O Millimeters	Grid display Displayed grid: Locator Units Suppress grid less than: 8 Pixels
C Mils C Inches C Other: Lambda Technology setup C Maintain physical size of objects C Rescale the design Lambda per Internal Unit	Mouse grid Cursor type: I Snapping C Smooth Mouse snap grid: 0.500 Locator Units
1 Internal Unit = 1 1000 Lambda	Locator Units One Locator Unit: 1000 Internal Units
1 Lambda = $\frac{1}{1}$ Microns	
OK Cancel	OK Cancel

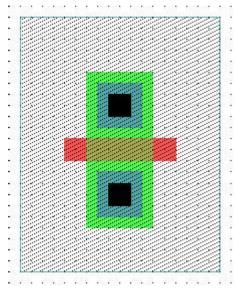
- 6. Create a new cell. Cell -> New, call it inv
- 7. Draw 14 x 6 λ **Active** Box.

8. Draw two 4 x 4 λ Metal1 box and put on both sides of Active box.

9. Draw two 2 x 2 λ Active Contact centered on each Metal 1 box It looks like.



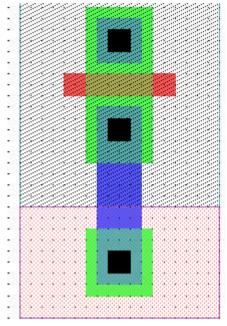
- 10. Draw 10 x 2 λ poly box centered at the active.
- 11. Draw 18 x 23 λ N Select.



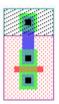
12. Copy the whole block above, select N Select and click Edit -> Edit Object, change

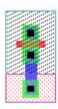
N Select to be P Select.

- 13. Draw 10 x 18 λ P Select below the Nselect of NMOS.
- 14. Draw 6 x 6 λ Active inside the Pselect.
- 15. Draw 2 x 2 λ Active Contact inside the Active
- 16. Extend the Metal1 to Pselect area, it looks like:

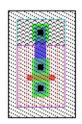


17. With the same method draw a Nselect on the top of PMOS



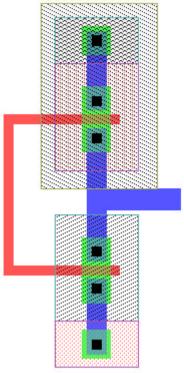


18. Draw 25 x 40 λ Nwell at PMOS place.

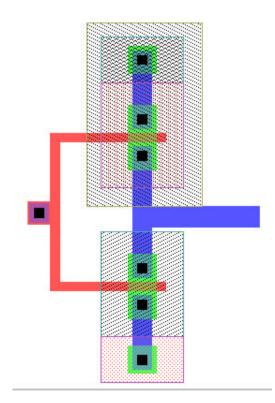




19. Connect following the inverter schematic.



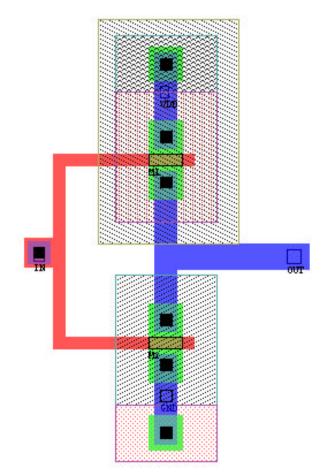
- 20. Draw 5 x 6 λ Poly beside the gate of two transistors.
- 21. Draw 4 x 4 λ Metal 1 centered in the poly.
- 22. Draw 2 x 2 λ Poly Contact centered in the Metal1



23. Click Port A on the Toolbar. And draw OUT port. The dialog jumps out. On Layer: Metal1 Port name: OUT

	1		ill Data type: 0
oxes Tori	Polygons Ports (1)	Wires Circles	Pie Wedges Instances
	name: OUT		
Texts	size: 2.500	🛨 Locator Units	
Coordinates	s (Locator Units)-	Text Alignment	
×1: 11	.500	0.0	C Above
	000	0 0	C Middle
X2: -9.0		• •	C Below
	500 🛁		D1.1.
Y1: 89.		Left Center	Hight
		Left Center	

24. With the same method draw port for IN, VDD, GND. On Layer: Metal1, Port name:IN/VDD/GND. It looks like



25. Run DRC check

A dialog box jumps out.

Place error ports		
 Place error ports Place error object 	te	
Log file:	do .	
Write errors to	file	
☐ Write detailed	timing statistics to file	
inv.drc	Browse.	
Bin size: 50.000	Locator Units	
	Ecodior Office	

- 26. If No DRC error, go to next step. If there is any, open the file inv.drc or click to see the error. If you don't like the error displayed on the screen, click on the bar.
- 27. Extract the file to be SPICE file. Click 🖾 on the toolbar. A dialog jumps out. Fill the form as following then click RUN.

Extract X	Extract General Output Subcircuit	X	
Extract definition file: morbn20.ext Browse SPICE extract output file:	Comments Write node names Write device coordinates (Locator Units) Write shorted devices Write layer capacitance and resistance wa	Write nodes and devices as Integers Names Integers	
Inv.spc Browse Image: Constraint of the second secon	 ☐ Write values in scientific notation ☐ Write verbose SPICE statements 	Nodal parasitic capacitance Image: Write nodal parasitic capacitance Ignore nodal parasitic capacitance Issues: than: 5	
Bin size: 100.000 Locator Units Run Cancel Accept	SPICE include statement: 	0.md"	

28. Launch T-Spice to run simulation. The Spice file looks like

* Circuit Extracted by Tanner Research's L-Edit Version 8.30 / Extract Version 8.30 ;

- * TDB File: F:\TA\ece755\Tutorial\LEDITTut\inv.tdb
- * Cell: inv Version 1.24
- * Extract Definition File: morbn20.ext
- * Extract Date and Time: 09/28/2001 10:26

.include "G:\WIN32\TannerT\models\ml2_20.md"

- * Warning: Layers with Unassigned AREA Capacitance.
- * <P Base Resistor>

- * <N Well Resistor>
- * <P Diff Resistor>
- * <N Diff Resistor>
- * <Poly2 Resistor>
- * <Poly Resistor>
- * Warning: Layers with Unassigned FRINGE Capacitance.
- * <Poly1-Poly2 Capacitor>
- * <P Base Resistor>
- * <N Well Resistor>
- * <P Diff Resistor>
- * <N Diff Resistor>
- * <Poly2 Resistor>
- * <Poly Resistor>
- * <Pad Comment>
- * Warning: Layers with Zero Resistance.
- * <PMOS Capacitor>
- * <NMOS Capacitor>
- * <Poly1-Poly2 Capacitor>
- * <Pad Comment>

* NODE NAME ALIASES

- * 1 = IN (-56.5,90)
- * 2 = OUT (-11.5,89.5)
- * 3 = VDD (-34,119)
- * 4 = GND (-34,65)

M1 OUT IN VDD VDD PMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u * M1 DRAIN GATE SOURCE BULK (-36 107 -30 109) M2 GND IN OUT GND NMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u * M2 DRAIN GATE SOURCE BULK (-36 74.5 -30 76.5)

* Total Nodes: 4

* Total Elements: 2

- * Total Number of Shorted Elements not written to the SPICE file: 0
- * Extract Elapsed Time: 0 seconds
- .END

Pay attention to the sequence of the MOSFET connection to ensure it is drain, gate, source and base

29. Add the running command and run simulation.

- * Circuit Extracted by Tanner Research's L-Edit Version 8.30 / Extract Version 8.30 ;
- * TDB File: F:\TA\ece755\Tutorial\LEDITTut\inv.tdb
- * Cell: inv Version 1.24
- * Extract Definition File: morbn20.ext
- * Extract Date and Time: 09/28/2001 10:26

.include "G:\WIN32\TannerT\models\ml2_20.md"

- * Warning: Layers with Unassigned AREA Capacitance.
- * <P Base Resistor>
- * <N Well Resistor>
- * <P Diff Resistor>
- * <N Diff Resistor>
- * <Poly2 Resistor>

- * <Poly Resistor>
- * Warning: Layers with Unassigned FRINGE Capacitance.
- * <Poly1-Poly2 Capacitor>
- * <P Base Resistor>
- * <N Well Resistor>
- * <P Diff Resistor>
- * <N Diff Resistor>
- * <Poly2 Resistor>
- * <Poly Resistor>
- * <Pad Comment>

* Warning: Layers with Zero Resistance.

- * <PMOS Capacitor>
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M1 OUT IN VDD VDD PMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u * M1 DRAIN GATE SOURCE BULK (-36 107 -30 109) M2 GND IN OUT GND NMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u * M2 DRAIN GATE SOURCE BULK (-36 74.5 -30 76.5)

Vin IN GND PULSE (0 5 0 1n 1n 100n 200n) Vdd VDD GND 5

.tran/powerup 5n 500n method=bdf .print tran v(IN) v(OUT)

- * Total Nodes: 4
- * Total Elements: 2
- * Total Elements: 2
- * Total Number of Shorted Elements not written to the SPICE file: 0
- * Extract Elapsed Time: 0 seconds

.END