



Guide to the Tanner EDA v12.6 Design Tools
for use in designing, simulating, and laying out ICs.
Department of Electrical and Computer Engineering
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Summary:

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to enter schematics, perform SPICE simulations, do physical design (i.e., chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks. There are 3 tools that are used for this process:

- | | |
|---------|--|
| S-edit | - a schematic capture tool |
| T-SPICE | - the SPICE simulation engine integrated with S-edit |
| L-edit | - the physical design tool |

Using S-Edit (Schematic Entry Tool) & T-SPICE (Analog Simulation Tool)

Example: IV Curves of an NMOS Transistor

S-edit is a schematic entry tool that is used to document circuits that can be driven forward into a layout of an integrated circuit. It also provides the ability to perform SPICE simulations of the circuits using a simulation engine called T-SPICE. T-SPICE can be setup and invoked from within S-edit.

Part 1: Setup your Directory Structure & download Libraries

- a) Log onto a computer on 6th floor Cobleigh.
- b) You want to create a directory for all of your Tanner EDA projects. You also will need to download and unzip a set of library & model files from the course website that will be used for your simulations.
 - Create a directory structure named “EELE414_VLSI_Fall2011\Tanner_Projects
- c) Go to the course website and download the zip file called “Tanner_Libraries.zip”. Unzip it into your Tanner Projects directory. This group of files contain the necessary information to enter components into S-edit (circuit symbols), perform SPICE simulations (models), and do physical layout (layer definitions, DRC, LVS)

Part 2: Start a New Design & Setup Libraries

- a) Start S-Edit:
 - Start – All Programs – Tanner EDA – Tanner Tools v12.6 – S-Edit v12.6
- b) Start a New Design:

Using the pull down menus, create a new design:

- File – New - New Design

A dialog will appear asking for a design name and location. When you give the name, S-edit will create a folder of that name in the directory that you provide that will contain all of the design files. You should give a descriptive name that represents each simulation you will be running.

- Enter the name “HW03_NMOS_IV_Part1” and browse to your “EELE414_VLSI_Fall2011\Tanner_Projects” directory

- Click “OK”

- c) Create a new Cell

A “cell” is a design element. A cell can contain multiple views such as schematics and

symbols. Cells can be instantiated in other cells. When performing a simulation, we will typically call the cell “TOP”. When we are testing a circuit, for example an inverter, the inverter will have its own cell that contains a schematic of the devices and a symbol. The inverter cell is instantiated in the TOP cell that contains ideal elements such as voltage sources and probes that are only used for simulation. This allows us to separate the cells that are actually going to be implemented on the die versus cells that are only used for simulation.

Using the pull down menus, create a new cell view:

- Cell – New View:

- enter the cell name “TOP”. Ensure the design name is “HW03_NMOS_IV_Part1” and click OK. You can leave the interface and view names “view0”.

A blank schematic page will appear. It is a good idea to save this right now.

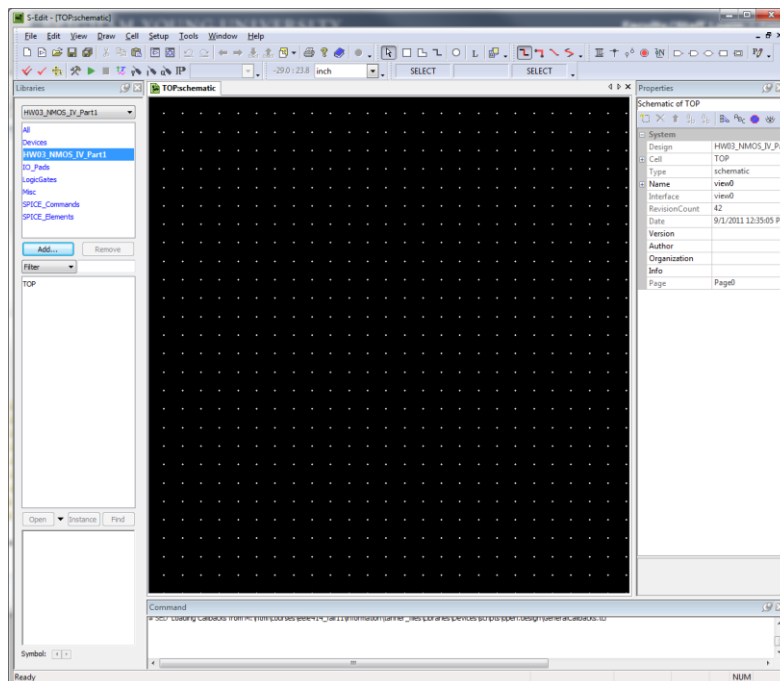
d) Enter the symbol libraries:

First, you need to include a *library* which contains the symbols for all basic circuit elements such as resistors, NMOS, capacitors, etc... The libraries for all the basic symbols are in the Tanner_Libraries.zip file you downloaded and unzipped.

- On the left side of the S-edit screen you’ll see a *Libraries* window, click on the “Add” button.

- Browse to “Libraries\All\All.tanner” and click “OK”

You should see a set of libraries appear:



- e) Setup the SPICE Models for the Generic_025 kit.

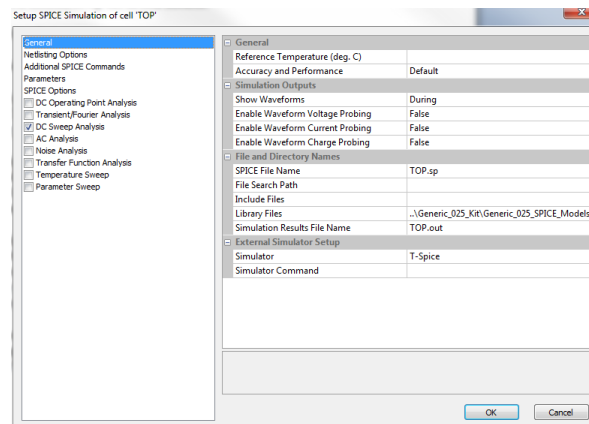
The libraries that you just added have symbols for NMOS and PMOS transistors. However, all non-linear components such as MOS transistors require a model to describe their behavior. If you simply enter an NMOS symbol in your schematic, SPICE will not know what to do since each NMOS transistor fabricated in a different technology behave differently.

In this example, we will use a transistor technology called “Generic_025”, which represents a standard, 0.25um CMOS process. You will need to setup the SPICE models for this process in S-edit. Once you do that, when you enter an NMOS or PMOS transistor, you can then associate the 0.25um model to that symbol.

Using the pull down menus, setup the SPICE models:

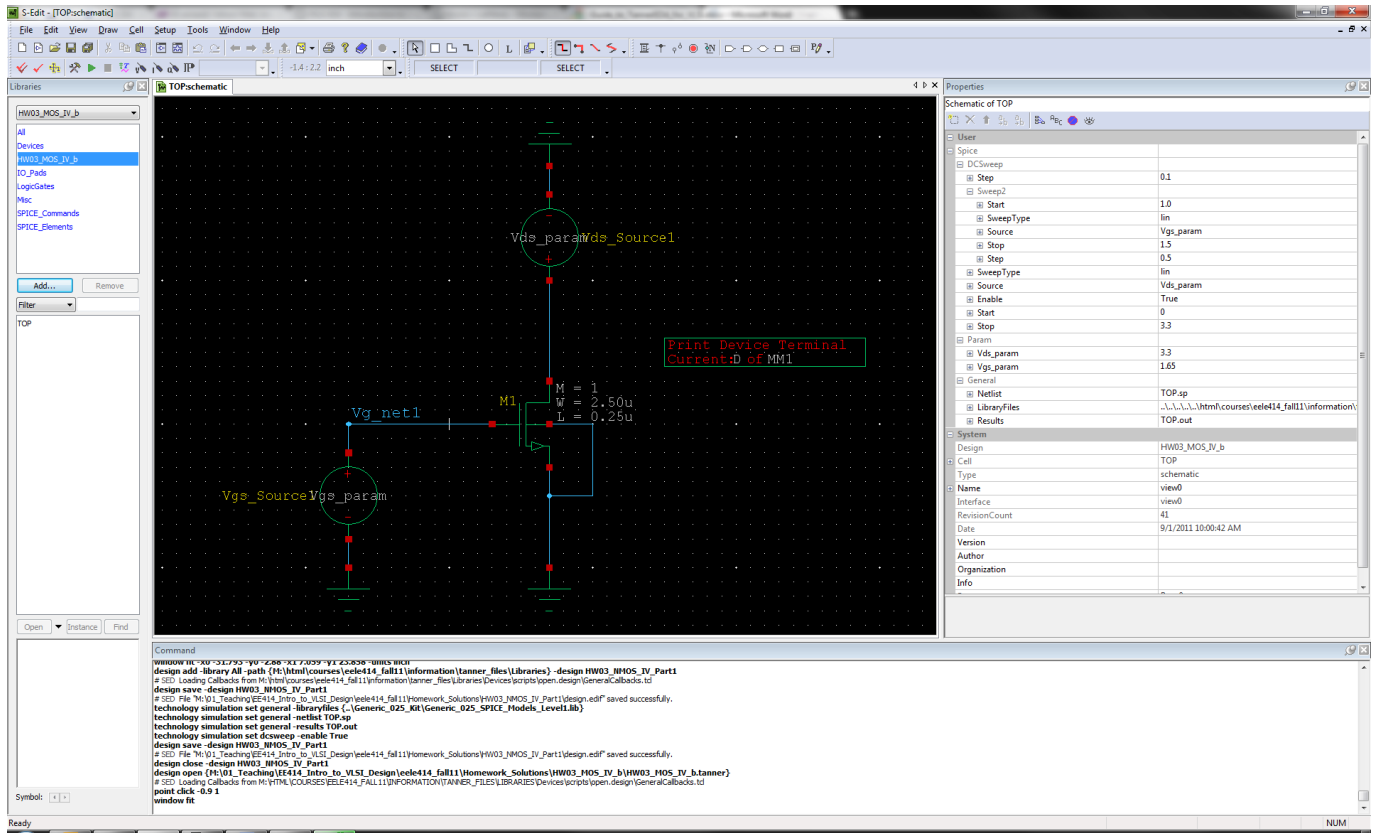
- Setup – SPICE Simulation

- In the dialog that appears, you should highlight “General” on the left.
- On the right, click in the “Library Files” field. This is where you will specify any SPICE models you will be using in your simulations. Browse & select “Generic_025_Kit\Generic_025_SPICE_Models_Level1.lib”
- On the right, click in the “SPICE File Name” field. This is where you specify the name and location of the SPICE Netlist output. Browse to your design directory “EELE414_VLSI_Fall2011\Tanner_Projects\HW03_NMOS_IV_Part1” and enter the filename “TOP.sp”.
- On the right, click in the “Simulations Results File Name” field. This is where the results of the simulation will be written. This file is what the waveform viewer will look for when you go to plot your results. Browse to your design directory “EELE414_VLSI_Fall2011\Tanner_Projects\HW03_NMOS_IV_Part1” and enter the filename “TOP.out”.
- Before you can exit this window, you will need to select an analysis type. We will setup the details of the analysis later, but for now, just check the “DC Sweep Analysis” and click “OK” to close the setup window.



Part 3: Enter the Schematic to simulate the IV behavior of an NMOS Transistor

We will be entering the following circuit.

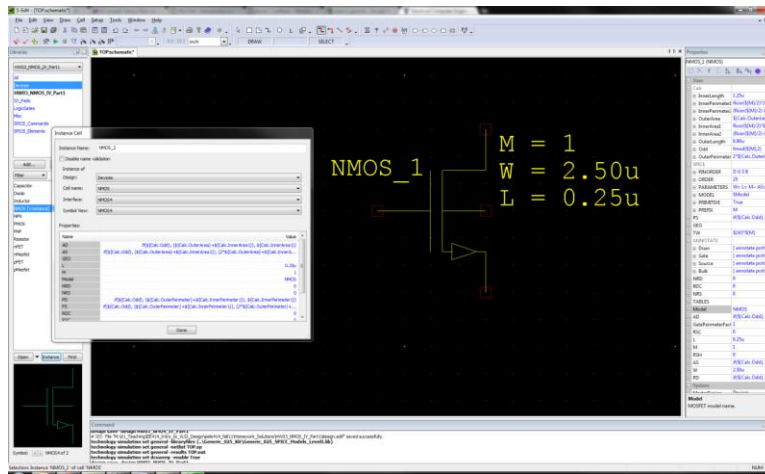


a) Enter the NMOS transistor

- On the left, click on “Devices” in the upper window. This will display all of the symbols available in this group. You should see all of the components that you can implement on a CMOS integrated circuit.

- On the bottom left window, click once on “NMOS”. You should see the symbol of the NMOS transistor show up in the symbol viewer window at the bottom.

- To place the NMOS, you will click on the “Instance” button. Two things happen when you click on this button. First, a dialog will appear that will allow you to setup the parameters for the NMOS. Second, the symbol will attach to your mouse. We will place the NMOS in the schematic first and then set its properties later. This is an easier way to enter the device. Click in the schematic window to drop an instance of the NMOS. Hit the “Esc” button to end the insert-mode.



The NMOS is now in the schematic.

A note on zooming:

- [Home] = zoom fit
- [-] = zoom out
- [=] = zoom in
- the scroll wheel also zooms in/out.

- To setup the NMOS, click on the NMOS symbol. You will see the properties of the device on the left. We want to setup the following:

- Model : enter "NMOS". This model is found in the Generic_025 library you added
- Name: M1. The SPICE designation for MOS transistors is to have the name start with an "M". S-edit automatically appends an M to the name is the final name will be "MM1" in the TOP.sp file. But it is good practice to name all MOS transistors with M's.
- W Set to 2.5u. This is the default.
- L Set to 0.25u. This is the default.

b) Enter a DC source for VGS

- Using the same process you used for the NMOS symbol, enter a "SPICE_Elements:VoltageSource". This is a generic voltage source symbol that is configured as a DC, TRAN, PWL, etc.. in its properties dialog.
- Click on the voltage source and enter the following:

- MasterInterface: DC (this is the default but this is how you would change it to something else.
- Name: VGS_Source (it is a good idea to use descriptive names)

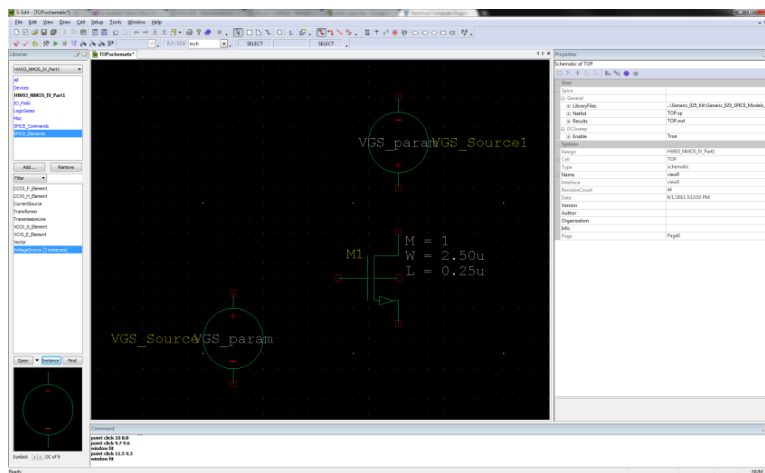
- V This is where you will set the DC voltage (i.e., 4v, 5v). However, for this example we will use a parameter instead of a hardcoded value. We will enter a parameter name here and then set up the parameter later. Enter “VGS_param” for the value of V. When performing a DC sweep, you must use parameters for the sweep.

c) Enter a DC source for VDS

- Using the same process as above, enter a DC source for VGS with the following:

- MasterInterface: DC (this is the default but this is how you would change it to something else.
- Name: VDS_Source
- V “VDS_param”

Position the sources as in the following figure:

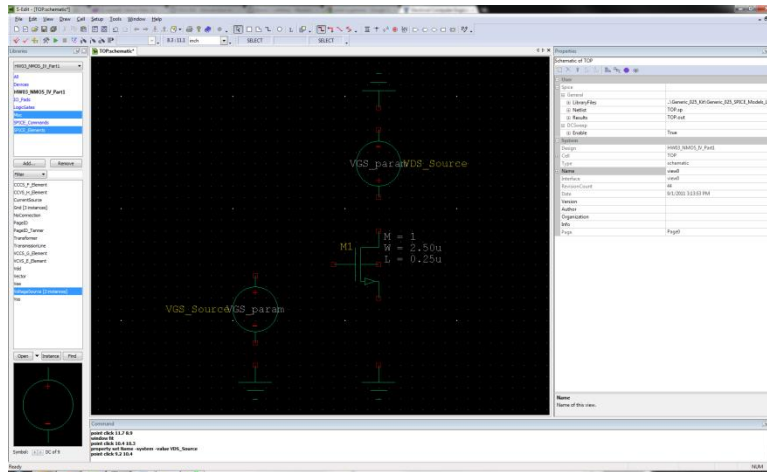


A note on zooming:

- **Hold down ALT-M to move a component. While holding these buttons down, click and drag the components.**
- **To rotate, click on the device and click the [r] button.**

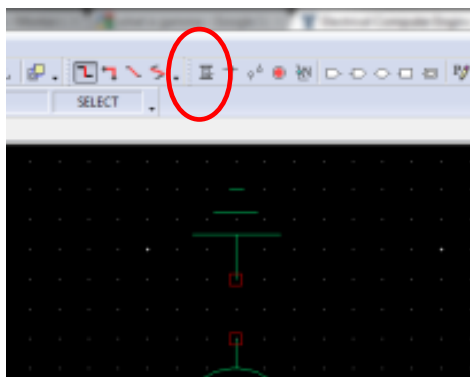
d) Enter Grounds

- Using the same process as above, enter 3 grounds from Misc:Gnd



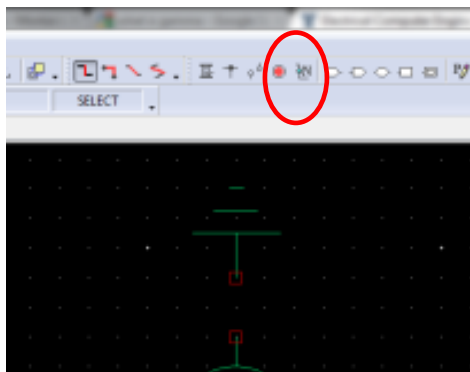
e) Enter Wires

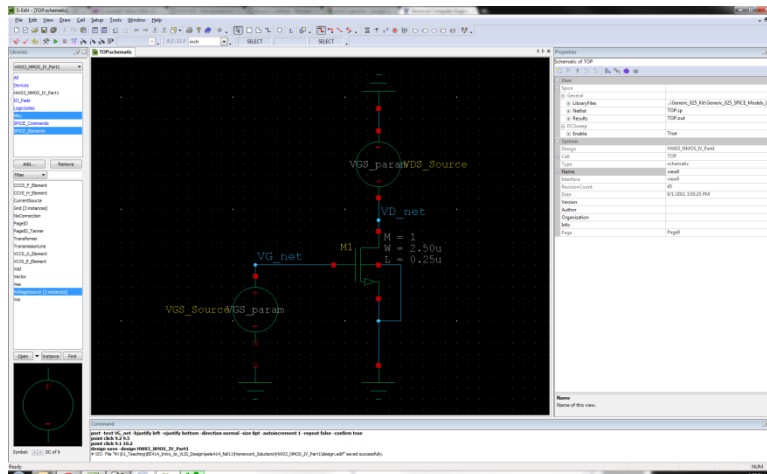
- You can enter wires by clicking on the “wire” icon at the top



- Enter wires by clicking on a symbol node and then dragging. Enter corners by clicking once where you want to turn.

- You can label nets using the “Net Label” icon at the top





f) Enter a Current Probe to monitor IDS

- Enter the SPICE_Commands:PrintCurrent component. This doesn't connect to anything. You just place it anywhere and then tell it what current to monitor in its properties dialog.

- In its properties dialog, setup:

Terminal: D (this is the Drain of the NMOS)

Device: MM1 (this is the name of the device. Notice that we called it M1, but S-edit automatically appends another M to the name. You will only see this once you run the Netlist.

Analysis: DC (**VERY IMPORTANT TO SELECT THIS!!!!**)

Part 4: Setup the Parameters that will be used during the DC sweep analysis

When we entered the VGS and VDS sources, we set their values to "VGS_param" and "VDS_param". We now need to setup these parameters.

Using the pull down menus:

- Setup – SPICE Simulations

- On the left, click on "Parameters"

- On the right, click on the "Add Parameters" button (it is in the upper right corner next to the red X)

Enter: Name: VGS_param
Value: 1v

- On the right, click on the "Add Parameters" button

Enter: Name: VDS_param
Value: 2.5v

We will overwrite these values during our sweep, but the parameters need to exist first.

Part 5: Setup the SPICE DC Sweep Analysis

Using the pull down menus:

- Setup – SPICE Simulations
- On the left, click on “DC Sweep Analysis”
- On the right, enter the following for Source (this is what will be swept)

Source or Parameter Name:	VDS_param
Start Value:	0
Stop Value:	2.5
Step:	0.1
Sweep Type:	lin

- On the right, enter the following for Source (this is what will be swept)

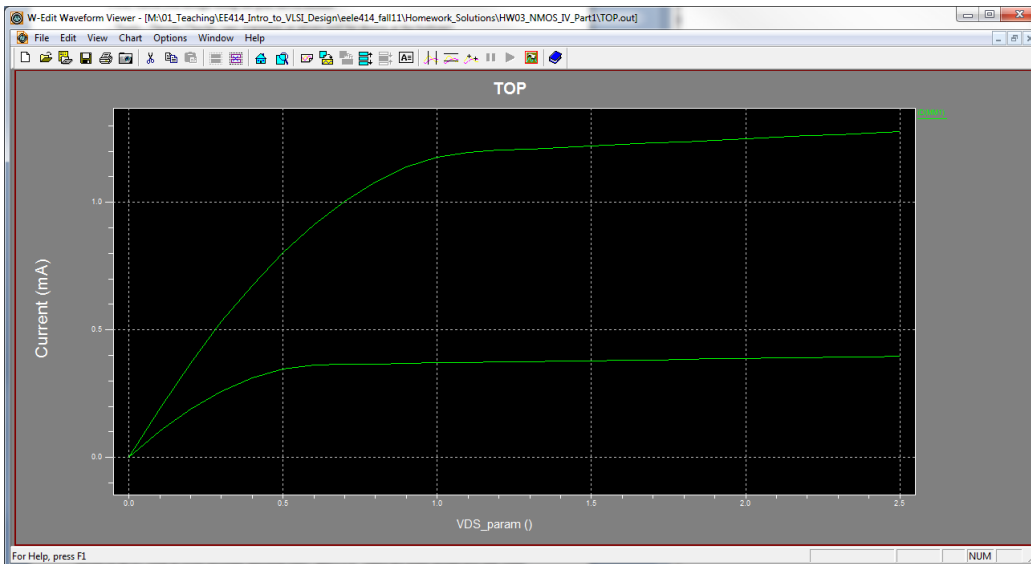
Source or Parameter Name:	VGS_param
Start Value:	1
Stop Value:	1.5
Step:	0.5
Sweep Type:	lin

NOTE: The first parameter you setup in this dialog will be plotted on the independent axis.

Part 6: Simulate the Design

- a) First, check you design using the pull down menus:
 - Tools – Design Checks (any warnings or errors will be shown at the bottom)
- b) Simulate your design:
 - Click on the Green Arrow to start the simulator:

The T-Spice window will appear. If everything is OK, the waveform viewer will also appear. If everything worked, your waveforms should look like this:



c) View the Netlist:

- In the T-spice window, right click on the file at the bottom and select “Show Netlist”

This will bring up the TOP.sp Netlist that was created and used by the spice engine. This is a good place to look when you get errors. This is the text based description of what you entered in S-edit.

```

* SPICE export by:  SEDIT 12.61
* Export time:     Wed Sep 07 15:22:50 2011
* Design:         HW03_NMOS_IV_Part1
* Cell:          TOP
* View:          view0
* Export as:     top-level cell
* Export mode:   hierarchical
* Exclude .model: no
* Exclude .end:  no
* Expand paths: yes
* Wrap lines:   no
* Root path:    M:\01_Teaching\EE414_Intro_to_VLSI_Design\eele414_fall11\Tanner_Projects\HW03_NMOS_IV_Part1
* Exclude global pins: no
* Control property name: SPICE

***** Simulation Settings - General section *****
.lib "M:\01_Teaching\EE414_Intro_to_VLSI_Design\eele414_fall11\Tanner_Projects\Generic_025_Kit\Generic_025_SPICE_Models_Level1.lib"

***** Simulation Settings - Parameters and SPICE Options *****
.param VDS_param = 1
.param VDS_param = 2.5

----- Devices: SPICE.ORDER > 0 -----
MM1 Vd_net VG_net Gnd Gnd NMOS W=2.5u L=250n AS=2.25p DS=6.8u AD=2.25p PE=6.8u
VVDS_Source Vd_net Gnd DC VDS_param
VVGS_Source VG_net Gnd DC VGS_param
.PRINT DC ID (MM1)

***** Simulation Settings - Analysis section *****
.dc lin VDS_param 0 2.5 0.1 lin VGS_param 1 1.5 0.5

***** Simulation Settings - Additional SPICE commands *****
.end

```

Status	Input file	Output file	Options	Start Date/Time	Elaps...
Failed	M:\01_...	TOP.out		September 07,2011 15:22:26	00:0...
Finished	M:\01_...	TOP.out		September 07,2011 15:22:50	00:0...

d) View the Waveform:

- If the windows viewer did NOT automatically appear, you can click on the file in the T-spice window and select “Show Waveform”

Example: Transient Analysis of a CMOS Inverter & Symbol Creation

Part 1: Start a New Design, Setup Libraries & Setup Simulation

- a) In this example, we will create a CMOS inverter and simulate its transient response. We will create an inverter design that contains a symbol and then instantiate it in another schematic to stimulate the circuit.

Symbols are handled by adding another view to a design. We will start by creating a design called “Inverter” and then create a schematic view. This schematic will contain an NMOS and PMOS wired as an inverter. We will add “Ports” for the Input, Output, VDD, and VSS. We will then add a symbol view to this design. The symbol will contain the inverter shape and the corresponding pins for Input, Output, VDD, and VSS.

We will then create a separate schematic called TOP that will be used to test the inverter. We will instantiate the inverter symbol in TOP. We only want to put items into the inverter design that can be fabricated. TOP will contain the ideal voltage sources to provide the input waveform, the power supplies, and a mock load. In this way, when we go into physical design (i.e., layout), we only drive forward the isolated circuits.

- Start S-Edit

- Create a new design called:

“EELE414_VLSI_Fall2011\Tanner_Projects\HW04_INV_Transient_Part1”

- Add the Tanner_Projects\Libraries\All\All.tanner library to the library list on the left

- Create a new Cell called “TOP” using the Pull Down Menus

- Cell - New View

Name = TOP
View Type = schematic

- Setup the simulation using the Pull Down Menus:

- Setup – SPICE Simulation

- Highlight the General Tab of the Setup SPICE window and set the following:

SPICE File Name: \HW04_INV_Transient_Part1\TOP.sp

Library Files: ..\Generic_025_Kit\Generic_025_SPICE_Models_Level1.lib

Simulation Results File Name: File Name: \HW04_INV_Transient_Part1\TOP.out

- Check the “Transient/Fourier Analysis” box on the left and set the following:

Stop Time = 2ns
Maximum Time Step = 10ps

- Click “OK”

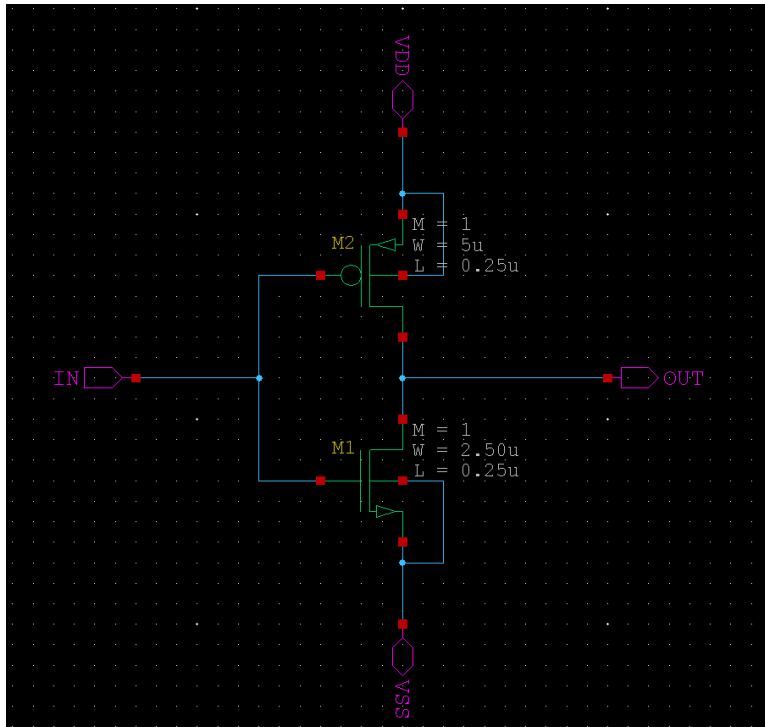
Part 2: Create the Inverter

a) Create a new schematic view using the pull-down menus:

- Cell - New View

Name = Inverter
View Type = schematic

b) Enter the inverter schematic:



- Entering the NMOS:

Name = M1
L = 0.25u
W = 2.5u
Model = NMOS

- Entering the PMOS:

Name	= M2
L	= 0.25u
W	= 5.0u
Model	=PMOS

- Entering the Ports:

Ports are entered using the icons on the top of the S-edit window.
Enter the following:

In Port:	Name it "IN"
Out Port:	Name it "OUT"
In/Out Port:	Name it "VDD"
In/Out Port:	Name it "VSS"

- Wire up the Inverter

Enter wire connections as shown in the previous figure.

c) Export a SPICE Netlist

Exporting a SPICE Netlist is a good idea in order to verify that you have entered the schematic correctly. Also, this Netlist will be used later when performing a "Layout versus Schematic (LVS)" check. We want to export a Netlist at the Inverter schematic cell level so that a Netlist of just the inverter exists for LVS. When we conduct the simulation of this inverter, we will create a TOP level schematic that will have a Netlist containing ideal voltage sources. This Netlist can't be used for LVS since it contains components that won't be fabricated.

With the schematic open, use the pull down menus to perform:

- File – Export – Export SPICE.
- Browse to your design directory and give the file name "Inverter.spice".
- Click "OK"

If you open the Inverter.spice with a text editor, you will see the following:

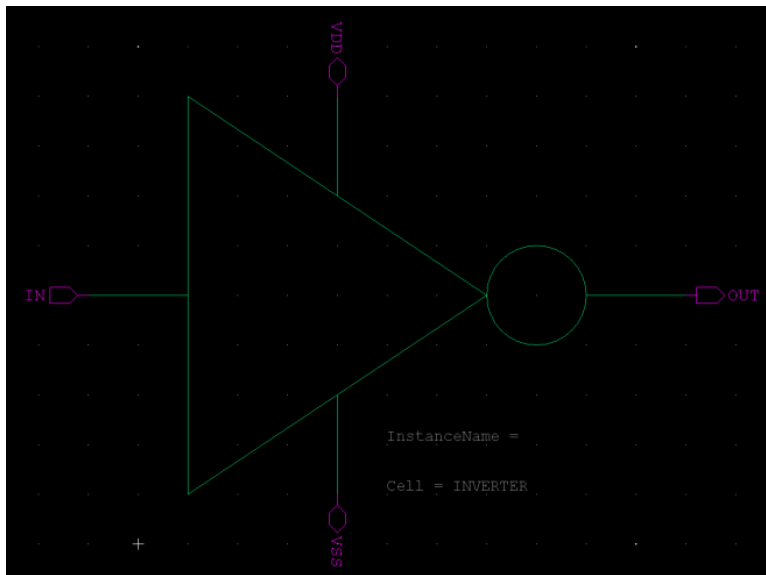
d) Create the Inverter Symbol

Symbols can either be created manually by creating a new symbol view or automatically by S-edit. We will use the automatic symbol generation. This will create a new symbol view from the schematic, create the ports for the symbol, and make a symbol shape. While the shape of the symbol is rarely what we ultimately want, it will do a lot of the work for us.

- With the schematic view open, use the pull down menus to create the symbol view:

Cell – Update Symbol

A new window will come up with a square symbol and 4 ports with the same names you entered in the Inverter:schematic view (i.e., IN, OUT, VDD, VSS). You should edit the shapes until you have created a symbol that looks like an inverter:



A note on drawing:

The “Path” icon will put you into a mode where you can draw lines that are not wires.

The “Circle” icon will allow you to enter the inversion bubble.

The ports can be moved by holding down “alt-m”

The ports can be rotated by selecting and pressing the “r” button

Remember to save.

Part 3: Create the TOP schematic to test the Inverter

- a) Instantiate the Inverter in the TOP schematic

Open the TOP schematic view using the pull-down menus:

- Cell – Open View:

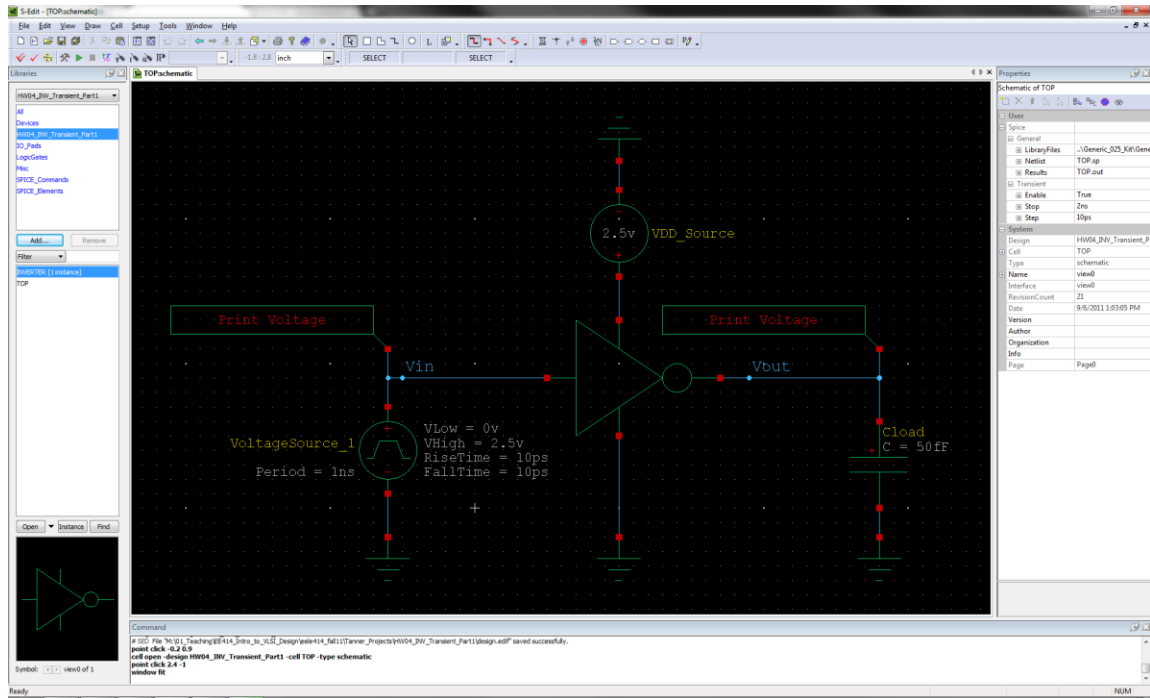
Cell Name: TOP
View Type: schematic

In the library windows on the left of the window, highlight your “HW04_INV_Transient_Part1” library. In the lower left window, you will see your two Cells “TOP” and “Inverter”.

- Click on “Inverter” and you will see your symbol show up in the symbol viewer.

- Click on the “Instance” button and place your symbol in the TOP schematic.

b) Enter the following circuit in order to power and stimulate your inverter:



- Enter the Pulse Voltage Source. All voltage sources are the same component in the SPICE_Elements library. The default is DC, but this can be changed to any other type of source in the properties dialog.

Name	= Vin_Source
MasterInterface	= Pulse
Period	= 1ns
PulseWidth	= 0.5ns
VHigh	= 2.5v
VLow	= 0v
RiseTime	= 10ps
FallTime	= 10ps

- Enter a Load capacitor from the Devices library.

Name	= Cload
C	=50fF

- Enter a DC Source for VDD

Name	= VDD_Source
MasterInterface	= DC
V	= 2.5v

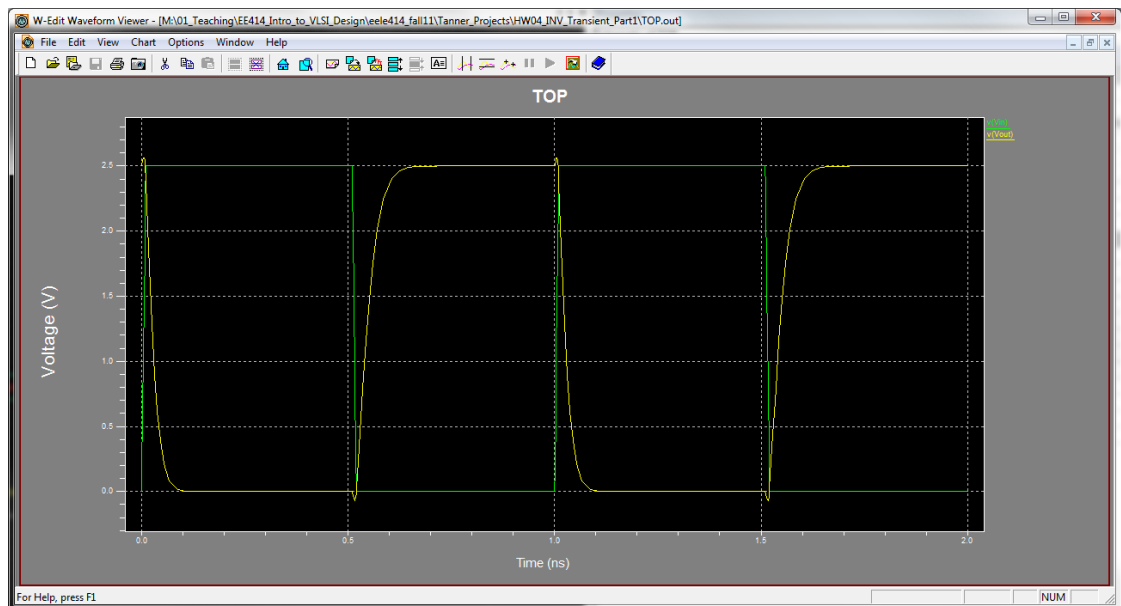
- Enter the grounds from the Misc library

- Enter wire connections and name them Vin and Vout
- Enter a voltage probe for both Vin and Vout

Part 4: Simulate the Design

- First, check you design using the pull down menus:
 - Tools – Design Checks (any warnings or errors will be shown at the bottom)
- Simulate your design:
 - Click on the Green Arrow to start the simulator:

The T-Spice window will appear. If everything is OK, the waveform viewer will also appear. If everything worked, your waveforms should look like this:



Using L-Edit (IC Physical Design Tool)

L-edit is an integrated circuit physical design tool from Tanner EDA. This tool allows you to draw the layout of an IC, look at cross-sections, perform DRC (design rule check), and generate a Netlist of your layout so that you can perform LVS (layout versus schematic) using a different tool.

Part 1: Launch L-edit, Start a design, and Setup the Technology

- a) Log onto a computer in the digital lab (601 Cobleigh) and launch L-edit using:

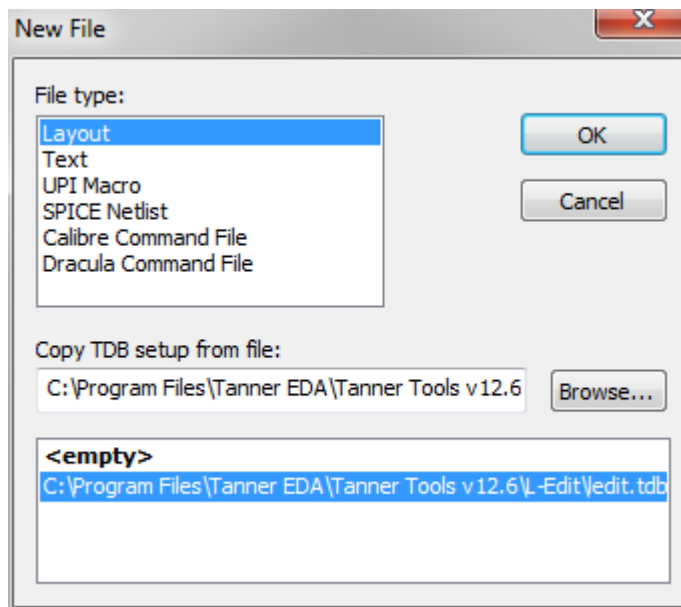
Start – All Programs – Tanner EDA – Tanner Tools v12.6 – L-Edit v12.6

- b) Create a new layout design:

- File – New
 - select “Layout”
 - under “Copy TDB...”, browse to:

\Tanner_Projects\Generic_025_Kit\Generic_025.tdb

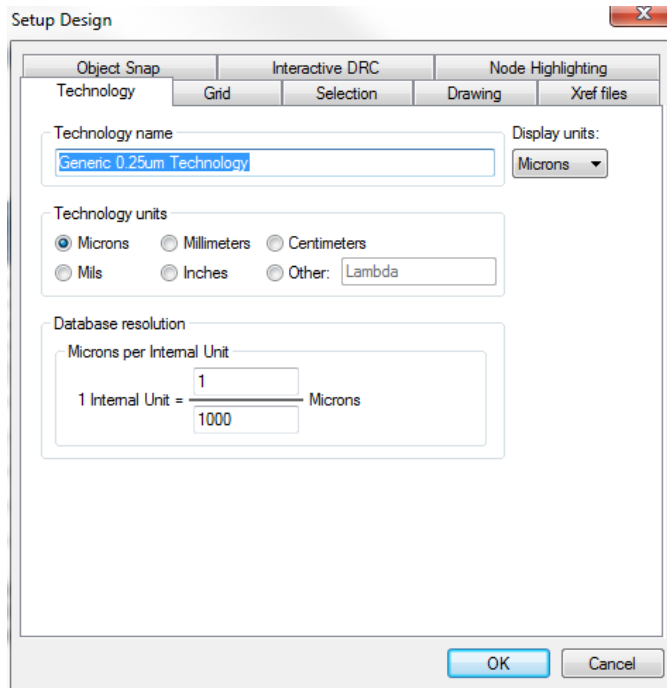
- Click “OK”



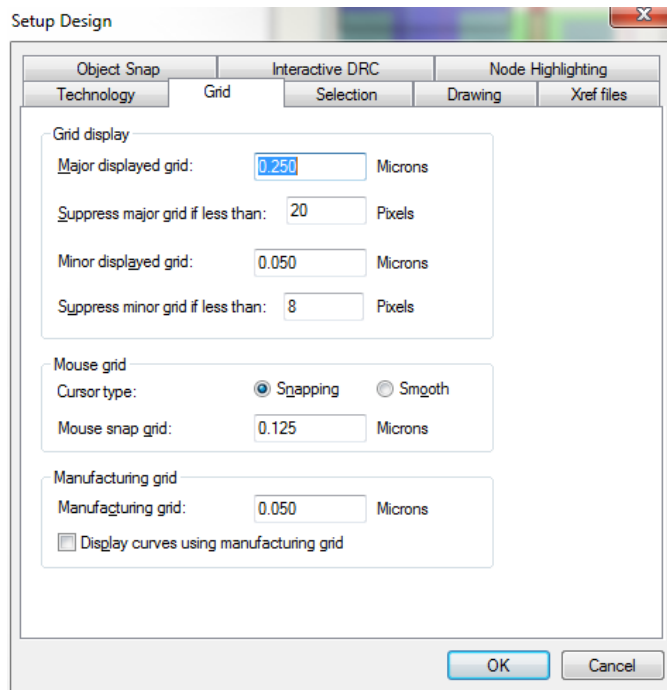
When you copy in the Generic_025.tdb files, it loads all of the layer definitions for the 0.25um process and the design rule information. On the left, you should see a set of layers for this technology that can be used to create devices.

- c) Verify the technology rule options & setup grid

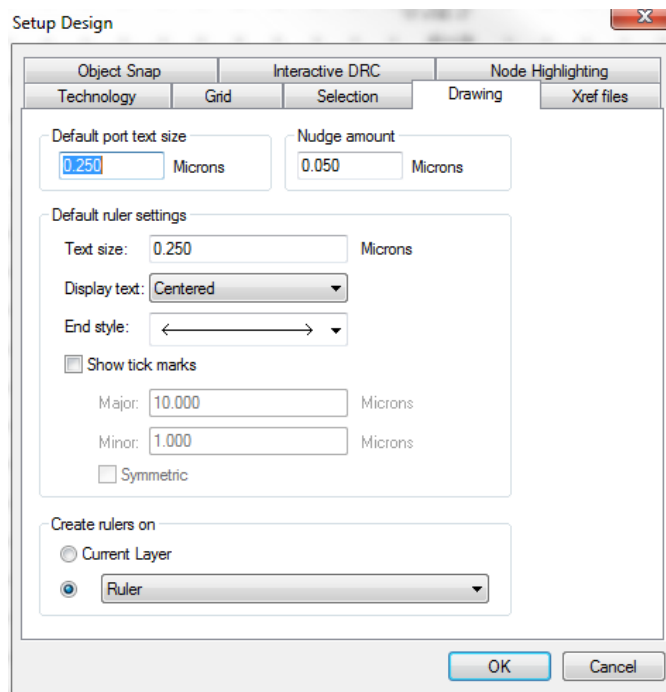
- Setup – Design



Now you want to setup the grid. Click on the “Grid” tab. Since we are using a 0.25um grid, let’s put our major grid and snap grid at 0.125um. Then we will put our minor grid at 0.05. Enter the following:



Now let's configure the ruler settings. When you draw polygons to implement your circuitry, you will continually be measuring your shapes to make sure they are what you want. You can place items called "rulers" that will show how large your shapes are. Click on the "Drawing" tab and configure the "Display Text" to "Centered".



d) Save your design

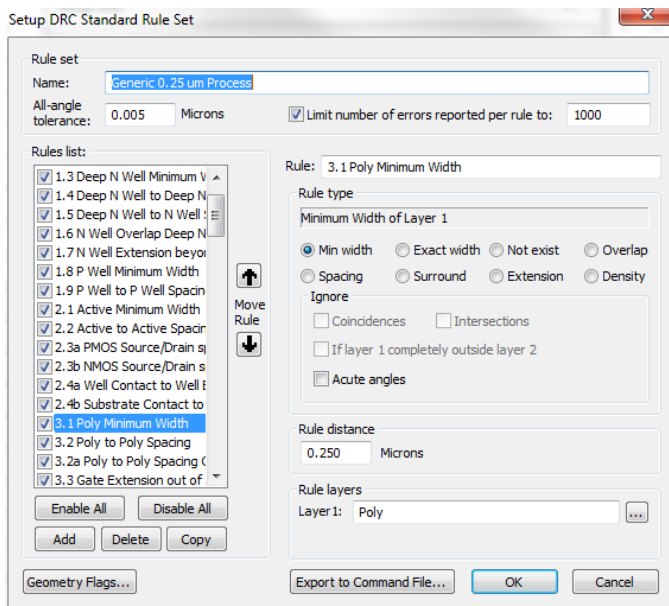
- Now you can click "save" and give your design a descriptive name and location. (i.e., \Tanner_Projects\HW07_INV_Layout_Part1")

Part 2: Inspect the design rules for the kit

The design rules for this kit were loaded when you specified the Generic 0.25um design kit. L-edit will check for violations in the design rules using a process called Design Rule Check (DRC). To see the rules, use the pull down menus:

- Tools – DRC Setup

- You'll see that the "DRC Standard Rule Set" is selected. Highlight this (if it isn't already) and click the "Edit" Button:



At this point, the only rule that makes much sense is the minimum gate length. If you click on Rule 3.1. Poly Minimum Width, you'll see that a DRC error will occur if you draw a shape on the Poly layer that is less than 0.25um in width. As you can also see, there are rules that govern all of the layers in the design kit.

- Once you look at the rules, click "OK" to go back to the "Setup DRC" dialog and check the "Pop up message box" so that you can see the results of the rule checking.

Part 3: Create your layout for the CMOS inverter

Let's create a CMOS inverter with $L_n=L_p=0.25\mu\text{m}$, $W_n=2.5\mu\text{m}$, $W_p=5\mu\text{m}$. This will match the inverter that you created in the second example in this tutorial and will allow us to perform an LVS check.

NMOS

The process that we are using is N-well CMOS. This means that the blank screen you see a p-type silicon substrate. We explicitly draw active regions on the screen to open up the field-oxide to insert diffusion regions. This means you can think of the screen as p-type silicon with FOX everywhere on it to begin with. In order to create the NMOS structure, we use three layers:

- | | |
|----------|---|
| N-Select | - This layer tell where the field-oxide should be opened up for the active regions. An N-select rectangle must be slightly larger than the shape defining where the implants go. |
| Active | - This tell the process where to implant the n-type ions (P or As). Remember that we want to implant into the Poly to reduce its resistance. The "Width" of the N-Select dictates the width of the transistor (W_n) |
| Poly | - This specifies the gate of the device. Under the poly will be thin oxide forming MOS structure. The "Length" of the Poly dictates the length of transistor (L_n). |

Display Notes

- You can setup the default units to use (micron vs. lambda) in the upper corner of the screen. If you are getting confusing measurements, make sure that this box is in the units you want.
- You can setup the grid display and snap using the "Setup – Design" menu and "Grid" tab. Doing this on the fly sometimes helps you draw faster.

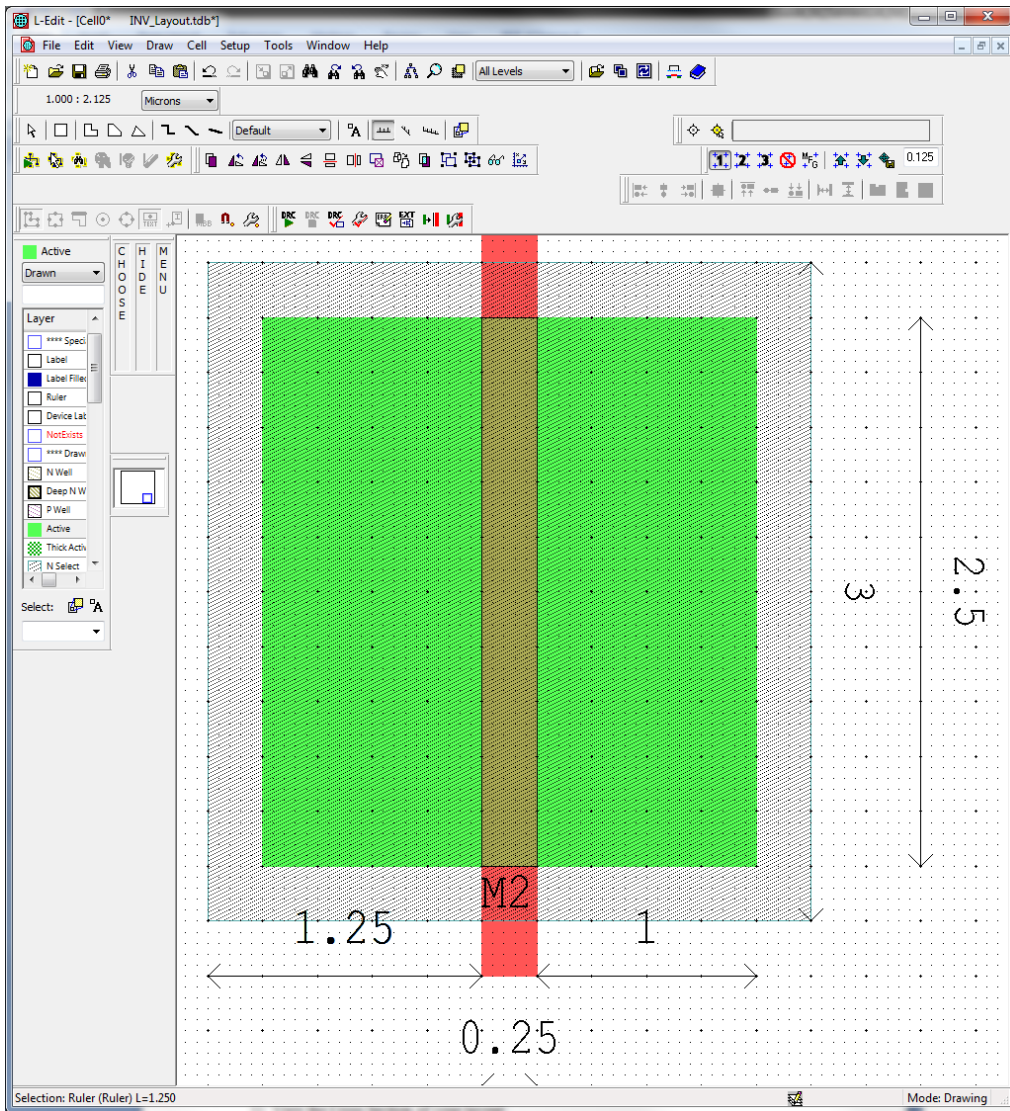
Entry Notes:

- You enter a rectangle by first selecting the layer and then clicking on the *square* icon.
- You can enter rulers in your design to measure your rectangles as they are entered. You can set the display options of the ruler on the "Setup – Design" menu on the "Drawing" tab.

a) Create the NMOS Structure

- Enter an N-select rectangle that is $2.75\mu\text{m} \times 3\mu\text{m}$
- Enter an Active rectangle that is $2.25\mu\text{m} \times 2.5\mu\text{m}$ (W_n) centered within the N-select
- Create a Poly rectangle that is $0.25\mu\text{m}$ (L_n) \times $3.5\mu\text{m}$ centered within the Active.

Your design should look like this:

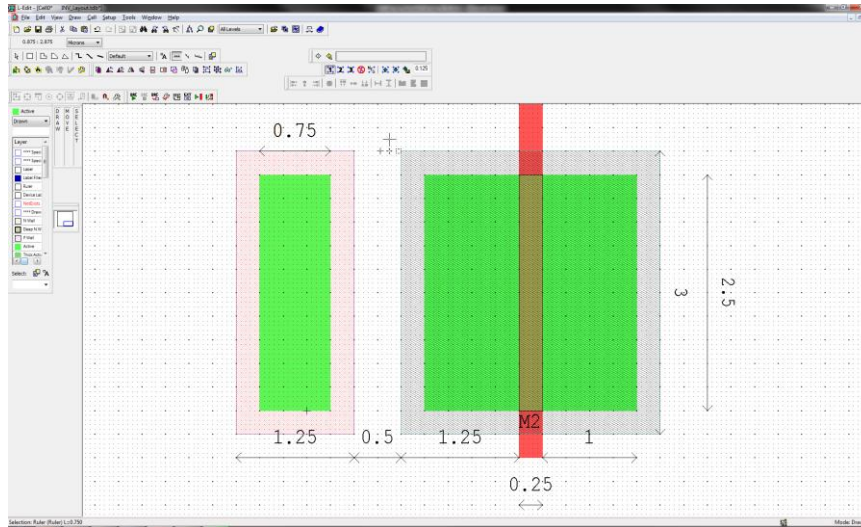


b) Run DRC to make sure your dimensions are not violating any design rules

- Click on the DRC button in the upper left corner of the screen (little green play arrow). If everything checks out, you should a pop up that says it passed DRC.

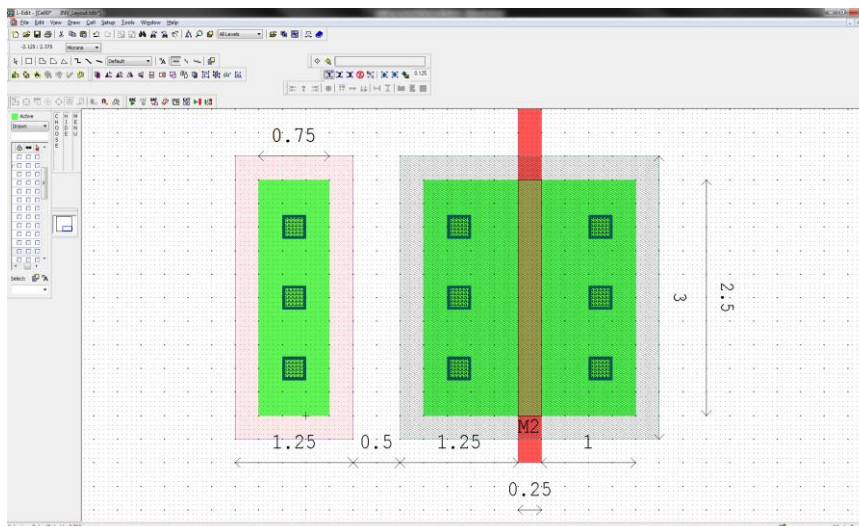
c) Enter the Body Diffusion point for the NMOS

- In order to enter a body contact, we need to tell the tool that we are going to create a p+ diffusion region. We do this using the active and P-select layers. We again use the Active layer to represent that ion implantation will be needed. Put a substrate diffusion region next to your NMOS as follows using P-Select and Active:

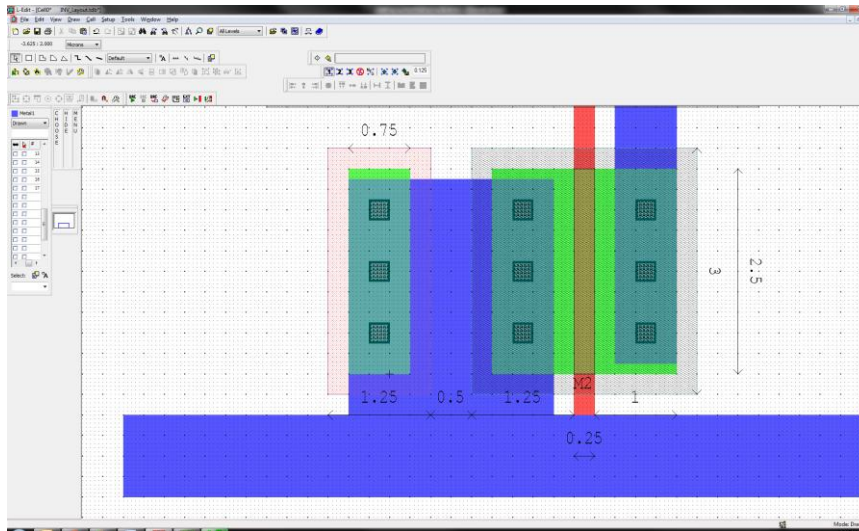


d) Enter the contact windows for the NMOS

- we do this using the Active Contact layer. We want to put as many as possible without violating DRC.

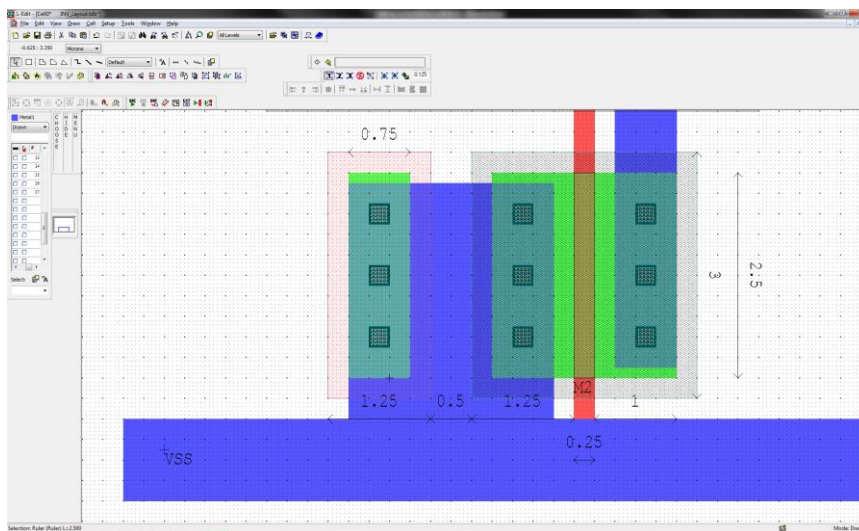


- e) Enter Metal 1 to connect the Source and Body of the NMOS together. Also add metal from this connection down to a VSS rail (named later). Put Metall over the Drain contact to connect to later.



- f) Assign a net label to the VSS rail.

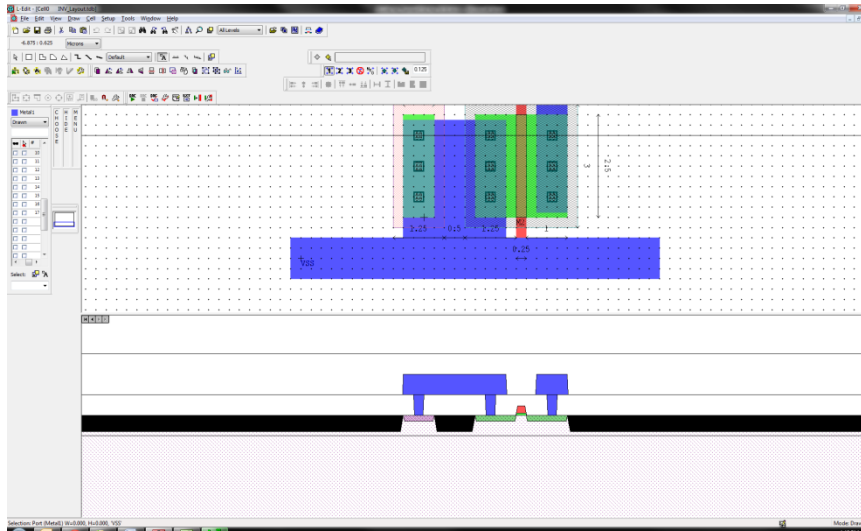
- Click on the “Switch to Drawing Ports” icon (it looks like a little square next to an “A”).
- Now that you are in the Port naming mode, click on the VSS rail and a dialog will appear.
- Enter “VSS” for the Port name



- g) Look at the cross-section of the NMOS to ensure everything is correct.

- Using the pull down menus, perform:
 - Tools – Cross Section

- You will first need to provide the Generic 0.25um process definition file (*.xst). Browse to “..\Generic_025_Kit\Generic_025.xst”
- You will then need to specify where you want to take the cross-section. Click the “Pick” button and then click on one of the upper active contacts:
- Click “OK”

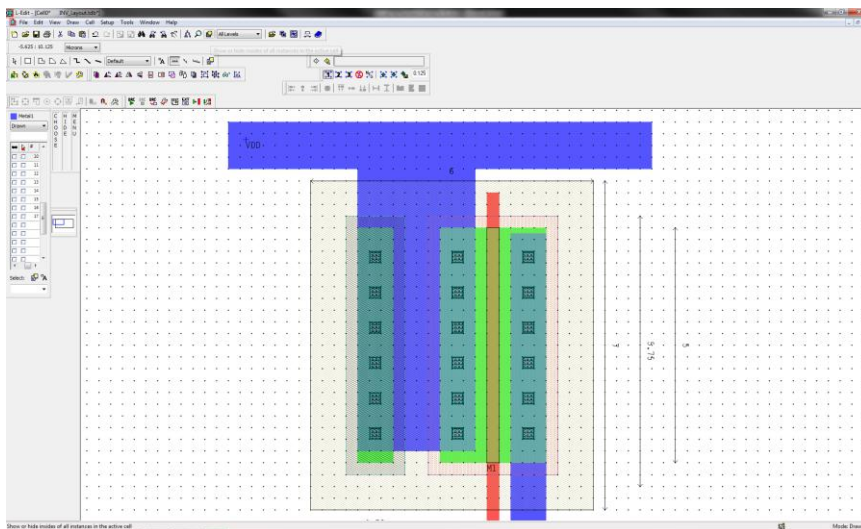


- Perform another DRC to ensure everything is OK

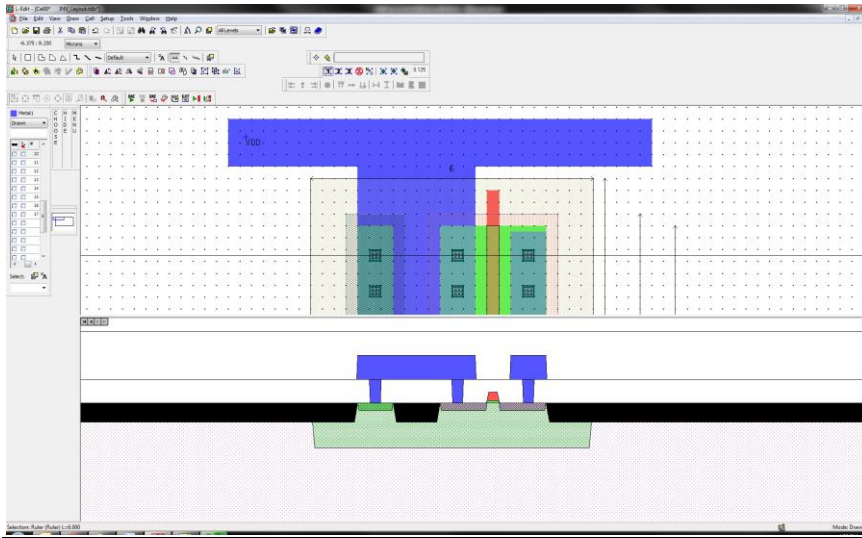
PMOS

A PMOS device is made in a similar manner as the NMOS except that we need to specify the N-well and use P-select instead of N-select. Enter a PMOST as follows:

- Enter the PMOS N-well, P-select, Active, Poly, Active Contact, and Metal 1 as follows:



b) Take a cross-section to verify everything is OK



You should clearly see the N-well used to create the PMOS substrate.

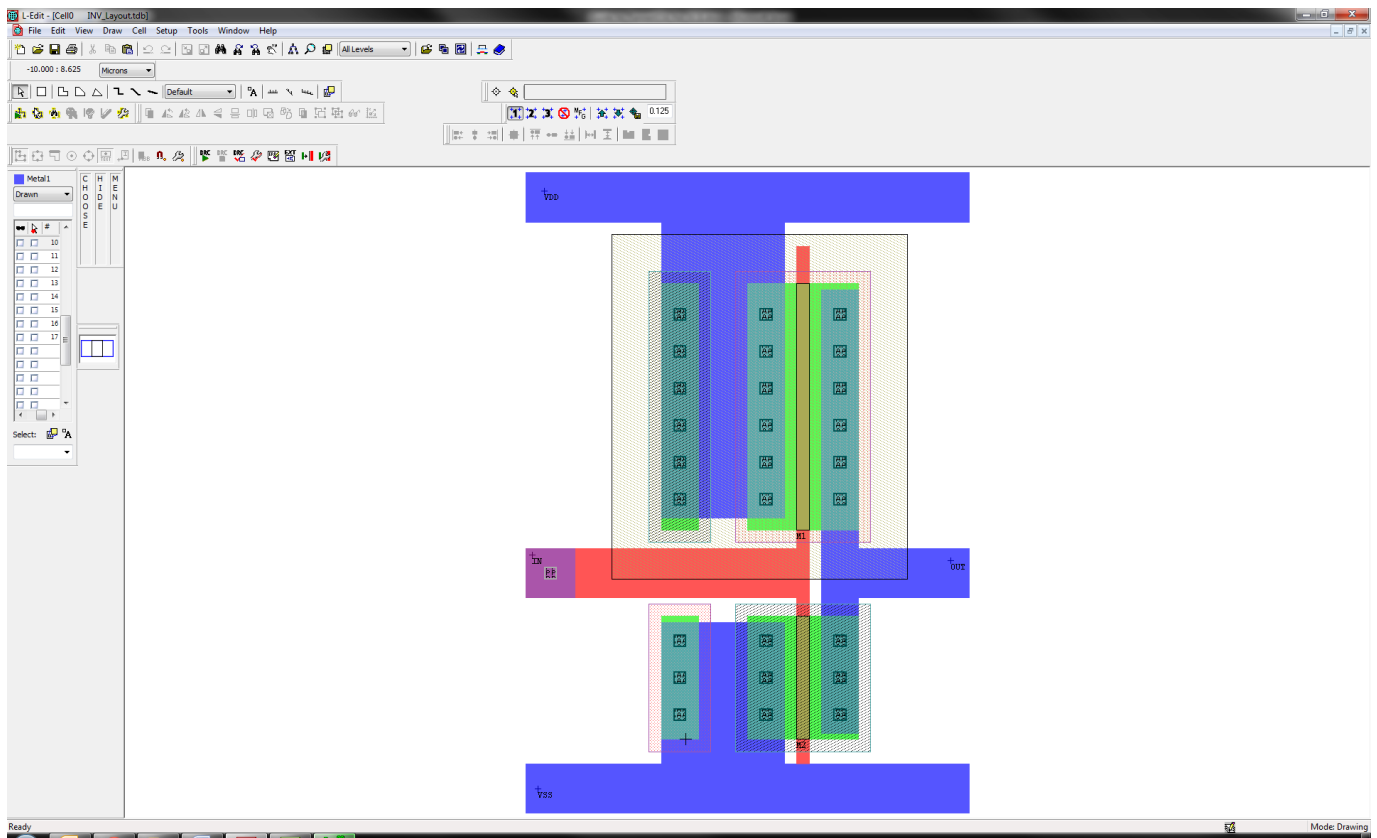
c) Label the top rail “VDD”

Connecting the Inverter

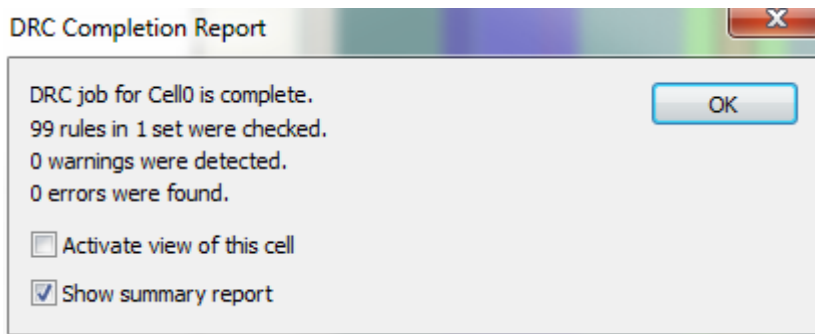
Metal and Poly are connected together by simply drawing rectangles that are adjacent to or overlap another rectangle of the same type (i.e., M1 to M1, Poly to Poly).

a) Connect the inverter together as shown in the following figure:

- Connect the gates together using Poly and then route the signal up to Metal 1 using a Poly Contact
- Connect the drains together using Metal 1
- Label the input Metal 1 “IN”
- Label the output Metal 1 “OUT”



Perform a Final DRC on the Design



Extract a SPICE Netlist of your Layout

Using the pull down menus, perform:

- Tools – Extract

You will need to provide an extraction file for this process (*.ext)

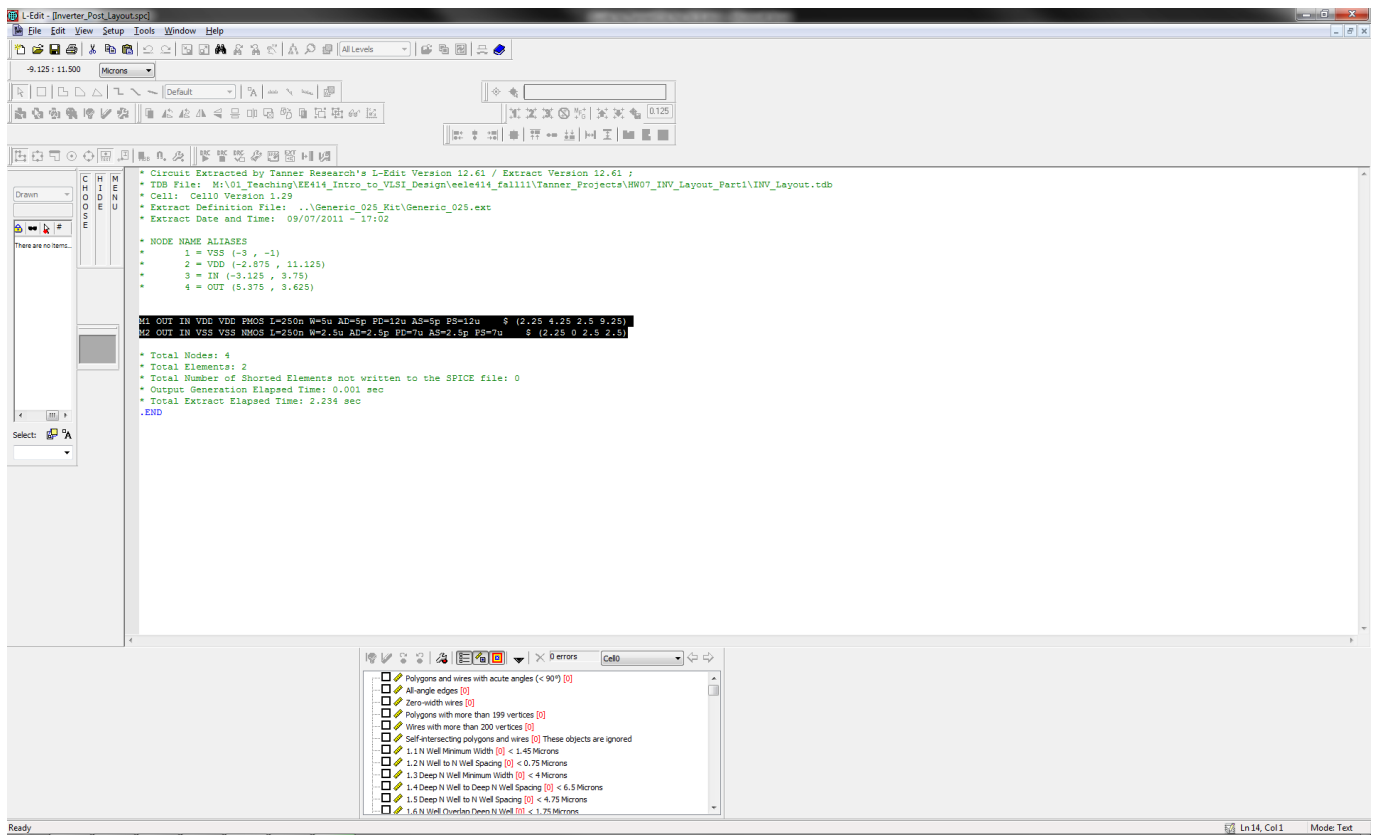
- Browse to “..\Generic_025_Kit\Generic_025.ext”

You will want to provide a SPICE output file. Browse to your design directory for this example and provide the name “Inverter_Post_Layout.spc”

- you will want to check the boxes:

- General: Label all devices
- General: Open SPICE output file after opening
- Output: delete the “include SpecialDevices.md” line in the SPICE include statement box

- Click “Run”



Notice that the extraction tool found two transistors (PMOS and NMOS) with the sizes that we intended.

Using LVS (Layout versus Schematic Checking Tool)

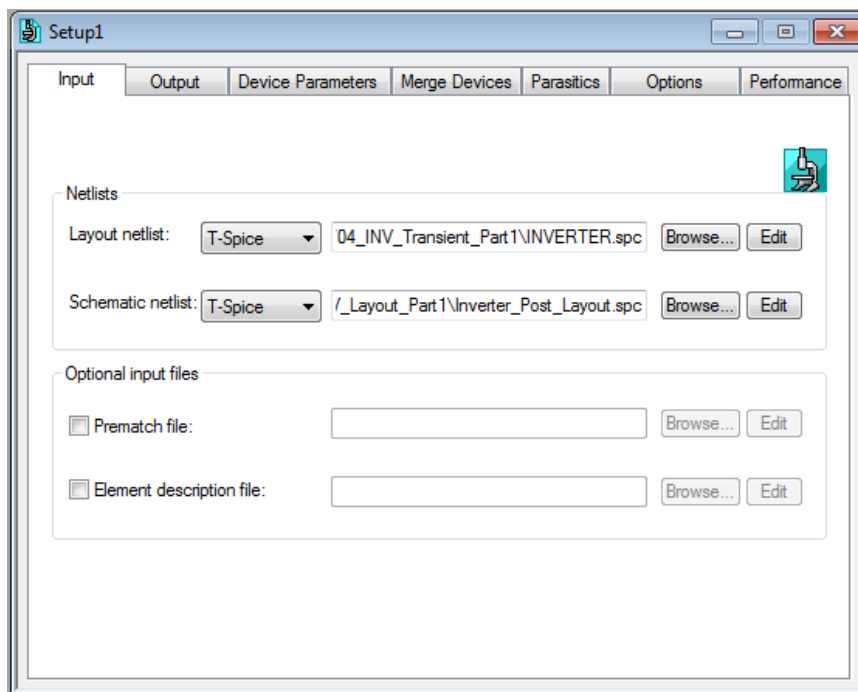
We always want to ensure that the layout we have created is what we intended in the schematic. LVS will compare the Netlist exported from S-edit and the Netlist exported from L-edit.

Start the LVS Tool using the Start Menu:

- Start – All Programs – Tanner EDA – Tanner Tools v12.6 – LVS v12.6

Using the pull down menus in the LVS tool, perform:

- File – New
- Select “LVS Setup”
- In the dialog that appears, browse to the Netlist you exported from S-edit for your Inverter (Inverter.spic)
- In the dialog that appears, browse to the Netlist you exported from L-edit for your Inverter (Inverter_Post_Layout.spic)



- Click the “Run Verification” icon (little green arrow) to perform LVS.
- If everything matches, you will see a report window that says “Circuits are equal” in red. If it does NOT match, you will be given a report showing what is wrong.

