



Course Title and Code Number:  
 Digital Integrated Circuits (EE 431)  
 Fourth Year (Communications and Electronics)  
 Time Allowed: 90 Mins

اسم المقرر والرقم الكودي له:  
 الدوائر المتكاملة الرقمية (EE 431)  
 السنة الدراسية الرابعة (اتصالات و إلكترونيات)  
 الزمن: ٩٠ دقيقة

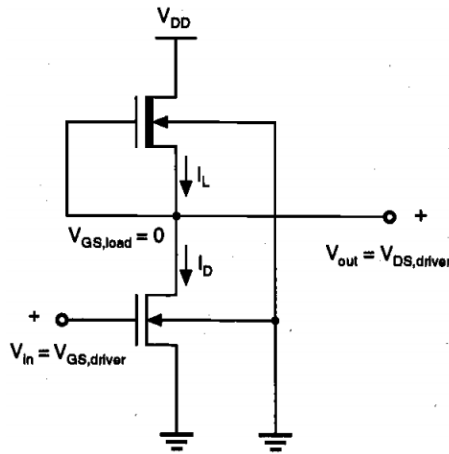
**Answer the following questions:**

**(25 marks)**

**Question 1:**

**(10 marks)**

Derive and calculate the critical voltages ( $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ ,  $V_{IH}$ ) and find the noise margins of the following depletion-load inverter circuit:



$$\begin{aligned}
 V_{DD} &= 5 \text{ V} \\
 V_{T0,driver} &= 1.0 \text{ V} \\
 V_{T0,load} &= -3.0 \text{ V} \\
 (W/L)_{driver} &= 2, \quad (W/L)_{load} = 1/3 \\
 k_{n,driver}' &= k_{n,load}' = 25 \mu\text{A}/\text{V}^2 \\
 \gamma &= 0.4 \text{ V}^{1/2} \\
 \phi_F &= -0.3 \text{ V}
 \end{aligned}$$

**Question 2:**

**(10 marks)**

A CMOS technology has the following parameters:

$$\begin{aligned}
 \mu_n C_{ox} &= 120 \mu\text{A}/\text{V}^2 & V_{T0,n} &= 0.8 \text{ V} \\
 \mu_p C_{ox} &= 60 \mu\text{A}/\text{V}^2 & V_{T0,p} &= -1.0 \text{ V} \\
 L &= 0.6 \mu\text{m} \text{ for both nMOS and pMOS devices, } & W_{min} &= 1.2 \mu\text{m}
 \end{aligned}$$

Design a CMOS inverter by determining the channel widths  $W_n$ , and  $W_p$  of the nMOS and pMOS transistors, to meet the following performance specifications (**Derive** all equations you need):

- $V_{th} = 1.5 \text{ V}$  for  $V_{DD} = 3 \text{ V}$
- Propagation delay times  $\tau_{PHL} \leq 0.2 \text{ ns}$  and  $\tau_{PLH} \leq 0.15 \text{ ns}$ .
- A falling delay of  $0.35 \text{ ns}$  for an output transition from  $2 \text{ V}$  to  $0.5 \text{ V}$ .

Assume a combined output load capacitance of  $300 \text{ fF}$  and ideal step input.

**Question 3:**

**(5 marks)**

Consider a uniform polysilicon line with a length  $l$  of  $1000 \mu\text{m}$  and a width  $W$  of  $4 \mu\text{m}$ . Assuming a sheet resistance value of  $30 \Omega/\text{square}$ , a parallel plate unit area capacitance of  $0.066 \text{ fF}/\mu\text{m}^2$ , and a fringing field unit length capacitance of  $0.046 \text{ fF}/\mu\text{m}$ . Calculate the propagation delay of the poly interconnect line using the following models:

- Lumped RC model.
- T model.
- Distributed RC ladder with  $N=5$ .
- Distributed RC ladder with  $N=\infty$ .

*Good Luck*

*Examiner: Dr. Mohammed Morsy*