University *of* Alexandria
Faculty of Engineering
Division of Communications & Electronics

Subject Name: Microprocessors **Lecturer:** Dr. Mohammed Morsy
Academic Year: 2012 – 2013 **Assistants:** Eng. Ahmed Bedewy

Third Year – Semester 1

SHEET 7 **Introduction to Hardware and Memory Address Decoding**

1) a) Differentiate between the microprocessor, microcontroller, DSP, FPGA, and ASIC computational elements and provide three application examples for each.

b) Draw the Von Newmann compute architecture, and briefly describe its advantages and limitations.

2) a) How many clock cycles are in the 8088/8086 bus cycle. Is this number always fixed?

b) Sketch in detail the memory bus cycle for the 8088/8086 microprocessor. Briefly describe the purpose of each state in the bus cycle including the wait state.

c) If the CLK input to the 8086/8088 is 4 MHz, how long is one bus cycle? How much time is allowed for memory access? How many MIPS is the 8086/8088 capable of obtaining when operated at this frequency?

d) Contrast minimum and maximum mode 8086/8088 operation.

3) a) What is the purpose of the ALE line in the 8088/8086?

b) Why are buffers and latches needed for the data, address and control buses of the 8088/8086 microprocessors?

c) Draw the demultiplexing and buffering circuits for the 8088 and 8086 microprocessors.

d) Why are memory address decoders important?

e) Using 64Kx8 SRAMs, determine the number of chips required to construct a memory interface to each of the following processors:

i) 8088 ii) 8086 iii) 80486 iv) Pentium

f) Sketch the bus timing waveform of a READ machine cycle for the 8086 processor.

g) The pinout of the 8284A and its internal circuitry is shown in figure 1 .Answer the following questions:

i) Which pin is connected to the clock of the microprocessor? If a crystal of 15 MHz is attached at pins 16 and 17, what is the operating frequency of the processor? If a memory chip of 500ns access time is interfaced with the processor,

does it require a wait state? Why? Which pin is responsible for the generation of the READY signal? Which pins are used to control the generation of the READY signal?

ii) Explain briefly how the clock signal is generated by two different methods using the pins (X1, X2, F/C, EFI and CLK)? If you need three chips of the 8284A clock generator, how many crystals do you have to buy to operate the three ICs? Explain your answer.

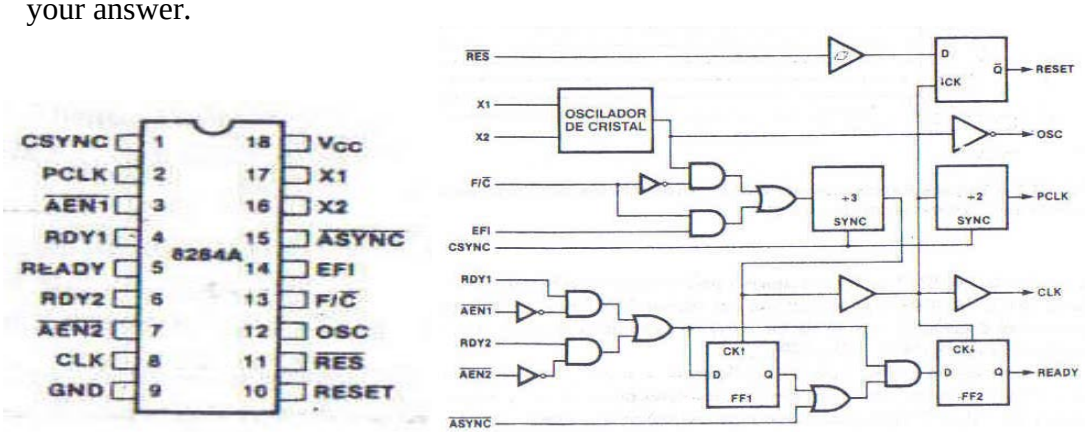

Figure 1.

4) For the shown memory in figure 2, find the range of addresses for each chip. If the 3-8 decoder 74138 is removed and we used a PAL 16L8 instead, draw the new circuit, and write down the equations describing the connections.

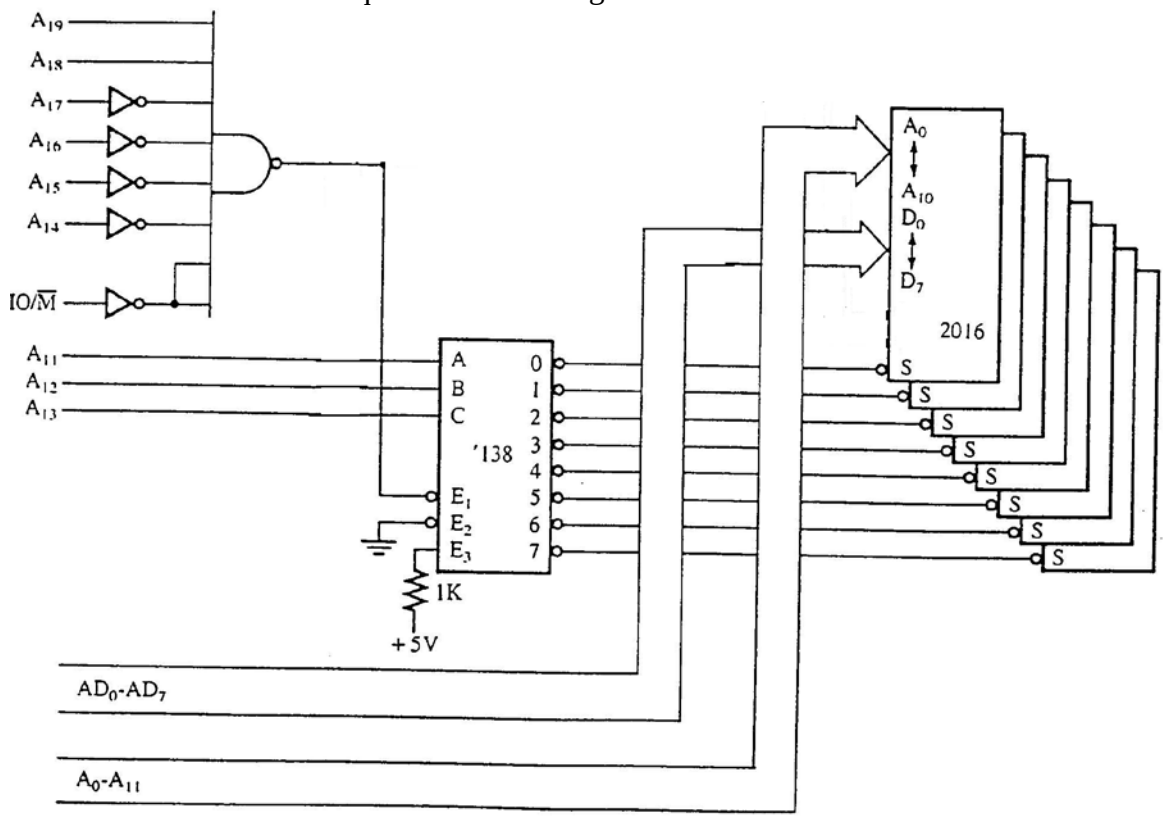

Figure 2.

5) Design a circuit showing how to interface 2732 EPROMs to the 8088uP using 74LS138 so that the memory range from 68000H – 6BFFFH is addressed.

6) Design a circuit showing how three 2732 EPROMs and two 2716 EPROMs to the 8088 microprocessor using one 74LS139 so that the memory range from 00000H – 03FFFH is addressed.

7) Design a memory system for the 8088 microprocessor consisting of:

a) ROM section using 2732 chips for the addresses from 00000H-02FFFH

b) RAM section using 4016 chips for the addresses from 06000H-06FFFH

8) Design a circuit showing how to interface 2732 EPROMs to the 8086 microprocessor using 74LS138 so that the memory required is 64KB starting at the address B0000H.

9) Consider an 8088 microprocessor with the following memory map. Design a decoding circuit to select the RAM0, RAM1 and ROM0 devices which consists of 2Kx8 chips. Use 74138 type devices (two low active enables and one high active enable) and any other standard logic gates

ROM	0C000-0FFFFH
MEMORY MAPPED IO	08000-0BFFFH
RAM1	04000-07FFFH
RAM0	00000-3FFFFH

10) a) Modify the circuit shown in figure 3 so that the EPROM is located at the memory address starting at B0000H and the RAM is located at the memory address starting at 10000H
b) Modify the new circuit so that the memories are doubled and starting at the same addresses
c) Modify the circuit in b) so that it can be connected to Pentium processor.

11) a) It is required to connect an 8088 to 8 ROM chips of 8KB each , starting at address A0000H.Show the connection indicating the range of addresses of each chip
b) Modify the circuit shown in figure 4 so that the Pentium processor is interfaced with 8 1MBx8 chips
c) If a 74138 decoder is used to connect the circuit in b) with starting address F0000000H, show the connection lines to the decoder.

12) a) Explain how odd parity is stored in a memory system and how it is checked.
b) Calculate the CRC value for the 16-bit data streams 48F9H, 538AH.
c) Test if these code words are correct, assuming they were created using an even parity Hamming Code. If one is incorrect, indicate what the correct code word should have been. Also, indicate what the original data was.

- 010101100011
- 111110001100
- 000010001010

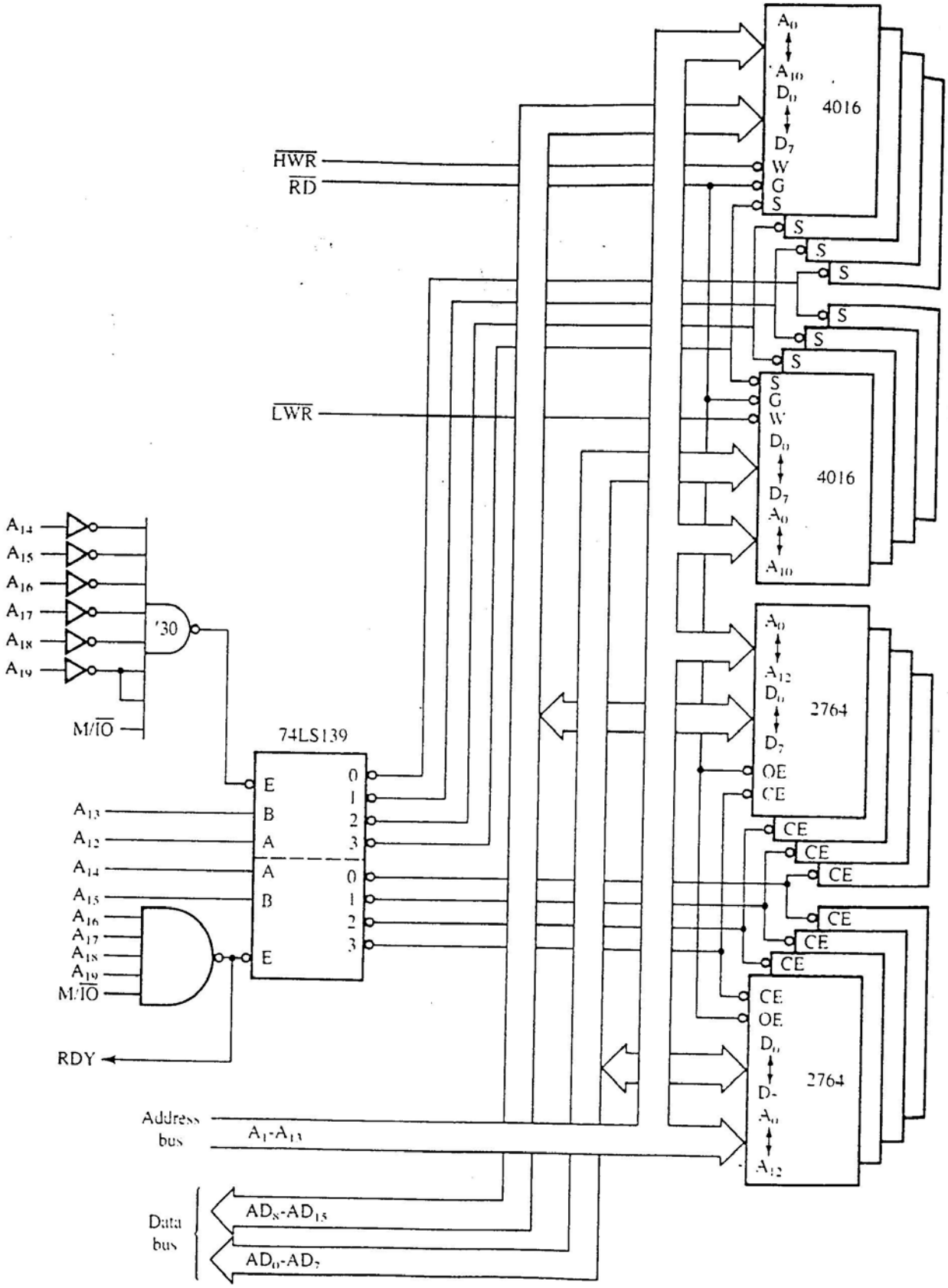
HWR
RD
LWR
4016
4016
2764
2764
'30
74LS139
M/IO
RDY
Address bus
A1-A13
Data bus
AD8-AD15
AD0-AD7

Figure 3.

512K × 8 Pentium SRAM interface.

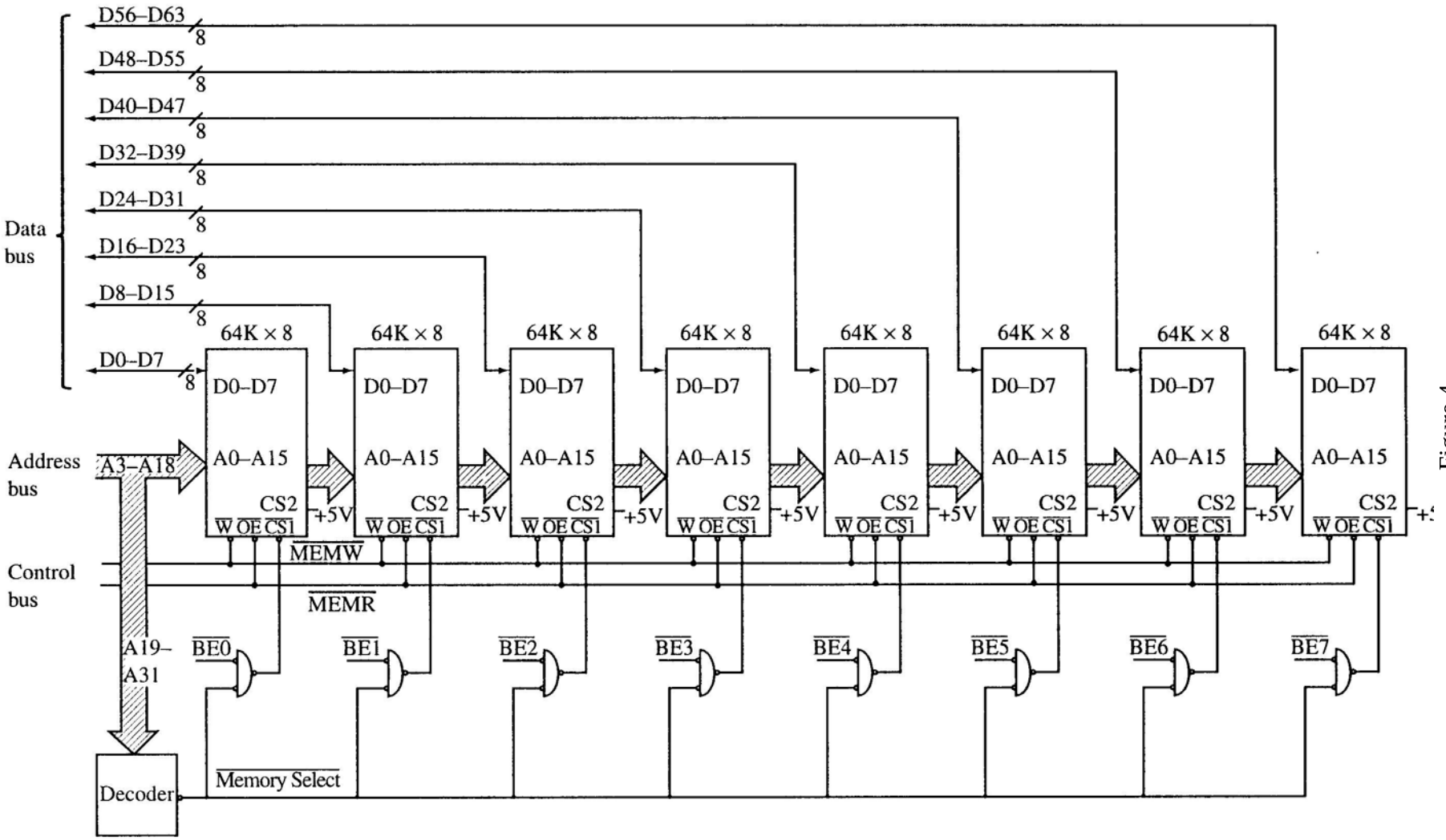

Figure 4.