Part II: 8086/8088 Hardware Specifications and Interfacing

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Introduction

- This course covers:
  - Assembly language Programming (Intel x86)
  - General system design concepts, devices and support chips
  - Specifically covers architecture of the Intel microprocessors
  - Hardware configuration and control of: Common microprocessor support chips, e.g. Interrupt controller, Popular I/O devices, e.g. UART, parallel IO, timers

- This part covers:
  - Intel 8086, 8088 processor hardware specifications
  - Memory Interfacing, basic I/O interfacing, Interrupts

- Textbook:
  - Barry B. Brey, 'The Intel Microprocessors', Fifth Edition

Systems Overview

- General Purpose Computing Systems
  - Personal Computers, laptops, workstations, mainframes and servers

- Embedded Systems
  - It is a system whose principal function is not computational, but which is con-trolled by a computer embedded within it
  - Consumer electronics such as Cell phones, pagers, digital cameras, camcorders, PDAs, DVD players, calculators
  - Automobiles Transmission control, cruise control, fuel injection, antilock brakes, active suspension

- Cyber-Physical Systems
  - Integrations of computation, networking, and physical processes

Computational Elements

- Microprocessors
  - The CPU is a unit that fetches and processes a set of general-purpose instructions
  - The CPU instruction set includes instructions for data transfer, ALU operations, stack operations, input and output (IO) operations and program control, sequencing and supervising operations
  - A microprocessor is a single VLSI chip that has a CPU and may also have other units (e.g. caches, floating point processing arithmetic unit, pipelining and super-scaling units) that are additionally present and result in faster processing of instructions.
  - Examples: Intel 8085, Intel x86 processors, Motorola 68HCxxx, Sun Sparc, IBM PowerPC etc.

Computational Elements

- Microcontrollers
  - A microcontroller is a single chip unit which, though having limited computational capabilities, possesses enhanced input-output capabilities and a number of on-chip functional units
  - Particularly suited for use in embedded systems for real-time control applications with on-chip program memory and devices
  - Common peripherals include serial communication devices, timers, counters, pulse-width modulators, analog-to-digital and digital-to-analog convertors
  - Examples: Motorola 68HC11xx, HC12xx, HC16xx, Intel 8051, 80251, PIC 16F84, PIC18, ARM9, ARM7, Atmel AVR etc.

Computational Elements

- Digital Signal Processor
  - Essential for systems that require large number of operations on digital signals, which are the digital encoding of analog signals like video and audio
  - They carry out common signal processing tasks like signal filtering, transformations or combinations
  - Used widely in image processing applications, multimedia, audio, video, HDTV,
  - DSP modem and telecommunication processing systems.
  - They perform math-intensive operations, including operations like multiplication and division.
  - Examples: TI TMS320Cxx, Analog Devices SHARC, Motorola 5600xx, etc.

Computational Elements

- Programmable Logic Devices (PLD)/ Field Programmable Gate Arrays (FPGA)
  - Contains general purpose logic elements that can be programmed to implement desired functionality, very flexible for implementing custom logic circuits
  - PLD usually are smaller and contain programmable gates like AND/OR arrays
  - FPGAs provide lot more functionality and can be used to implement complex designs
  - FPGAs can have on-chip microprocessors, memory, DSP, communication devices
  - Examples: Xilinx Virtex, Spartan series FPGAs, Actel, Altera, Lattice, QuickLogic

Computational Elements

- Application Specific Integrated Circuits (ASICs)/ System-on-a-chip (SOCs)
  - Custom designed VLSI chips that perform the required function
  - Functionality can be integrated using IP (Intellectual property) cores
  - General purpose processors are also available as IP cores and can be integrated on the chip
  - Embedded processors are available from ARM, Intel, Texas Instruments and various other vendors
  - Only feasible for high volume, relatively high cost systems as initial costs and time-to -market can be significant

Intel x86 Family Evolution

- In this course we focus on the Intel x86 architecture, associated peripherals and assembly language programming. However, concepts covered apply to other logic families.

- 4004:
  - 4-bit microprocessor
  - 4KB main memory
  - 45 instructions
  - PMOS technology
  - 50 KIPS

- 8008: (1971)
  - 8-bit version of 4004
  - 16KB main memory
  - 48 instructions
  - NMOS technology

- 8080: (1973)
  - 8-bit microprocessor.
  - 64KBmain memory.
  - 2 microseconds clock cycle time; 500,000 instructions/sec.
  - 10X faster than 8008.

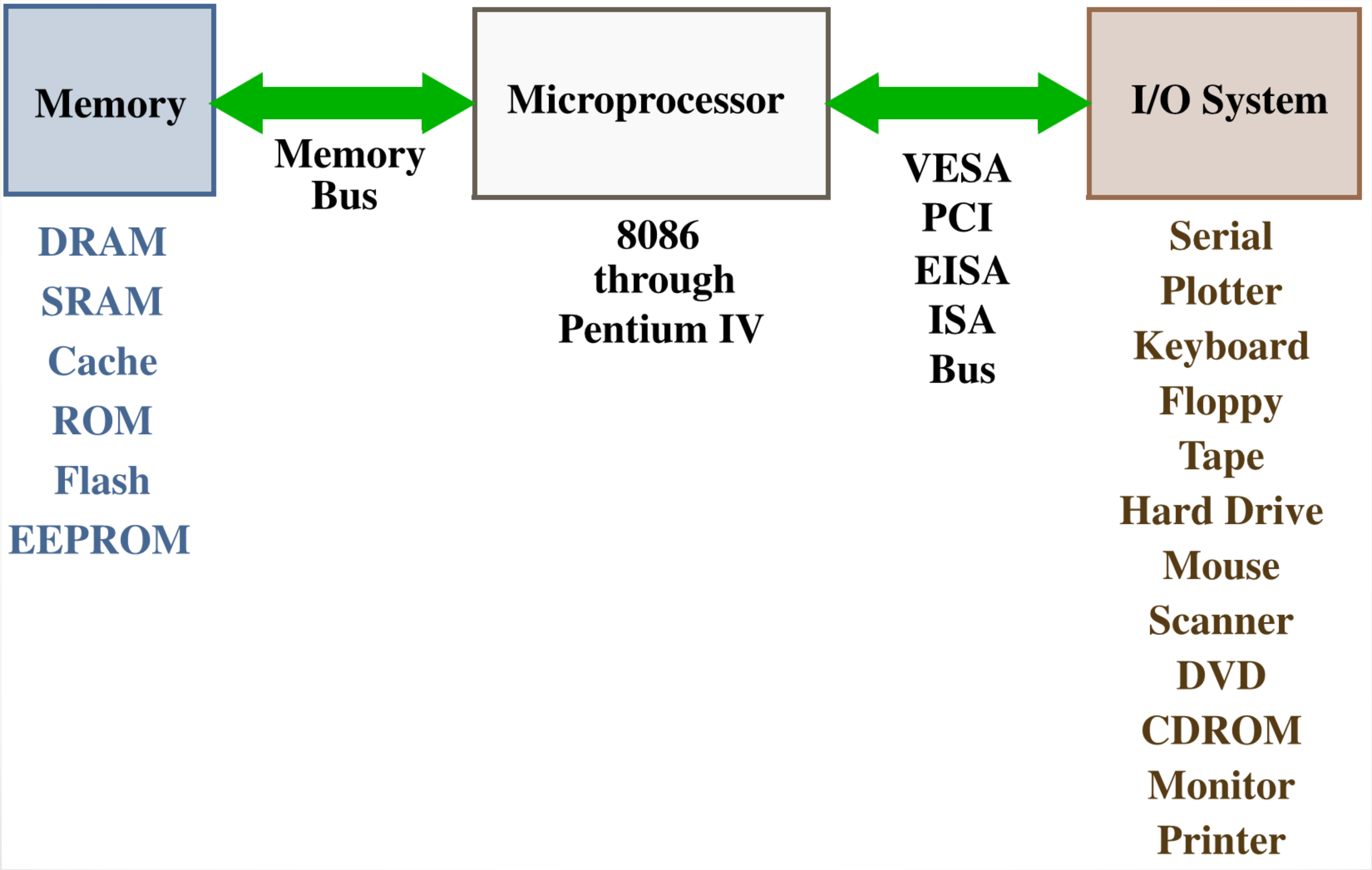
Intel x86 Family Evolution

- 8085: (1977)
  - 8-bit microprocessor - upgraded version of the 8080.
  - 64KB main memory.
  - 1.3 microseconds clock cycle time; 769,230 instructions/sec.
  - 246 instructions.
  - Intel sold 100 million copies of this 8-bit microprocessor.
- 8086: (1978) 8088 (1979)
  - 16-bitmicroprocessor.
  - 1MB main memory.
  - 2.5 MIPS (400 ns).
  - 4- or 6-byte instruction cache.
  - Other improvements included more registers and additional instructions.
- 80286: (1983)
  - 16-bit microprocessor very similar in instruction set to the 8086.
  - 16MB main memory.
  - 4.0 MIPS (250 ns/8MHz).

Intel x86 Family Evolution

- Report the Intel x86 processor family enhancements showing the following:
  - Fabrication technology, transistor count, and chip area.
  - Operating frequency, bus width, and throughput in MIPS.
  - Notable enhancements and breakthroughs
  - Applications and limitations of each generation

Processor Basic Components



Memory

Memory Bus

Microprocessor

I/O System

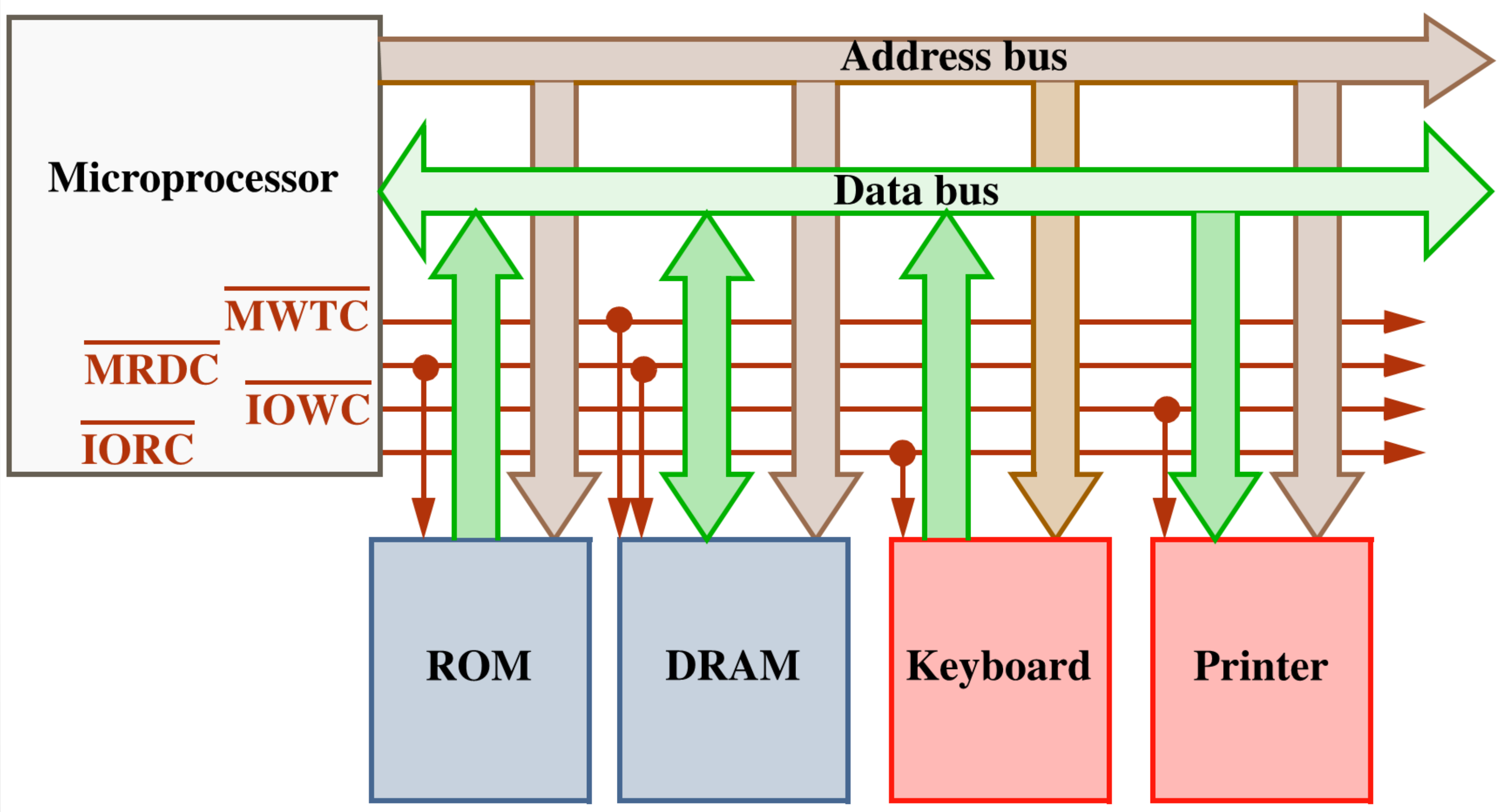
DRAM
SRAM
Cache
ROM
Flash
EEPROM

8086 through Pentium IV

VESA
PCI
EISA
ISA
Bus

Serial
Plotter
Keyboard
Floppy
Tape
Hard Drive
Mouse
Scanner
DVD
CDROM
Monitor
Printer

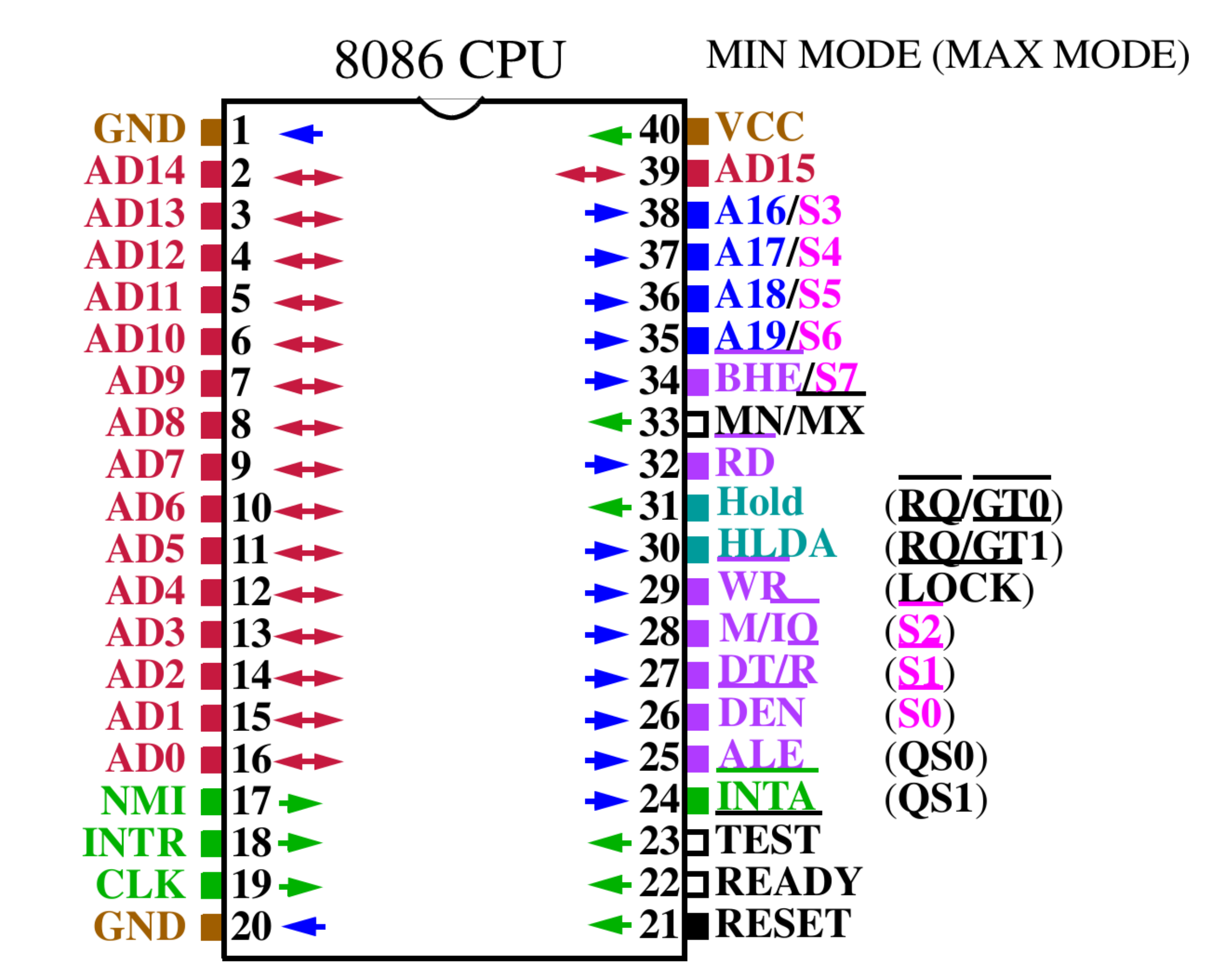
Processor Basic Architecture (Von Neumann Bus Architecture)



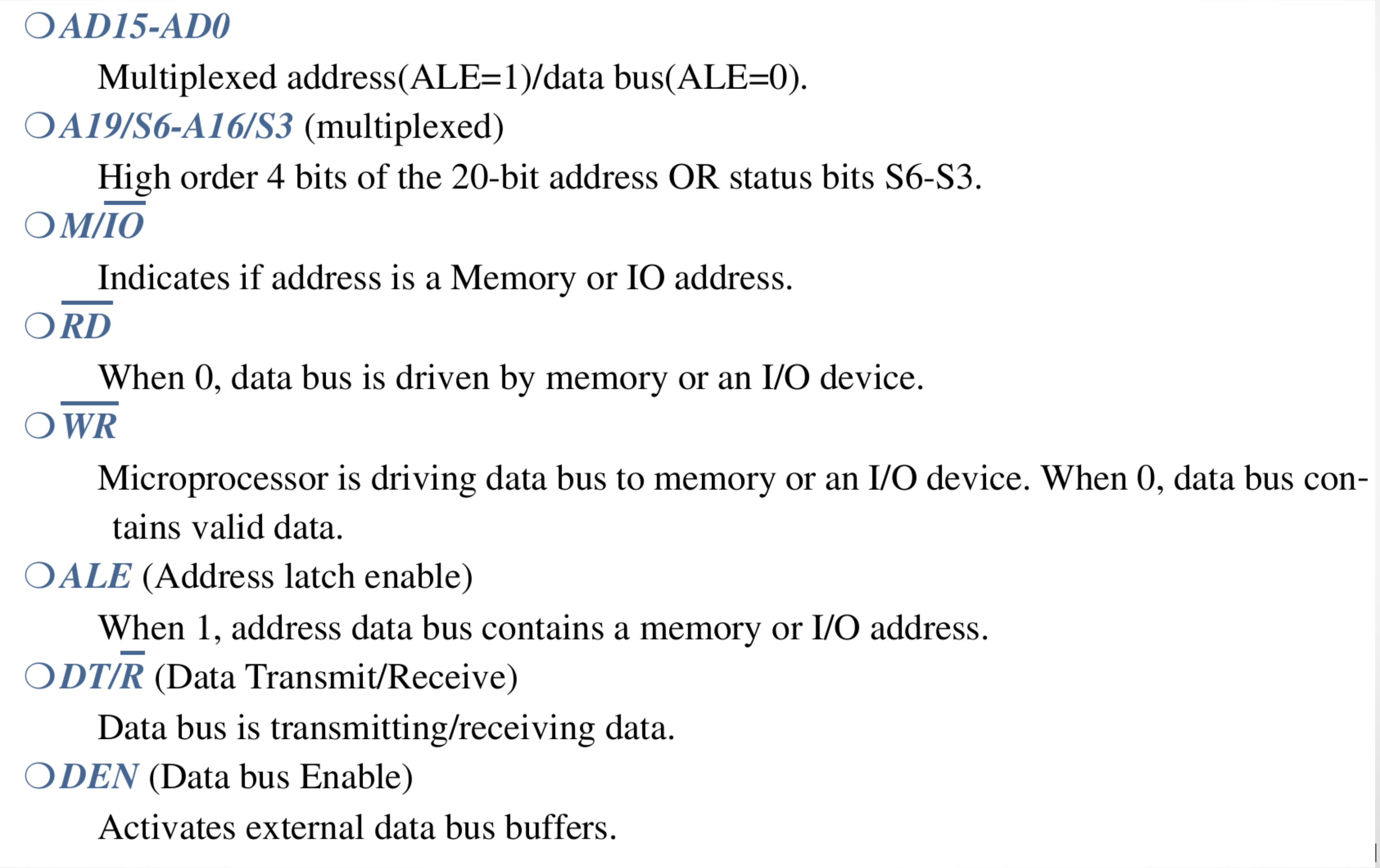
8086/88 Device Specifications

- Both are packaged in DIP (Dual In-Line Packages)
  1. The 8086 has 16-bit data bus (AD_0-AD_{15}), but the 8088 has 8-bit data bus (AD_0-AD_7).
  2. The 8086 has $\mathrm{M}/\overline{IO}$, but the 8088 has $\mathrm{IO}/\overline{M}$
- 8086 draws a maximum supply current of 360 mA, 8088 draws a maximum supply current of 340 mA.
- Both microprocessors operates in ambient temperature between 0°C and 70°C.
- Extended temperature-range versions are available

8086 Pinout


8086 CPU
MIN MODE (MAX MODE)
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 Hold (RQ/GT0)
30 HLDA (RQ/GT1)
29 WR (LOCK)
28 M/IO (S2)
27 DT/R (S1)
26 DEN (S0)
25 ALE (QS0)
24 INTA (QS1)
23 TEST
22 READY
21 RESET

8086 Pin Functions



- ***AD15-AD0***

  Multiplexed address(ALE=1)/data bus(ALE=0).

- ***A19/S6-A16/S3*** (multiplexed)

  High order 4 bits of the 20-bit address OR status bits S6-S3.

- $M/\overline{IO}$

  Indicates if address is a Memory or IO address.

- $\overline{RD}$

  When 0, data bus is driven by memory or an I/O device.

- $\overline{WR}$

  Microprocessor is driving data bus to memory or an I/O device. When 0, data bus contains valid data.

- ***ALE*** (Address latch enable)

  When 1, address data bus contains a memory or I/O address.

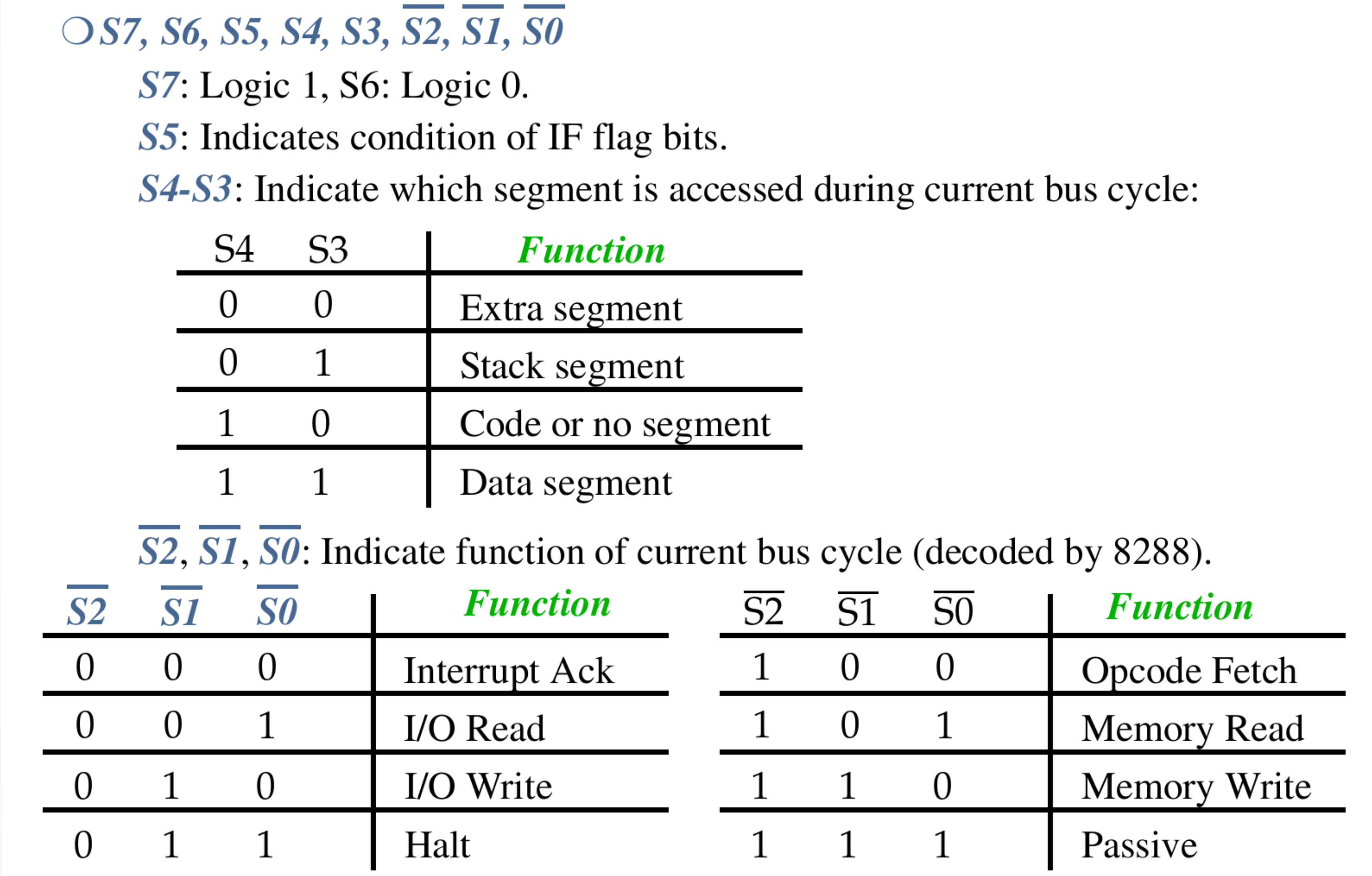
- $DT/\overline{R}$ (Data Transmit/Receive)

  Data bus is transmitting/receiving data.

- ***DEN*** (Data bus Enable)

  Activates external data bus buffers.

8086 Pin Functions



- ***S7, S6, S5, S4, S3, $\overline{S2}$, $\overline{S1}$, $\overline{S0}$***

  S7: Logic 1, S6: Logic 0.

  S5: Indicates condition of IF flag bits.

  S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	***Function***
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{S2}$, *$\overline{S1}$*, *$\overline{S0}$*: Indicate function of current bus cycle (decoded by 8288).

$\overline{S2}$	*$\overline{S1}$*	*$\overline{S0}$*	***Function***
0	0	0	Interrupt Ack
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	***Function***
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

8086 Pin Functions

- ***INTR***

  When 1 and IF=1, microprocessor prepares to service interrupt. $\overline{\text{INTA}}$ becomes active after current instruction completes.

- ***$\overline{\textit{INTA}}$***

  Interrupt Acknowledge generated by the microprocessor in response to INTR. Causes the interrupt vector to be put onto the data bus.

- ***NMI***

  Non-maskable interrupt. Similar to INTR except IF flag bit is not consulted and interrupt is vector 2.

- ***CLK***

  Clock input must have a duty cycle of 33% (high for 1/3 and low for 2/3s)

- ***VCC/GND***

  Power supply (5V) and GND (0V)

- ***MN/$\overline{\textit{MX}}$***

  Select minimum (5V) or maximum mode (0V) of operation.

8086 Pin Functions

- $\overline{BHE}$

  Bus High Enable. Enables the most significant data bus bits (D_{15}-D_8) during a read or write operation.

- ***READY***

  Used to insert wait states (controlled by memory and IO for reads/writes) into the microprocessor.

- ***RESET***

  Microprocessor resets if this pin is held high for 4 clock periods.

  Instruction execution begins at FFFF0H and IF flag is cleared.

- $\overline{TEST}$

  An input that is tested by the WAIT instruction.

  Commonly connected to the 8087 coprocessor.

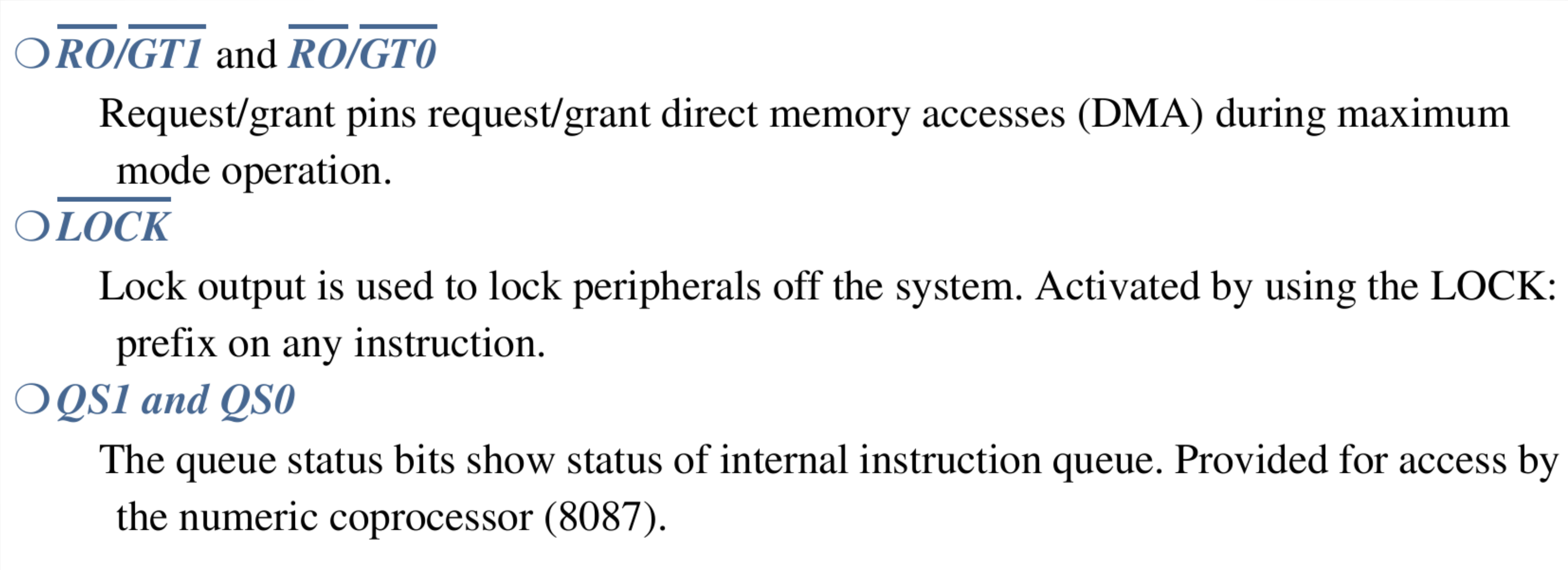
- ***HOLD***

  Requests a direct memory access (DMA). When 1, microprocessor stops and places address, data and control bus in high-impedance state.

- ***HLDA*** (Hold Acknowledge)

  Indicates that the microprocessor has entered the hold state.

8086 Pin Functions



- ***$\overline{RO}/\overline{GT1}$*** and ***$\overline{RO}/\overline{GT0}$***

  Request/grant pins request/grant direct memory accesses (DMA) during maximum mode operation.

- ***$\overline{LOCK}$***

  Lock output is used to lock peripherals off the system. Activated by using the LOCK: prefix on any instruction.

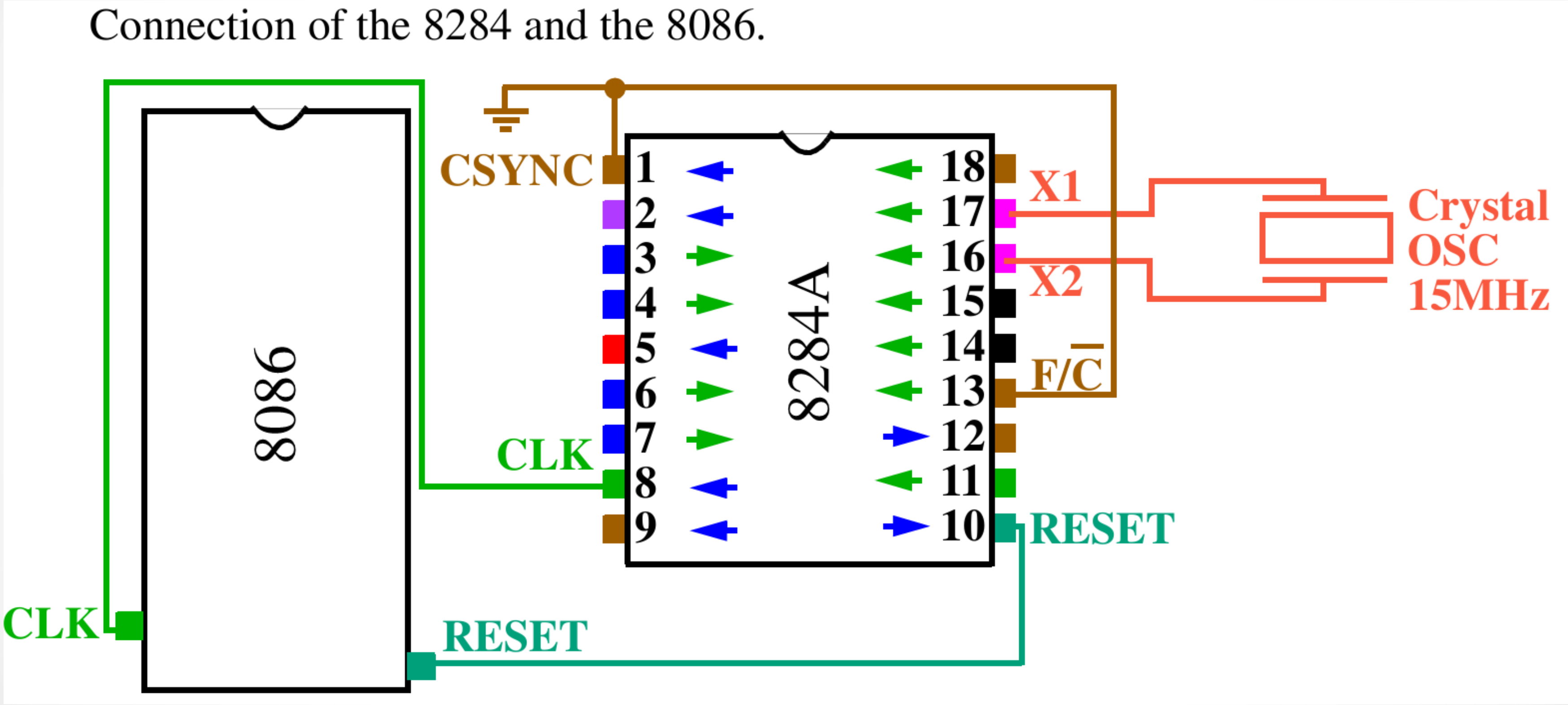
- ***QS1 and QS0***

  The queue status bits show status of internal instruction queue. Provided for access by the numeric coprocessor (8087).

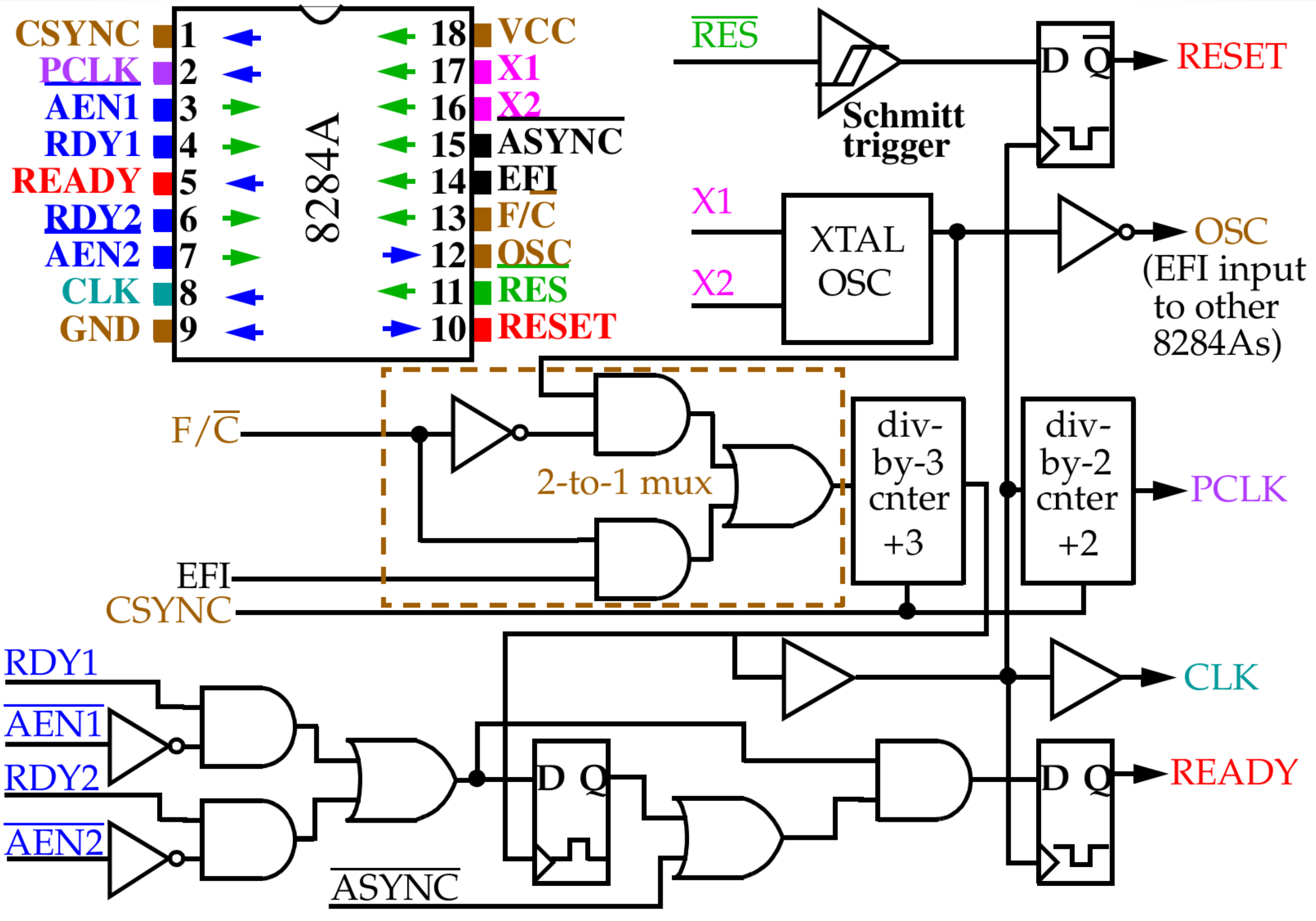
Clock Generation

- The 8284A is an ancillary component to the 8086/8088
- Clock generation
  - RESET synchronization
  - READY synchronization
  - Peripheral clock signal

Clock Generation


Connection of the 8284 and the 8086.

8284A Clock Generator



8284A Clock Generator

Crystal is connected to X1 and X2.

XTAL OSC generates square wave signal at crystal's frequency which feeds:

- An inverting buffer (output OSC) which is used to drive the EFI input of other 8284As.
- 2-to-1 MUX: F/$\bar{C}$ selects XTAL or EFI external input.

The MUX drives a divide-by-3 counter (15MHz to 5MHz).

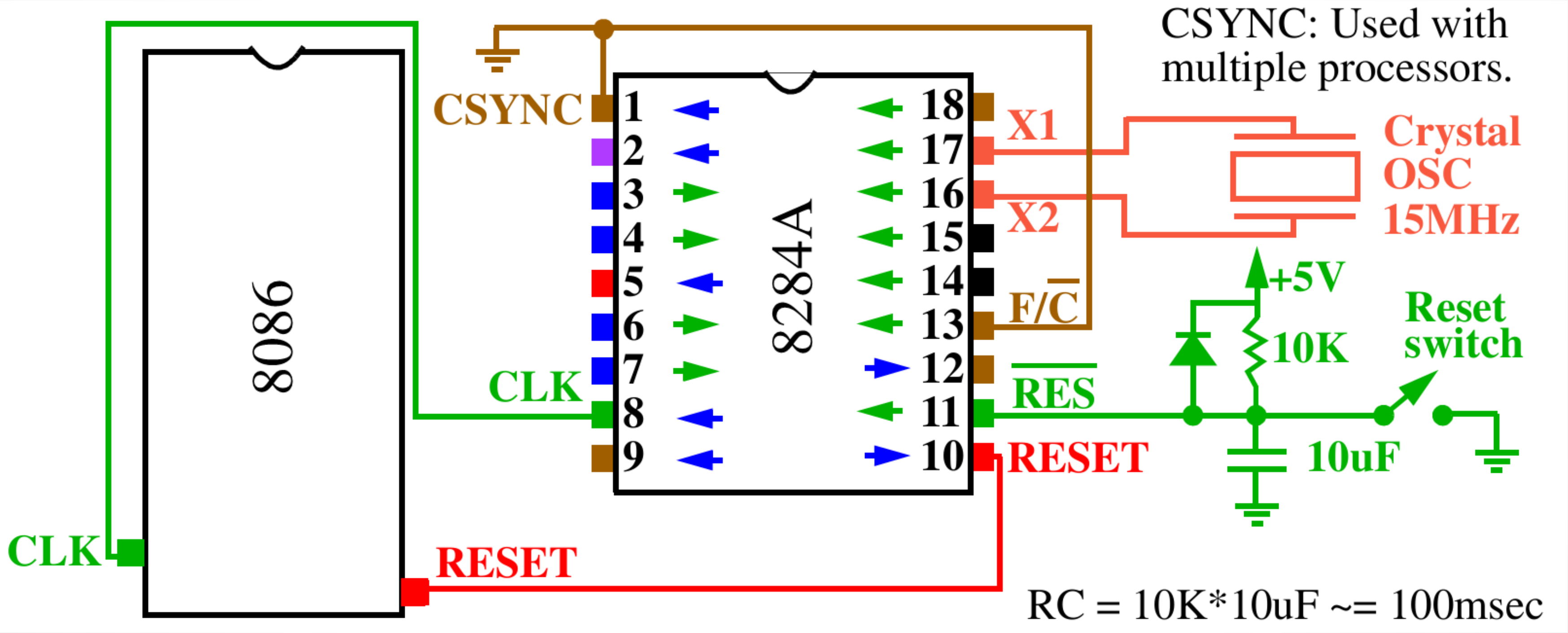
This drives:

- The READY flip-flop (READY synchronization).
- A second divide-by-2 counter (2.5MHz clk for peripheral components).
- The RESET flip-flop.
- CLK which drives the 8086 CLK input.

8284A Clock Generator

- RESET: Negative edge-triggered flip-flop applies the RESET signal to the 8086 on the falling edge
- The 8086 samples the RESET pin on the rising edge
- Correct reset timing requires that the RESET input to the microprocessor becomes a logic 1 NO LATER than 4 clocks after power up and stay high for at least 50μs

8284A Clock Generator



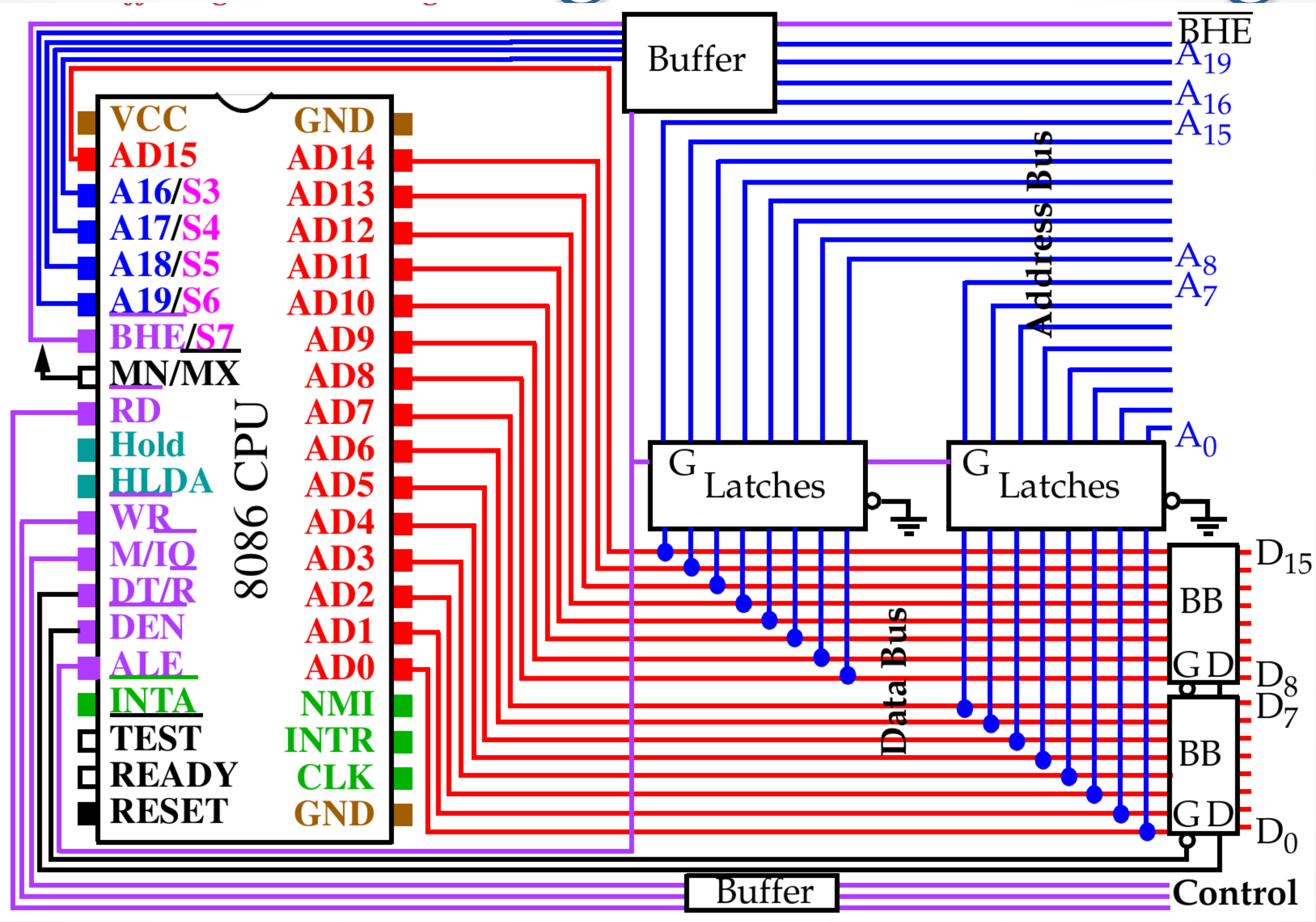
Bus Buffering and Latching

- For very large systems, the buses are buffered. WHY?
- The address/data bus are multiplexed to save the number of pins required for the 8086/8088 IC.
- They must be demultiplexed. WHY?
- All computer systems have three buses:
  - Address bus
  - Data bus
  - Control bus
- These buses must be present to interface memory and I/O.

Bus Buffering and Latching

- Computer systems have three buses: Address, Data, and Control
- The Address and Data bus are multiplexed (shared)due to pin limitations on the 8086.
- The ALE pin is used to control a set of latches.
- All signals MUST be buffered
  - Buffered Latches for A0-A15
  - Control and A16-A19+ $\overline{BHE}$ are buffered separately.
  - Data bus buffers must be bidirectional buffers.
- In an 8086 system, the memory is designed with two banks
  - High bank contains the higher order 8-bits and low bank the lower order 8-bits
  - Data can be transferred as 8 bits from either bank or 16-bits from both
  - $\overline{BHE}$ pin selects the high-order memory bank

Bus Buffering and Latching



Timing In General

- The 8086/8088 uses the memory and I/O in periods of time called bus cycle.
- Each bus cycle equal to 4 system-clocking periods (T states).
- If the clock is operated at 5 MHz, one bus cycle is completed in 800ns.
- The 8086/8088 reads or writes data at the rate of 1.25 million times a second.

Timing In General

- During the first clocking period (T_1):
  - The address is placed on the Address/Data bus.
  - Control signals (M/ $\overline{IO}$, ALE and DT/ $\bar{R}$) specify memory or I/O, latch the address onto the address bus and set the direction of data transfer on data bus

- During the second clocking period (T_2):
  - The 8086/8088 issues the $\overline{RD}$or $\overline{WR}$ signal for read or write the data
  - The 8086/8088 issues $\overline{DEN}$ enables the memory or I/O device to receive the data for writes and the 8086/8088 to receive the data for reads

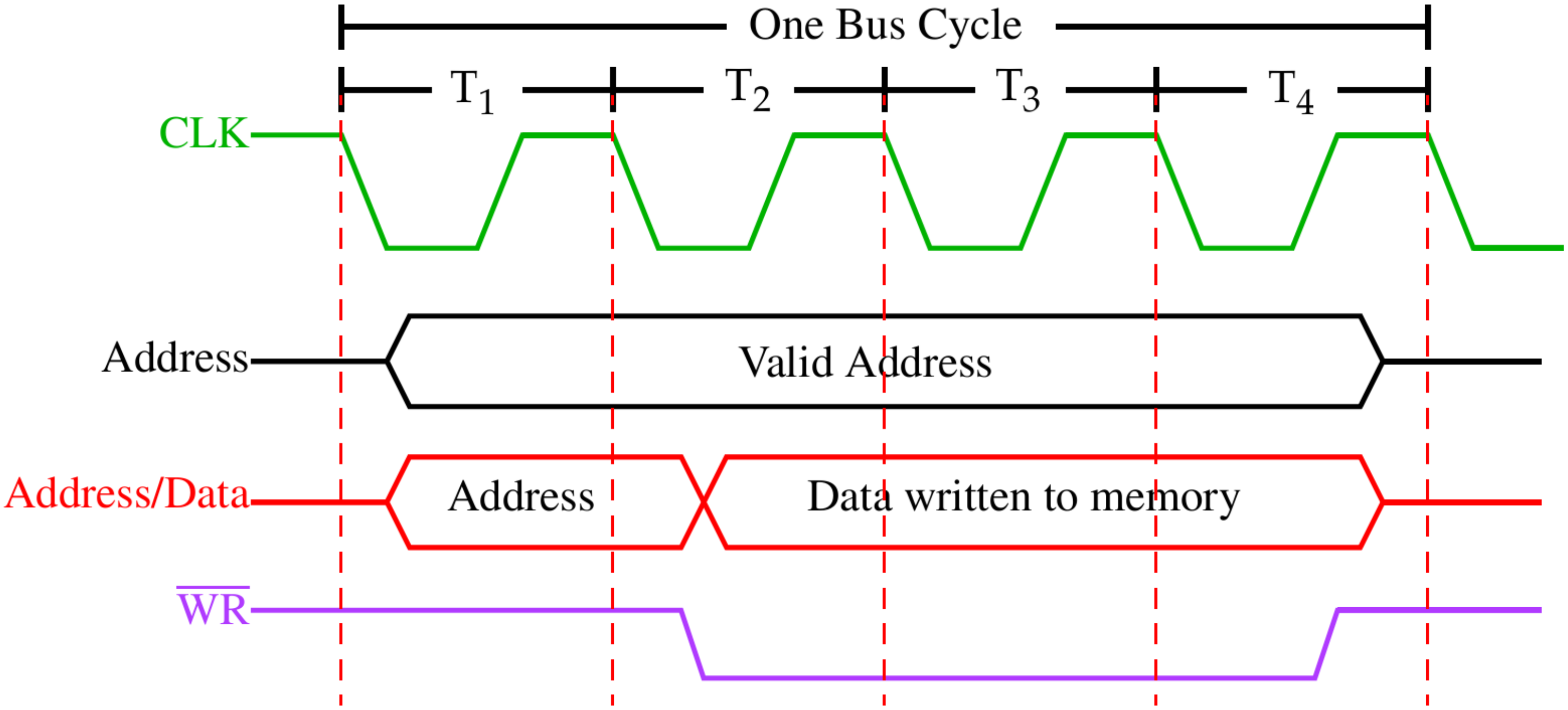
Timing In General

- During the third clocking period (T_3):
  - This cycle is provided to allow memory to access data.
  - READY is sampled at the end of T_2
    - If low, T_3 becomes a wait state
    - Otherwise, the data bus is sampled at the end of T_3
- During the fourth clocking period (T_4):
  - All bus signals are deactivated, in preparation for next bus cycle
  - Data is sampled for reading
  - Data writes occur for writing

Bus Timing

Writing

- Dump address on address bus.
- Dump data on data bus.
- Issue a write ($\overline{WR}$) and set M/$\overline{IO}$ to 1.

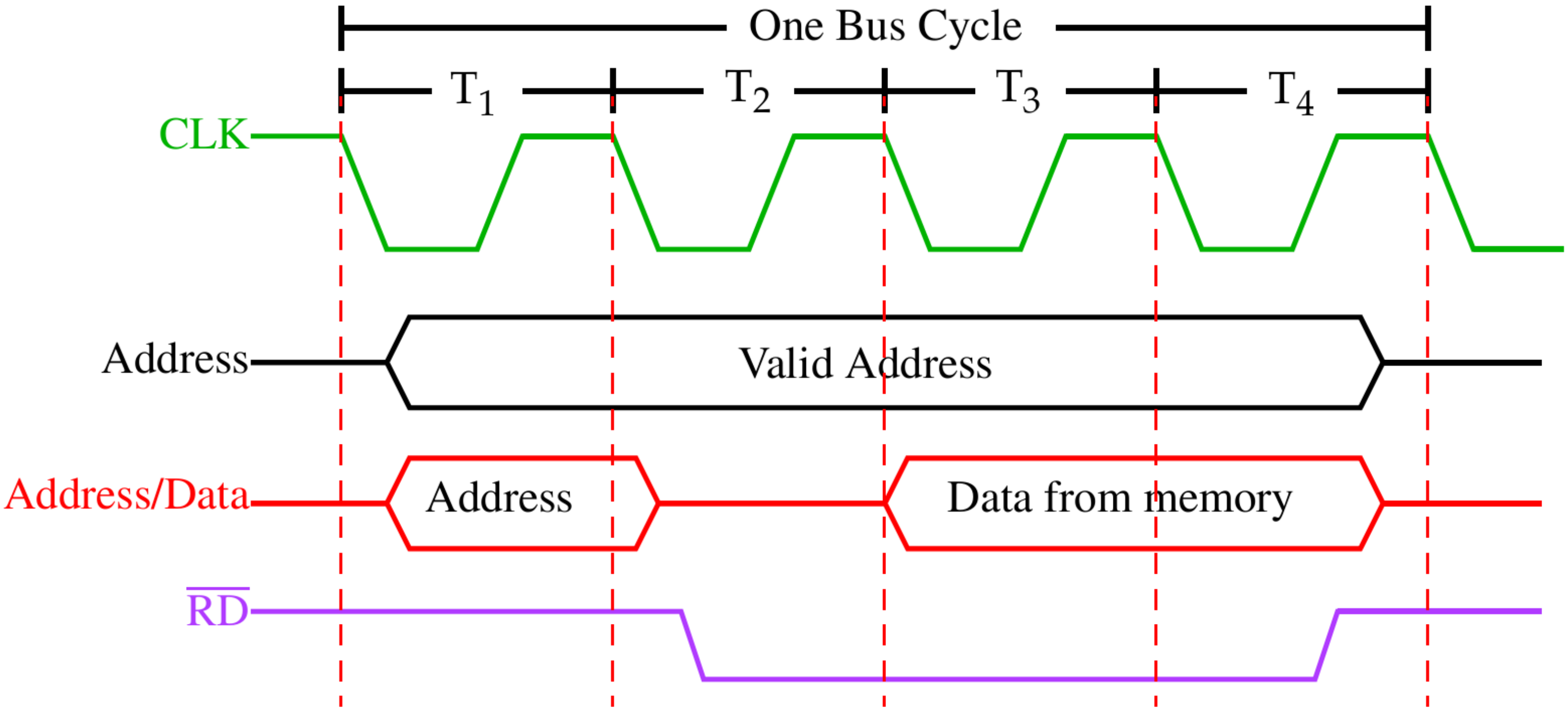


Simplified 8086 Write Bus Cycle

Bus Timing

Reading

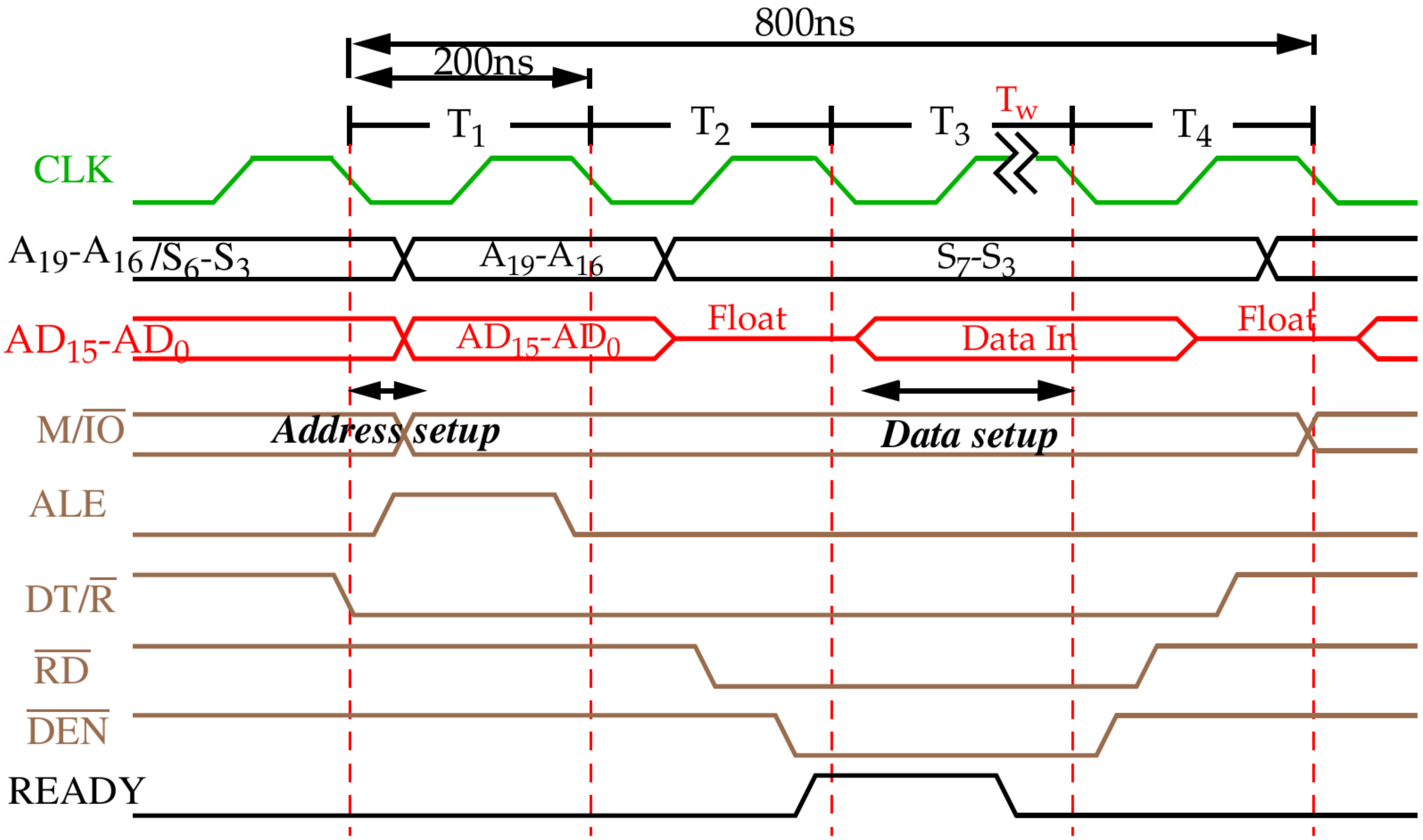
- Dump address on address bus.
- Issue a read ($\overline{RD}$) and set M/$\overline{IO}$ to 1.
- Wait for memory access cycle.



Simplified 8086 Read Bus Cycle

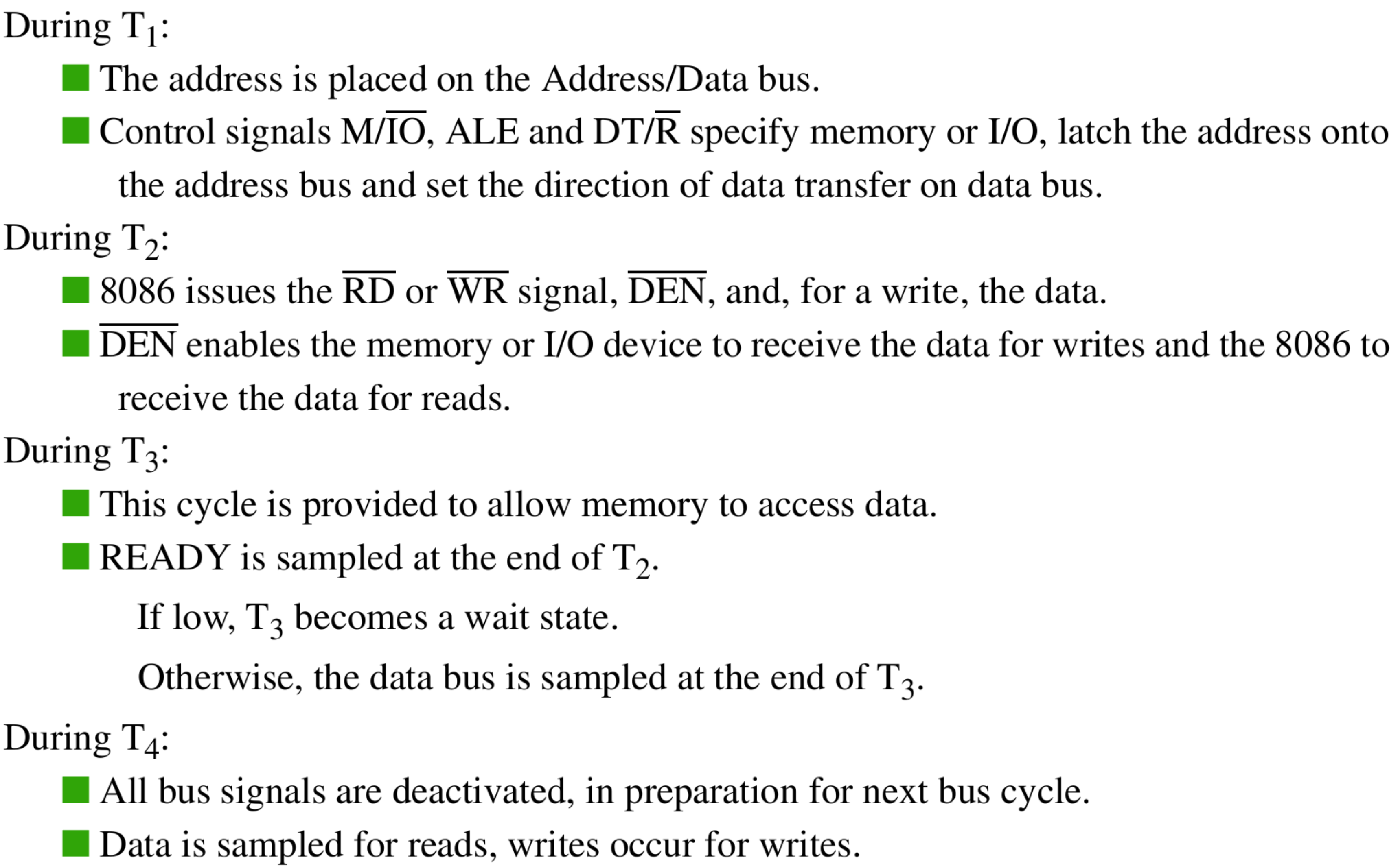
Read Bus Timing

Read Bus Timing:



Bus Timing for a Read Operation

Read Bus Timing



During T_1:

- The address is placed on the Address/Data bus.
- Control signals M/$\overline{\text{IO}}$, ALE and DT/$\overline{\text{R}}$ specify memory or I/O, latch the address onto the address bus and set the direction of data transfer on data bus.

During T_2:

- 8086 issues the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal, $\overline{\text{DEN}}$, and, for a write, the data.
- $\overline{\text{DEN}}$ enables the memory or I/O device to receive the data for writes and the 8086 to receive the data for reads.

During T_3:

- This cycle is provided to allow memory to access data.
- READY is sampled at the end of T_2.

  If low, T_3 becomes a wait state.

  Otherwise, the data bus is sampled at the end of T_3.

During T_4:

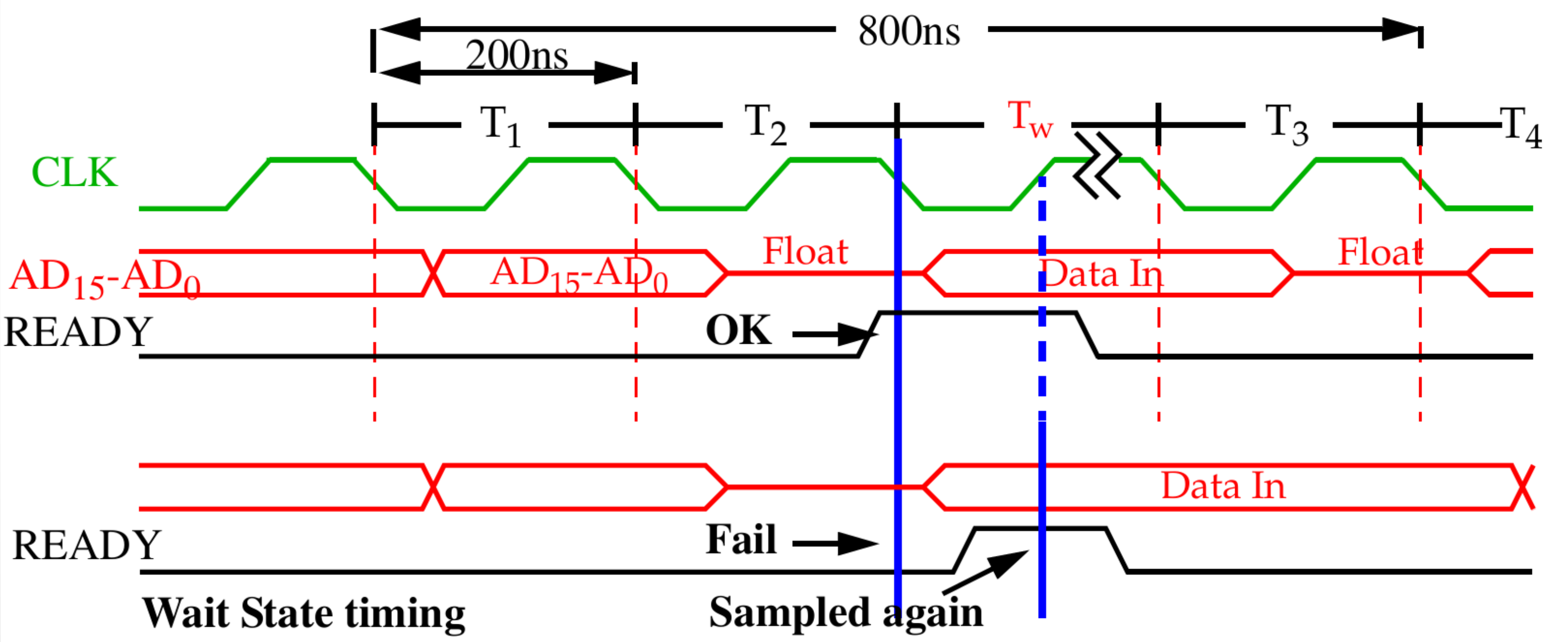
- All bus signals are deactivated, in preparation for next bus cycle.
- Data is sampled for reads, writes occur for writes.

Bus Timing

- Each BUS CYCLE on the 8086 equals four system clocking periods (T states)
- The clock rate is 5MHz, therefore one Bus Cycle is 800ns and the transfer rate is 1.25MHz
- Memory specifications (memory access time) must match constraints of system timing
- For example, bus timing for a read operation shows almost 600ns are needed to read data
- However, memory must access faster due to setup times, e.g. Address setup and data setup

Bus Timing

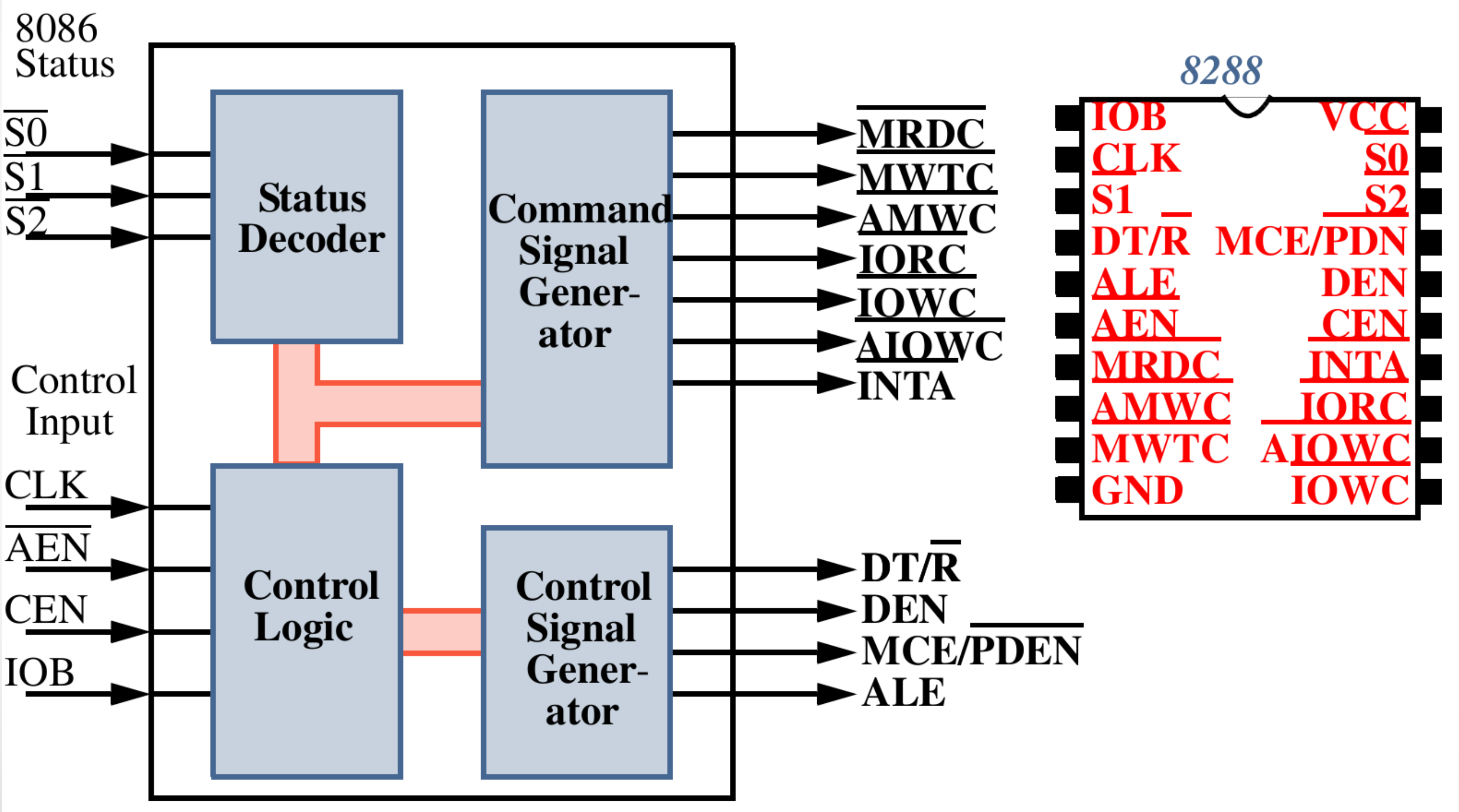
- READY: An input to the 8086 that causes wait states for slower memory and I/O components
- A wait state (T_W) is an extra clock period inserted between T_2 and T_3 to lengthen the bus cycle



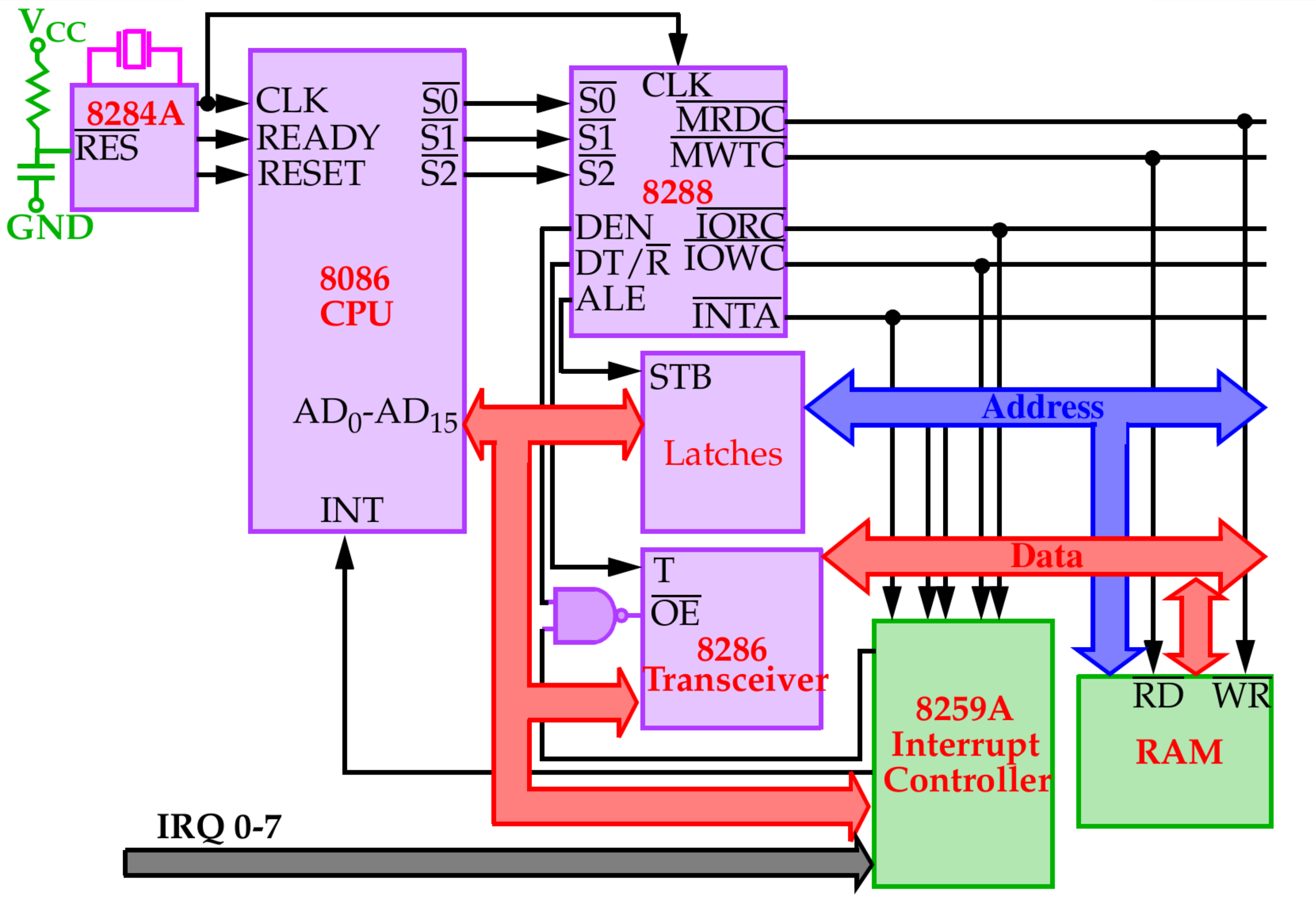
Minimum Mode versus Maximum Mode

- Minimum mode:
  - It is the least expensive way to operate the 8086/8088.
  - It costs less because all the control signals are generated inside the microprocessor.
  - It allows the 8085A peripherals to be used.
- Maximum mode:
  - It is dropped from the Intel family beginning from 80286.
  - All the control signals must be externally generated.
  - An external bus controller is used.
  - It is used only when the system contains external coprocessor.

8288 Bus Controller



MAX Mode 8086 System



V_{CC}
8284A
RES
GND
CLK
READY
RESET
$\overline{S0}$
$\overline{S1}$
$\overline{S2}$
8086
CPU
AD_0-AD_{15}
INT
$\overline{S0}$
$\overline{S1}$
$\overline{S2}$
CLK
$\overline{MRDC}$
$\overline{MWTC}$
8288
DEN
$DT/\overline{R}$
ALE
$\overline{IORC}$
$\overline{IOWC}$
$\overline{INTA}$
STB
Latches
Address
T
$\overline{OE}$
8286
Transceiver
Data
8259A
Interrupt
Controller
$\overline{RD}$
$\overline{WR}$
RAM
IRQ 0-7