Alexandria University
Faculty of Engineering
Electrical Engineering Department
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جامعة الإسكندرية
كلية الهندسة
قسم الهندسة الكهربية
يناير 2013

Course title : Microprocessors-1 — **اسم المقرر والرقم الكودى له: المعالجات الدقيقة-1**
Year : 3rd Communications — **السنة الدراسية : الثالثة- اتصالات**
Time allowed: 3 hours — **مدة الإمتحان : 3 ساعات**

The examiners: Dr. Nayera Sadek, Dr. Mohammed Morsy and the committee

Part I: Software

Answer All the following questions:

QUESTION ONE: **[15 points]**

Choose the best answer(s). In your answer book, write the question number and your answer(s) only. If none of the given answer fits, write NONE and your answer in your answer book.

1) The large number of the registers in the 8086 microprocessor…….
   a) Increases the data access time. b) Increases the number of instruction executed per second.
   c)Increases the data storage space. d)Accelerates data movements to/from the ALU.
2) During execution, the ratio of the activated memory locations to the total memory size is….
   a) 1:1 b) 1:2 c) 1:4 d) 1:8
3) The ALU of the 8088 microprocessor can perform its operation on the data whose size is ….
   a) 4 bits b) 8 bits c) 16 bits d) 32 bits
4) The ratio of the size of the physical memory of the 8086 to that of the 8088 is …….
   a) 1:1 b) 2:1 c) 1:2 d) 1:4
5) To transfer a word to the memory, the ratio of speed transfer of the 8086 to that of 8088 is…
   a) 1:1 b) 2:1 c) 1:2 d) 1:4
6) The size of the interrupt-vectors table is:
   a) 256 Bytes b) 512 Bytes c) 1024 Bytes d) 64 KB
7) All the interrupt instructions are stored in …. bytes except…..
   a) 1, INT 2 b) 1, INT 3 c) 2, INTO d) 2, INT 3

Using the memory part shown below, answer questions 8 to 15.

8) A character is stored in its ASCII format starting from the physical address 12344H, its ASCII code is…….
   a)38H b) 3938H c) 3837H d) 41403938H
9) Using the IEEE-754 short-form, the real number is stored starting at the physical address 12348H, this real number is …….. (in decimal)
   a) -232.7625 b) -465.625 c)-931.25 d)+232.7625
10) A word-instruction is stored starting from the memory location whose physical address is 1234CH, this instruction is…..
   a) MOV AX, BX b) MOV [BP+DI+2001], AX
   c)MOV ES, BX d) MOV BX, DS
11) If BP = 2344H is used to point to the memory location whose physical address is 12344H, the DS register has……
   a) 1000H b) 1010H c) 2000H d) 2010H
12) If SP is initialized at 0000H and SP = 0350H points to the memory location whose address is 12350H, the stack is storing …..words
   a) 424 b) 848 c) 32344 d) 64688
13) According to question 11), the range of the stack segment is…
   a)03500H-134FFH b)10000H-1FFFFH c) 12000H- 21FFFH d)12350H-2234FH
14) According to question 11), after executing POP AX, AX equals…
   a) 11FFH b) FF11H c) 2011H d) 1120H
15) After executing question 13), the SP equals……
   a) 0348H b) 0349H c) 0351H d) 0352H

Memory Locations

Physical address	Contents
12340H	12H
12341H	34H
12342H	FAH
12343H	37H
12344H	38H
12345H	39H
12346H	40H
12347H	41H
12348H	00H
12349H	D0H
1234AH	E8H
1234BH	C3H
1234CH	8EH
1234DH	C3H
1234EH	01H
1234FH	20H
12350H	11H
12351H	FFH
12352H	94H

QUESTION TWO: **[15 points]**

Choose the best answer(s). In your answer book, write the question number and your answer(s) only. If none of the given answer fits, write NONE and your answer in your answer book.

Using Program 1, answer questions 1 to 8.

1) The machine code of MOV CX, 10 is ……H
   a) C7C110 b) B910 c) B90A d)B90A00
2) When CX =10, the program…..
   a) Jumps to COMP b) Shifts AX by 1
3) The addressing mode of IN AX, DX is….
   a) Direct b) Indirect c) Immediate d) Register
4) The addressing mode of JZ COMP is…….
   a) Direct b) Indirect c) Relative
5) The JMP DONE instruction will be executed…… times
   a) Zero b) 5 c) 10 d) 16
6) The TEST CX, 1 can be replaced by……
   a)AND CX, 1 b)OR CX,1 c)CMP CX,0 d)XOR CX,1
7) The SHL AX, 1 is equivalent to….
   a)Signed multiplying by 2. b)Unsigned multiplying by 2
   c)Signed dividing by 2 d)Unsigned dividing by 2
8) The machine code of LOOP NEXT is……H
   a) E210 b)E2F0 c)E2F2 d)E2F4

Program 1

Address	Code
CS:X	MOV CX, 10
CS:0107H	NEXT: TEST CX, 1
CS:010BH	JZ COMP
CS:010DH	SHL AX, 1
CS:010FH	OUT 15H, AX
CS:0111H	JMP DONE
CS:0113H	COMP: IN AX, DX
CS:0115H	DONE: LOOP NEXT
CS:0117H	HLT

Using Program 2, answer questions 9 to 15.
Assume that AX = 2310H, BX = F976H, CX = 01FBH, DX = 539AH, Flag register = 0417H

9) After executing the instruction in line 1, AX becomes….
   a) 0070H b) 0A90H c) 0FB0H d) FF90H
10) After executing LAHF, AX becomes…..
   a) 0417H b) 0470H c) 1710H d) 1790H
11) After executing CBW, AX becomes …….
   a) 0004H b) 0017H c) FF17H d) FF90H
12) After executing the instruction in line 6, AX becomes…..
   a) 01DBH b) 0203H c) 02B3H d) 02FBH
13) After executing line 8, CX and the Flag register become….
   a) 0175H, 0404H b) 0176H, 0400H
   c)0176H, 0401H d) 0276H, 0401H
14) If SP = FFF0, after executing IRET, SP becomes…….
   a) FFECH b) FFF2H c) FFF4H d) FFF6H
15) If the given program is the ISR of INT 60, the address of SERVICE should be stored in the interrupt vector table at the physical address……..
   a) 000ECH b) 000F0H c) 000F4H d) 00180H

Program 2

```
1.  SERVICE:
        IMUL CL
2.      MOV BX, AX
3.      LAHF
4.      XCHG AH, AL
5.      CBW
6.      IDIV CL
7.      MOV DX, AX
8.      SUB CX, 85H
9.      IRET
```

QUESTION THREE: **[15 points]**

Choose the best answer(s). In your answer book, write the question number and your answer(s) only. If none of the given answer fits, write NONE and your answer in your answer book.

Given: CS=1000H, DS=2000H, SS=2002H, ES=3000H, AX=0008H, BX=0030H, CX=0000H, BP=0004H, SP=0010H and the Flag=0000H. Part of memory locations are given as follows (in H)

2000:0000	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2000:0010	00	01	02	03	04	FE	89	45	09	0A	C2	7F	49	20	44	60
2000:0020	A2	B6	71	84	00	00	00	20	10	00	71	72	73	04	75	76
2000:0030	80	90	43	87	55	22	84	0A	10	12	0E	12	34	15	18	19

Using this data and program 4 to answer the following questions.

1) The physical address of the first executed instruction is ….
   a) 10100H b) 10010H c) 20030H d) 30100H

2) After executing line 2, ES and DI becomes……
   a) 0000H, 1020H b) 1020H, 0000H
   c)2000H, 0000H d) 1000H, 2000H

3) After executing XLAT, AL becomes……
   a) 0AH b) 10H c) 12H d) 0EH

4) After executing line 10, CX becomes……
   a) 0009H b) 000AH c) 000BH d) 000CH

5) After executing line 18,…….
   a) The data stored from 20000H to 2000FH changed.
   b) The data stored from 20010H to 2001FH have no change.
   c) The data stored from 20000H to 2000F becomes equal to the data stored from 20010H to 2001FH.
   d) The data stored from 20010H to 2001F becomes equal to the data stored from 20000H to 2000FH.

6) The MOV instructions at lines 19 to 21 are used to….
   a) Load DI, SI and CX by new values.
   b) Retrieve the old values of DI, SI and CX.

7) The LOOP AGAIN will be executed…..times
   a) 10 b) 12 c) 16 d) 18

8) After executing line 23, the register(s)……is/are pushed to the stack.
   a) IP b) CS, and IP c) flags, CS, and IP

9) The LOOP NEW will be executed…. times
   a) 8 b) 10 c) 12 d) 16

10) If AL = 04H, after executing the subroutine, AL becomes…
   a) 02H b) 04H c) 08 d) 10H

11) If AL = 04H, after executing the subroutine, DL becomes…
   a) 00H b) 01H c) 02H d) 04H

12) If AL = 04H, after executing the subroutine, CL becomes…
   a) 00H b) 08H c) 10H
   d)The same value before calling the subroutine.

13) After executing line 37, the SP becomes……
   a) 00FCH b) 00FEH c) 0010H d) 0012H

14) After executing line 26,…..
   e) The data stored from 20000H to 2000FH have no change.
   f) The data stored from 20010H to 2001FH have changes.
   g) The data stored from 20000H to 2000F becomes a function of the data stored from 20010H to 2001FH
   h) The data stored from 20010H to 2001F becomes a function of the data stored from 20000H to 2000FH.

15) While executing the NOP instruction, …..
   a) The microprocessor just waits.
   b) The microprocessor performing an interrupt.
   c) The microprocessor is in idle state and the co-processor uses the buses and accesses the memory.
   d) The microprocessor communicates with the I/O device.

Program 3

```
1.        org 100H
2.        LES  DI, [BP]
3.        MOV SI, [BP+04H]
4.        CLD
5.        XLAT
6.        MOV CL, AL
7.        MOV [BX], DI
8.        MOV [BX+2], SI
9.        MOV [BX+4], CX
10.       REPE CMPSB
11.       DEC SI
12.       DEC DI
13.       INC CX
14.   NEXT: MOV AL, ES:[DI]
15.       MOV [SI], AL
16.       INC SI
17.       INC DI
18.       LOOP NEXT
19.       MOV DI, [BX]
20.       MOV SI, [BX+2]
21.       MOV CX, [BX+4]
22.   AGAIN: LODSB
23.       CALL COMPUTE
24.       MOV AL, DL
25.       STOSB
26.       LOOP AGAIN
27.       HLT

28.   COMPUTE: PROC NEAR
29.       MOV DL, 0
30.       PUSH CX
31.       MOV CX,8
32.       NEW: RCL AL, 1
33.       JNC DONE
34.       INC DL
35.   DONE: LOOP NEW
36.       POP CX
37.       NOP
38.       RET
39.   COMPUTE: ENDP
```

Part II: Hardware

Attempt all questions:

12 **QUESTION FOUR:** **[12 points]**

(3) a. Draw the Von Newmann computer architecture, and briefly describe its advantages and limitations.

(3) b. Draw the demultiplexing and buffering circuits for the 8086 microprocessor shown in Figure 1, and explain the importance of address decoding.

(3) c. Briefly describe the purpose of each T state including the wait state in the 8086 processor bus cycle shown in Figure 2. Is this a read or write bus cycle? How many bus cycles are needed to transfer 16 bits of data from the 8088 and 8086 processors to the memory system.

(3) d. If a memory chip of 500ns access time is interfaced to the processor with the bus cycle given in Figure 2, does it require a wait state? What are the factors affecting this decision?

18 **QUESTION FIVE:** **[18 points]**

(3) e. Compare between SRAM and DRAM in terms of memory access time, size, and complexity, and give an example application of each memory type in personal computers.

(3) f. For the memory interface shown in Figure 3, find the address range for each chip. If the 74138 (3-8 decoder) is replaced by a PAL 16L8 programmable decoder, draw the new interface circuit and write the 16L8 program.
Note: PAL 16L8 is constructed with AND/OR gate logic and has 10 fixed inputs, 2 fixed outputs, and 6 pins programmable as inputs or outputs.

(5) g. An 8086 processor is required to interface to:
- 24 KB of EROM at addresses (10000H - 15FFFH).
- 16 KB of SRAM at addresses (16000H - 19FFFH).
- 512 KB of DRAM at addresses (1A000H - 99FFFH).

Design the full interface circuit using the minimum number of resources. You can only use the following chips: NAND gates, 74LS138 (3-to-8 decoder) and 74LS139 (dual 2-to-4 decoder), 74157 (2-to-1 MUX), 2716 (2K×8) EPROM, TMS 4016 (2K×8) SRAM, and TMS 4464 (64K×4) DRAM. Chip pinouts are shown in Figure 4. Calculate the required number of memory and decoder chips and draw the full interface circuitry.
Hint: You should select an appropriate decoding method to minimize the number of decoders used in the 8086 memory interface.

(3) h. Draw a simplified diagram to illustrate how to connect a memory system of an 8-bit data width to an even parity generator and checker,

and briefly explain how this circuit can help in error detection, and what are its limitations.

(4) i. Test if these code words are correct (D93H, D97H, DD7H, C93H), assuming they were created for a single byte of data using an even parity Hamming Code. If one is incorrect, indicate what the correct code word should have been. Also, indicate what the original data was.

20 **QUESTION SIX:** **[20 points]**

(4) a. Write the necessary assembly instructions to load the appropriate control word to program the 8255 PPI for the I/O configuration shown in Figure 5, add bytes read from Ports A and B, and output the result to Port C. Please reset all do not care bits in the address to zeros if exist.

(4) b. Write the PAL program to interface the 8254 chip shown in Figure 6 to an 8086 microprocessor at I/O ports AF00H, AF02H, AF04H, and AF06H, and write an assembly program to generate a 100KHz square-wave (mode 3) at counter OUT0 and a 200KHz continuous pulse (mode 2) at counter OUT1.

(3) c. Explain a method to measure the period between two events (events generate pulses) using 8254 (No assembly programs are needed).

(5) d. Design an interface circuit to establish full-duplex serial communication between two 8088 systems connected through two 16550 UARTs. Both UARTs are decoded at addresses 40-47H, transmit and receive data at 38,400 bps baud rate, and operated with an 18.432 MHz crystal oscillator. A serial frame contains 8 data bits, an even parity bit, and one stop bit. Draw the interface circuit and write assembly programs to initialize both UARTs, transmit 16 bytes from a small buffer in the data segment of the first system memory, and receive the 16 bytes and store them in a small buffer in the data segment of the other system memory. Choose arbitrary values for the transmit and receiving buffer addresses. The necessary information to write your program is shown in Figure 7. The table defines the register addresses, followed by the line control register, followed by FIFO control register, and finally the line status register.

e.

(4) i. List the events that occur for any interrupt instruction, and compare between software and hardware interrupts.

ii. Compare between the daisy-chined mechanism and the programmable interrupt controller for processing multiple interrupt requests.

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Code	Explanation
00	Memory mode, no displacement
01	Memory mode, 8-bit displacement
10	Memory mode, 16-bit displacement
11	Register mode, no displacement
*Except when R/M=110, then 16 bit displacement	

Segment codes:

Register	SR
ES	00
CS	01
SS	10
DS	11

Mode = 11			Effective address Calculation			
R/M	W=0	W=1	R/M	Mode=00	Mode=01	Mode=10
000	AL	AX	000	[BX]+[SI]	[BX]+[SI]+D8	[BX]+[SI] +D16
001	CL	CX	001	[BX]+[DI]	[BX]+[DI] +D8	[BX]+[DI] +D16
010	DL	DX	010	[BP]+[SI]	[BP]+[SI] +D8	[BP]+[SI]+D16
011	BL	BX	011	[BP]+[DI]	[BP]+[DI] +D8	[BP]+[DI]+D16
100	AH	SP	100	[SI]	[SI] +D8	[SI] +D16
101	CH	BP	101	[DI]	[DI] +D8	[DI] +D16
110	DH	SI	110	Direct address	[BP]+D8	[BP]+D16
111	BH	DI	111	[BX]	[BX] +D8	[BX]+D16

MOV=Move:

Register/memory to/from register	100010dw	Mod Reg R/M	Disp-lo	Disp-hi		
Immediate to register/memory	1100011w	Mod 000 R/M	Disp-lo	Disp-hi	Data	Data if w=1
Immediate to register	1011wReg	Data	Data if w=1			
Register/memory to Segment Register	1000 1110	Mod 0 SR R/M				
Segment Register to Register/memory	1000 1100	Mod 0 SR R/M				

LOOP: loop CX times

1110 0010	Displacement

The Flag Register

				O	D	I	T	S	Z		A		P		C

The Conditional Jump instructions

Instruction	Flags	Function
JZ	ZF = 1	Jumps if zero
JNC	CF = 0	Jumps if no carry

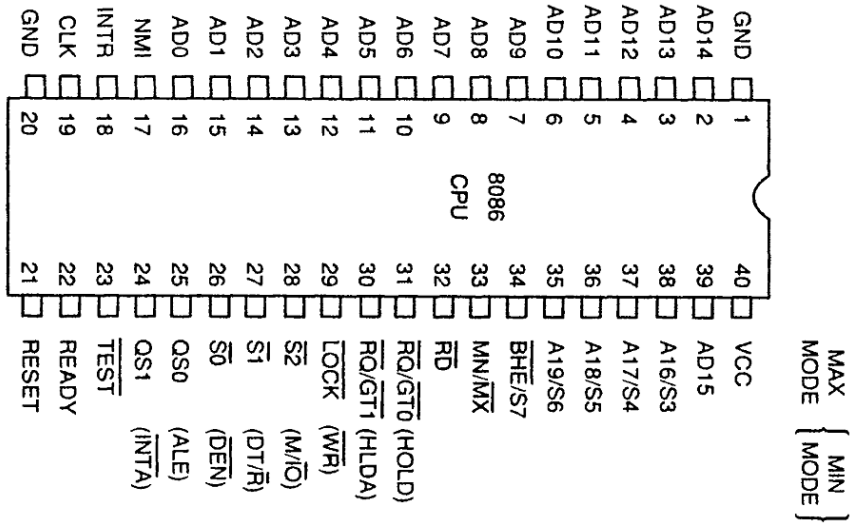


Figure 1

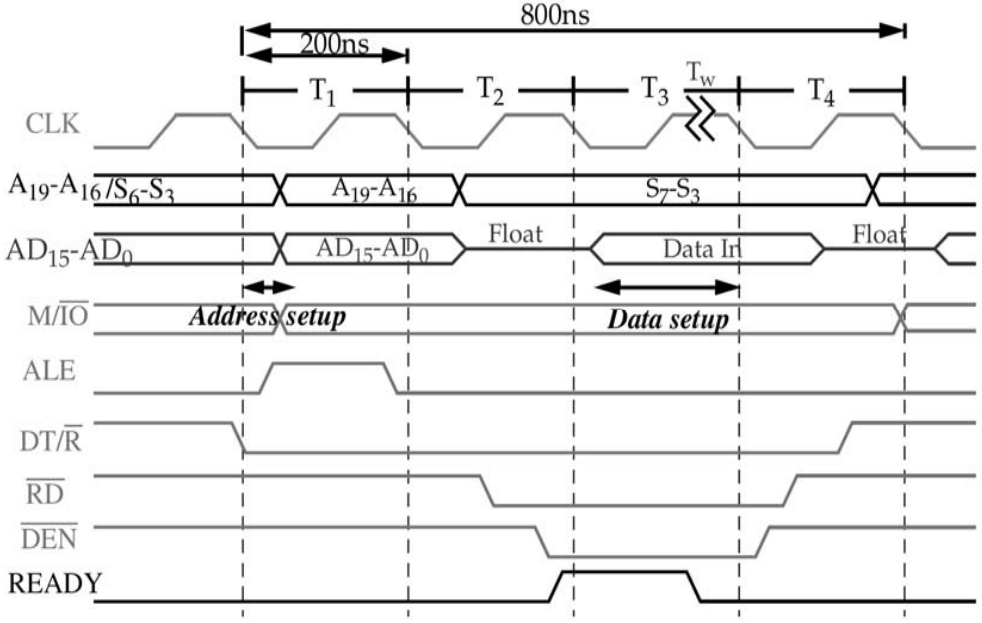


Figure 2

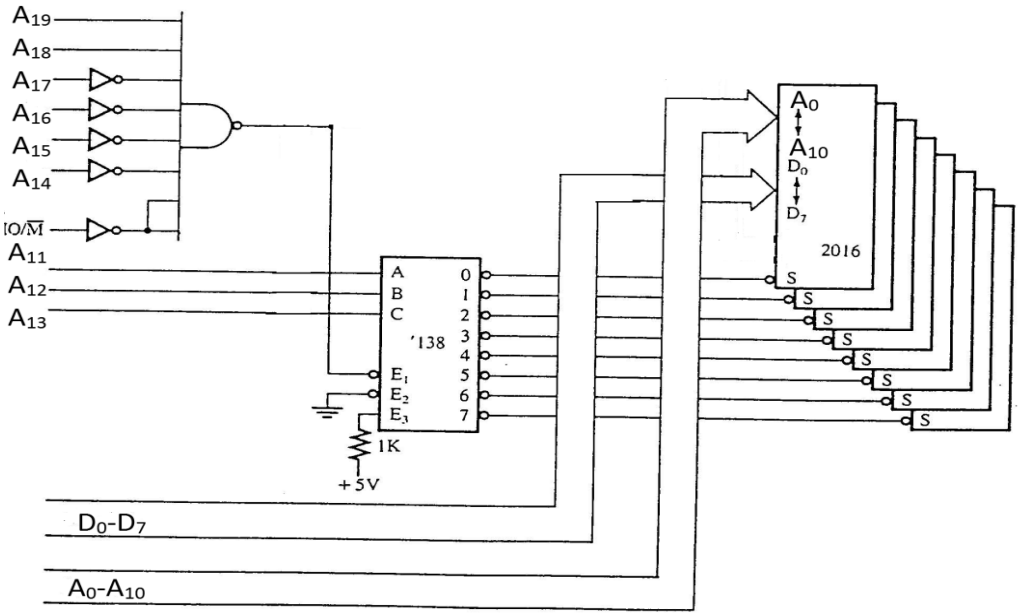


Figure 3

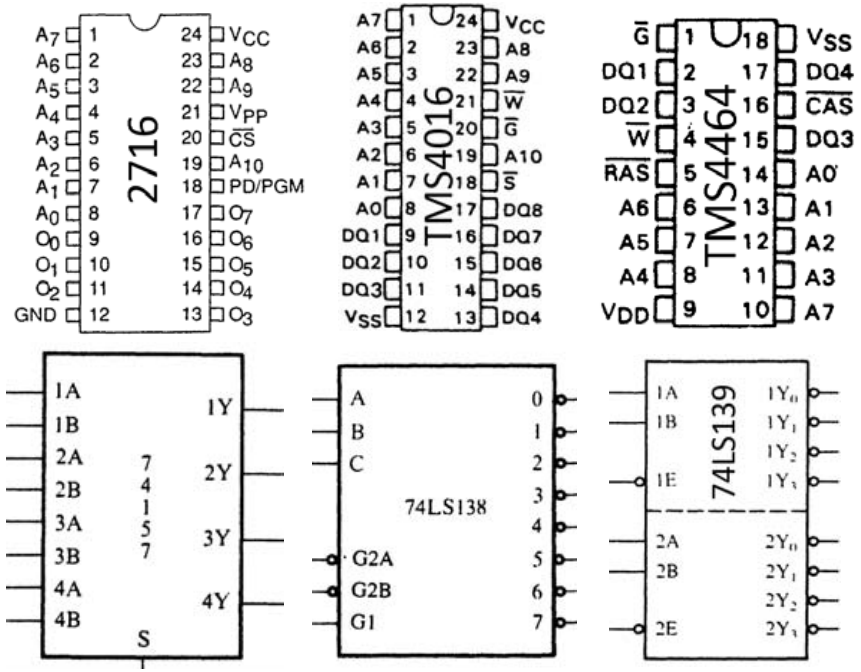


Figure 4

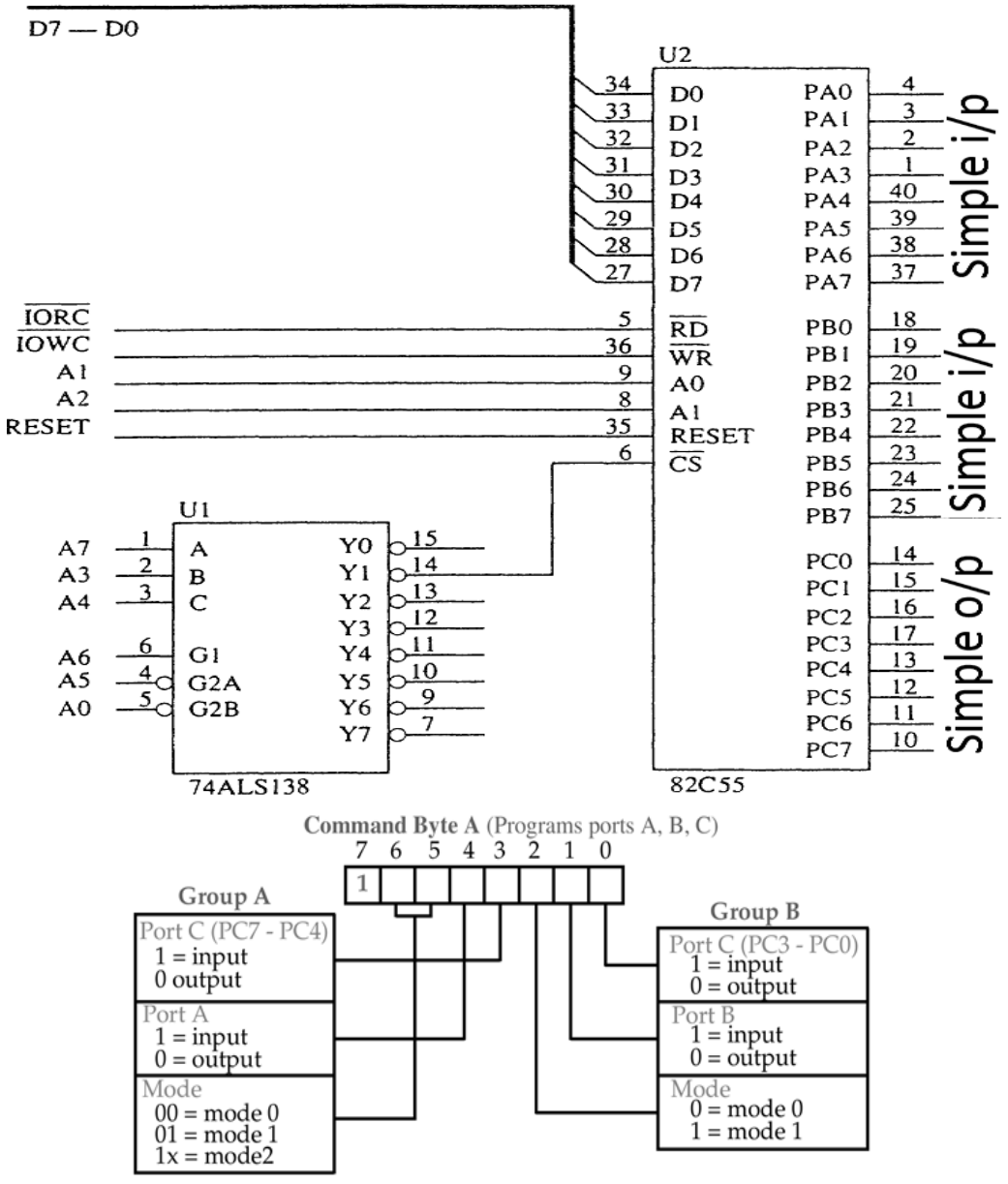
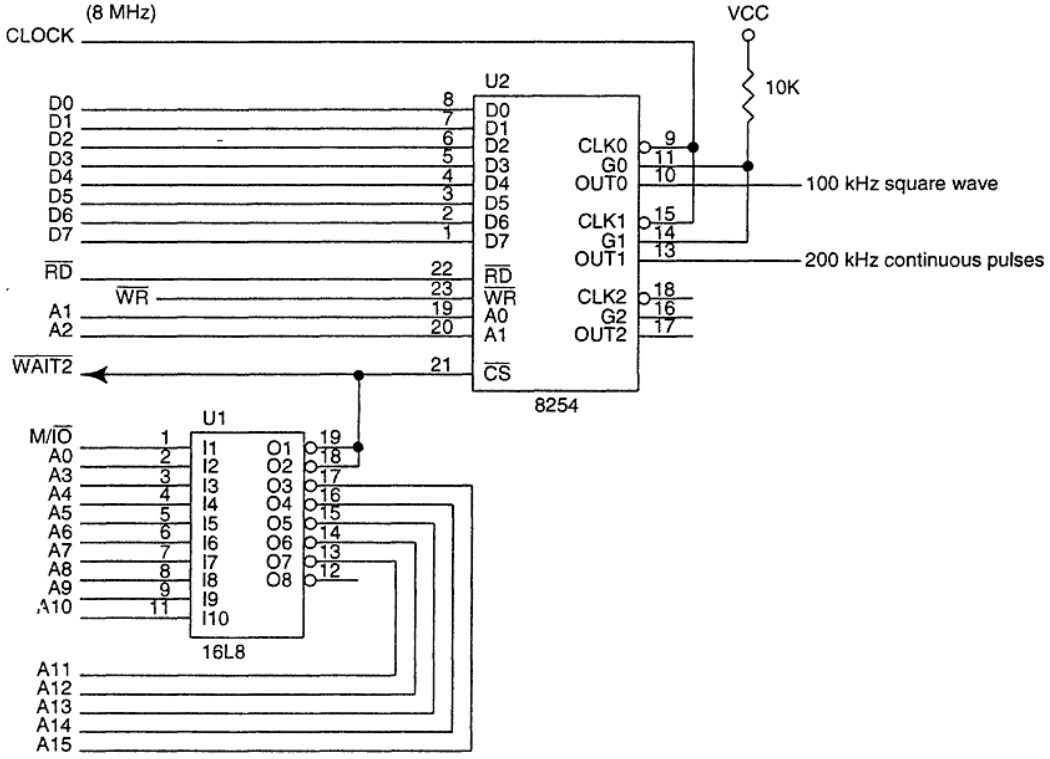


Figure 5



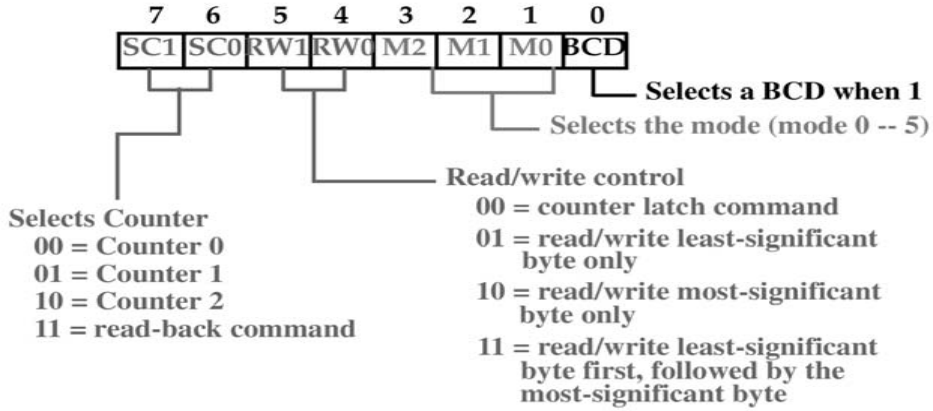
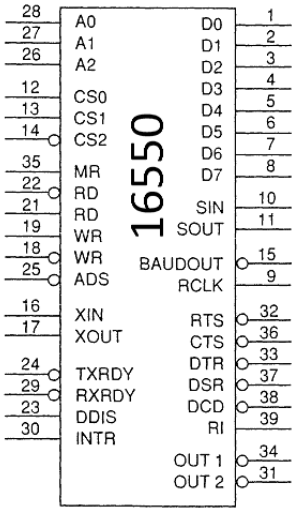
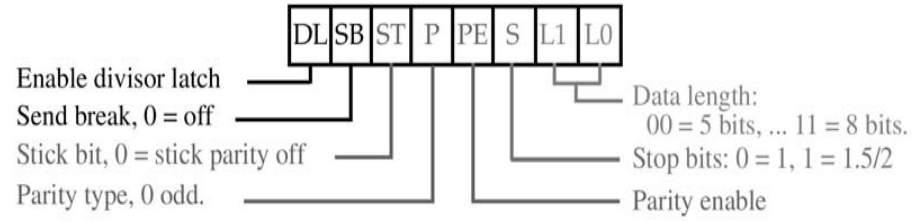


Figure 6



A_2	A_1	A_0	Register
0	0	0	Receiver buffer (read) and transmitter holding (write)
0	0	1	Interrupt enable
0	1	0	Interrupt identification (read) and FIFO control (write)
0	1	1	Line control
1	0	0	Modem control
1	0	1	Line status
1	1	0	Modem status
1	1	1	Scratch



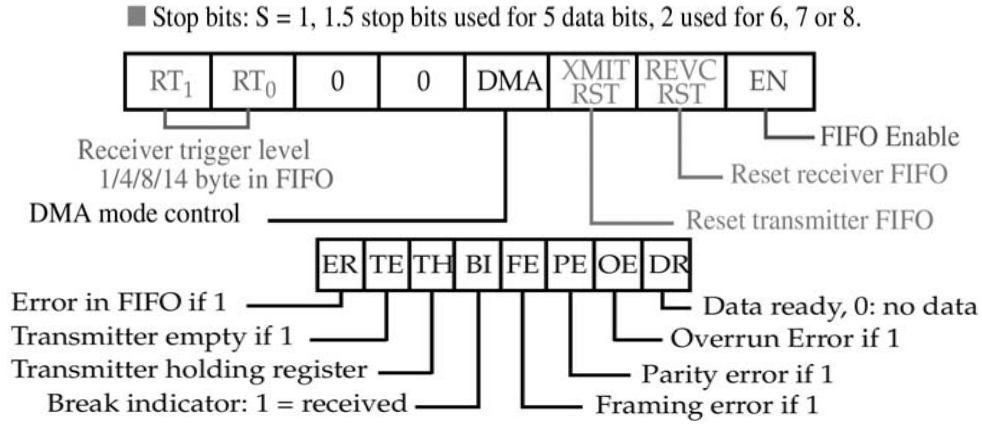


Figure 7