Chapter 16:

1. For the Figure below answer the following questions:
   a. Draw the Block Diagram describing the charge situation inside an ideal *p*-bulk MOS-C biased at the onset of inversion.
    b. Is your part (a) diagram in agreement with the plot of ρ/qN_A versus x in the below figure? Explain why the ρ/qN_A plot has a spike-like nature near $x = 0$ and shows a value of $\rho/qN_A = -2$ at $x = 0$.
    c. Noting that $\phi_F/(KT/q) = 12$ and $T = 300$ K was assumed in constructing the below figure, determine W_T. Is the deduced W_T consistent with the approximate charge distribution shown in the figure?
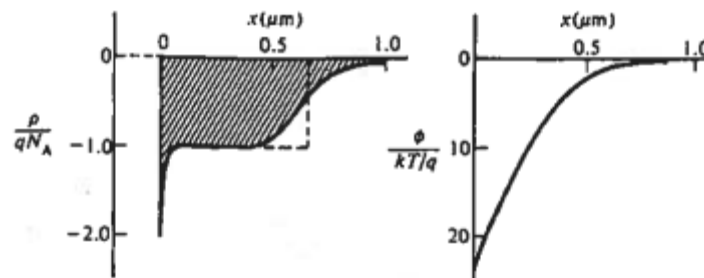

2. An MOS-C is maintained at $T = 300$ K, $x_o = 0.1$ µm and the Si doping is $N_D = 10^{15}$ / cm^3. Compute:
    a. ϕ_F in KT/q units and in volts
    b. W when $\phi_s = 2\phi_F$
    c. ε_s when $\phi_s = 2\phi_F$
    d. $V_G = V_T$ when $\phi_s = 2\phi_F$ and state how the result is related to the figure below.
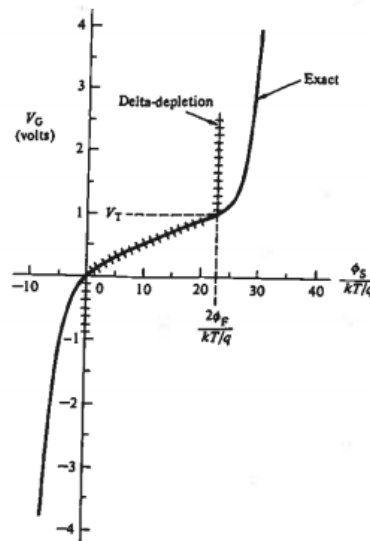
3. The energy band diagram for an ideal $x_o = 0.2$ μm MOS-C operated at T = 300 K is sketched in the below figure. Note that the applied gate voltage causes band bending in the semiconductor such that $E_F = E_i$ at the Si-SiO$_2$ interface. Invoke the delta-depletion approximation as required in answering the questions that follow.
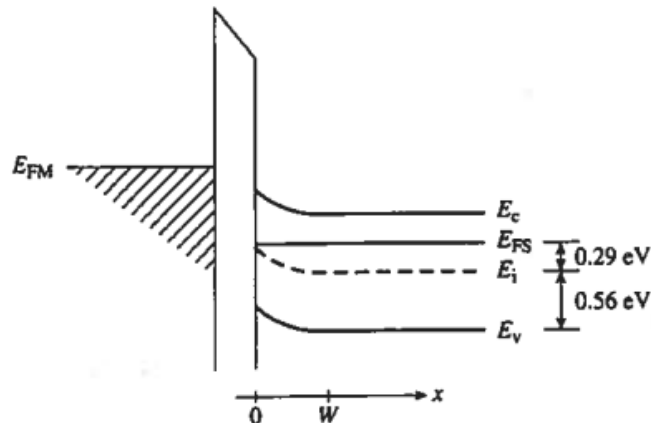
a. Sketch the electrostatic potential (ϕ) inside the semiconductor as a function of position.
b. Roughly sketch the electric field (ε) inside the oxide and semiconductor as a function of position.
c. Do equilibrium conditions prevail inside the semiconductor? Explain.
d. Roughly sketch the electron concentration versus position inside the semiconductor.
e. What is the electron concentration at the Si-SiO$_2$ interface?
f. $N_D = ?$
g. $\phi_s = ?$
h. $V_G = ?$
i. What is the voltage drop ($\Delta\phi_{ox}$) across the oxide?
j. What is the normalized small-signal capacitance, C/C_o, of the MOS-C at the pictured bias point?

4. The below figure is a dimensioned energy band diagram for an ideal MOS-C operated at T = 300 K with $V_G \neq 0$. Note that $E_F = E_i$ at the Si-SiO$_2$ interface.
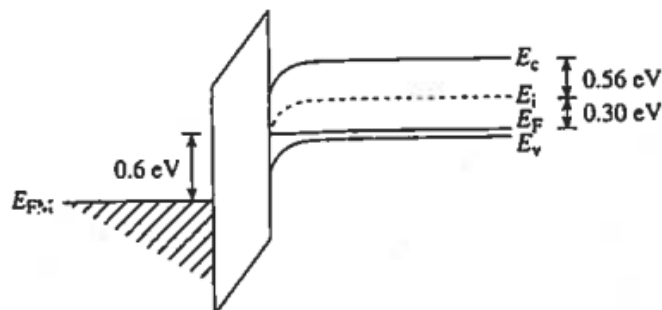
a. Do equilibrium conditions prevail inside the semiconductor?
b. $\phi_F = ?$
c. $\phi_s = ?$
d. $V_G = ?$
e. $x_o = ?$

f. Draw the block charge diagram corresponding to the state pictured in the energy band diagram. For reference purposes, include the maximum equilibrium depletion width, W_T, on your diagram.

g. Sketch the general shape of the low- frequency C-V characteristic to be expected from the given MOS-C. Place an X on the C-V characteristic at a point that roughly corresponds to the state pictured in the energy band diagram.

h. For the specific bias point pictured in the energy band diagram, which of the following is the correct expression for the capacitance exhibited by the structure? Explain.

$$\text{(i) } C = \frac{C_O}{1 + \dfrac{K_O W_T}{K_S x_o}},$$

$$\text{(ii) } C = \frac{C_O}{\sqrt{1 + \dfrac{V_T}{2V_\delta}}},$$

$$\text{(iii) } C = \frac{C_O}{1 + \dfrac{K_O W_T}{\sqrt{2} K_S x_o}},$$

$$\text{(iv) } C = \frac{C_O}{\sqrt{1 + \dfrac{V_T}{V_\delta}}}$$

5. With modern-day processing it is possible to produce semiconductor-oxide-semiconductor (SOS) capacitors in which a semiconductor replaces the metallic gate in a standard MOS-C. Answer the following questions assuming an SOS-C composed of two identical n-type nondegenerate silicon electrodes, an ideal structure, and a biasing arrangement as defined by the below figure. Include any comments which may help to forestall a misinterpretation of the requested pictorial answers.

   a. Draw the energy band diagram for the structure when (i) $V_G=0$, (ii) $V_G>0$ but small, (iii) $V_G>0$ and very large, (iv) $V_G<0$ but small, and (v) $V_G<0$ and very large.

   b. Draw the block charge diagrams corresponding to the five biasing conditions considered in part (a)

   c. Sketch the expected shape of the high frequency C-V characteristic for the SOS-C described in this problem. For reference purposes, also sketch on the same plot the high frequency C-V_G characteristic of an MOS-C assumed to have the same semi-conductor doping and oxide thickness as the SOS-C.
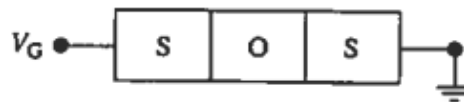
6. The C-V characteristic exhibited by an MOS-C (assumed to be ideal) is displayed in the figure below.
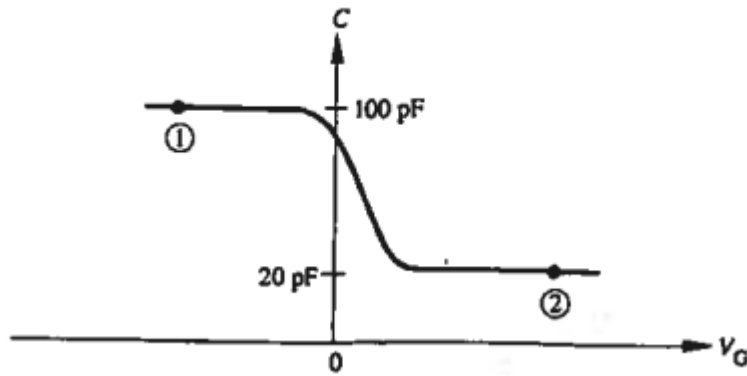
a. Is the semiconductor component of the MOS-C doped n-type or p-type? Indicate how you arrived at your answer.
b. Draw the MOS-C energy band diagram corresponding to point 2 on the C-V characteristic. (Be sure to include the diagrams for all three components of the MOS-C, show the proper band bending in both the oxide and semi-conductor, and properly position the Fermi level in the metal and semiconductor.)
c. Draw the block charge diagram corresponding to point 1 on the C-V characteristic.
d. If the area of the MOS-C is 3×10^{-3} cm^2, what is the oxide thickness (x_o)?
e. Invoking the delta-depletion approximation, determine W_T and the associated semi-conductor doping concentration for the given MOS-C.

Chapter 17:

1. Given an ideal p-channel MOSFET maintained at room temperature:
   a. Assuming $V_D = 0$, sketch the MOS energy band diagram for the gate region of the given transistor at threshold.
   b. Assuming $V_D = 0$, sketch the MOS block charge diagram for the gate region of the given transistor at threshold.
   c. Sketch the inversion layer and depletion region inside the MOSFET at pinch-off. Show and label all parts of the transistor.

2. Construct a plot of V_T versus N_A for ideal n-channel MOSFETs operated at room temperature. Superimpose on the same plot the curves corresponding to $x_o = 0.01$, 0.02, 0.05, and 0.1 μm. Let the semiconductor doping vary over the range $10^{14} / \text{cm}^3 \le N_A \le 10^{18} / \text{cm}^3$; limit the plotted V_T to $0 \le V_T \le 3$ V.

3. Suppose a battery $V_B \geq 0$ is connected between the gate and drain of an ideal n-channel MOSFET as pictured in the figure. Using the square law results,

    a. Sketch I_D versus V_D ($V_D \geq 0$) if $V_B = V_T / 2$;
    b. Sketch I_D versus V_D ($V_D \geq 0$) if $V_B = 2\,V_T$.
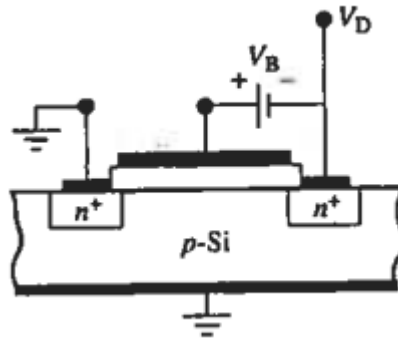
4. The most widely encountered MOSFET characteristics are a plot of I_D versus V_D with V_G or $V_G - V_T$ held constant at select values. An alternative plot of I_D versus V_G or $V_G - V_T$ with V_D held constant at select values is sometimes useful. Sketch the shape of the I_D versus $V_G - V_T$ characteristics to be expected from an ideal n-channel MOSFET. Specifically show the characteristics corresponding to $V_D = 1$, 2, 3, and 4 V. Explain how you arrived at your sketch.

5. An I_D - V_D characteristic derived from an ideal MOSFET is pictured in the figure below. Note that $I_{Dsat} = 10^{-3}$ A and $V_{Dsat} = 5$ V for the given characteristic. Answer the questions that follow making use of the square-law theory and the information conveyed in the figure.
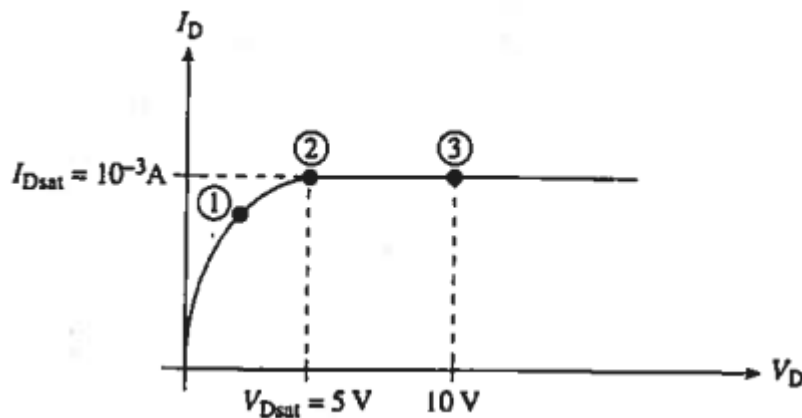
    a. Carefully sketch the inversion layer and depletion region inside the MOSFET corresponding to point (1) on the pictured characteristic. Show and label all parts of the transistor.
    b. Given a turn-on voltage of $V_T = 1$ V, what is the gate voltage one must apply to the MOSFET gate to obtain the pictured characteristic?
    c. If $x_o = 0.1\ \mu$m, what is the inversion-layer charge / cm^2 at the drain end of the channel when the MOSFET is biased at point (2) on the characteristic?
    d. Suppose the gate voltage is readjusted so that $V_G - V_T = 3$V. For the new condition, determine I_D if $V_D = 4$ V.

e. Determine g_d if the quiescent operating point of the MOSFET is point (3) on the pictured characteristic.
f. Determine g_m if the quiescent operating point of the MOSFET is point (3) on the pictured characteristic.
g. If $V_D = 0$ (i.e., the drain is shorted to the source and back), sketch the general shape of the C_G (gate capacitance) versus V_G characteristic to be expected from the MOSFET.