MOS CAPACITORS

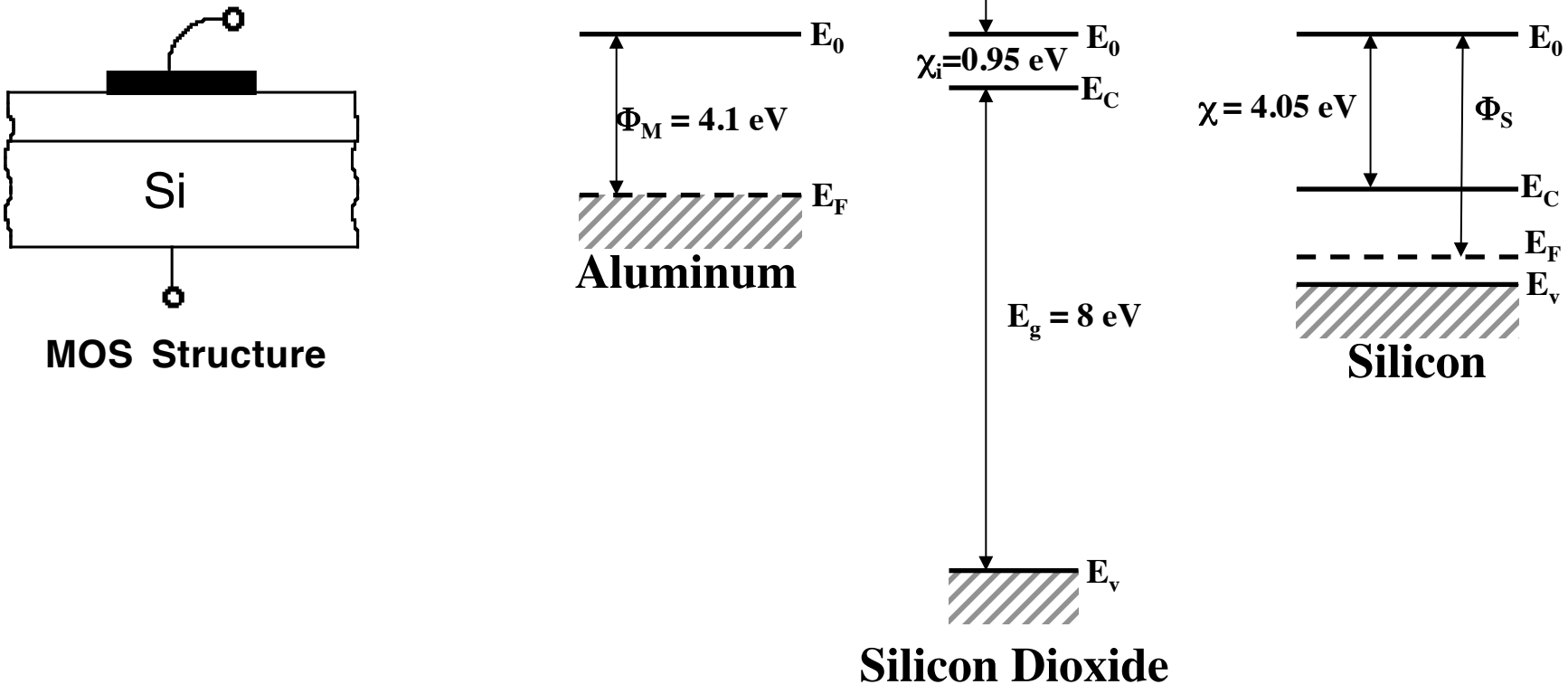
Why should we study MOS capacitors?

- A good chunk of electronics industry is spawned by MOS capacitor
  - ✓ With 2 p-n junctions added it makes a MOS transistor
  - ✓ Heart of DRAM
  - ✓ CCD imagers
  - ✓ Analog to digital converters

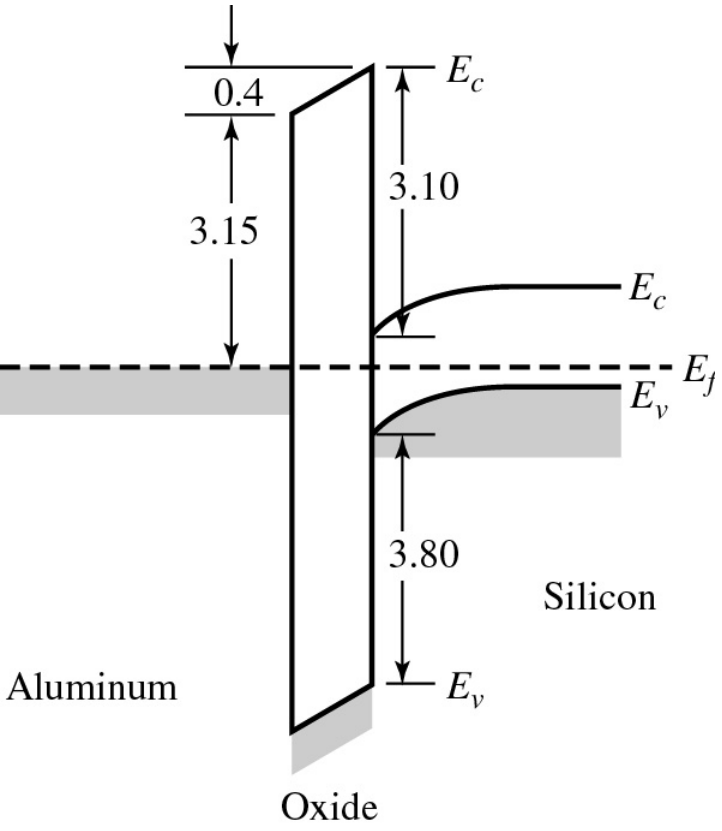
MOS CAPACITORS: Band Diagrams

I. Band Diagrams

Metal-Oxide-Silicon (MOS) is the single most important component for a large number of semiconductor devices.



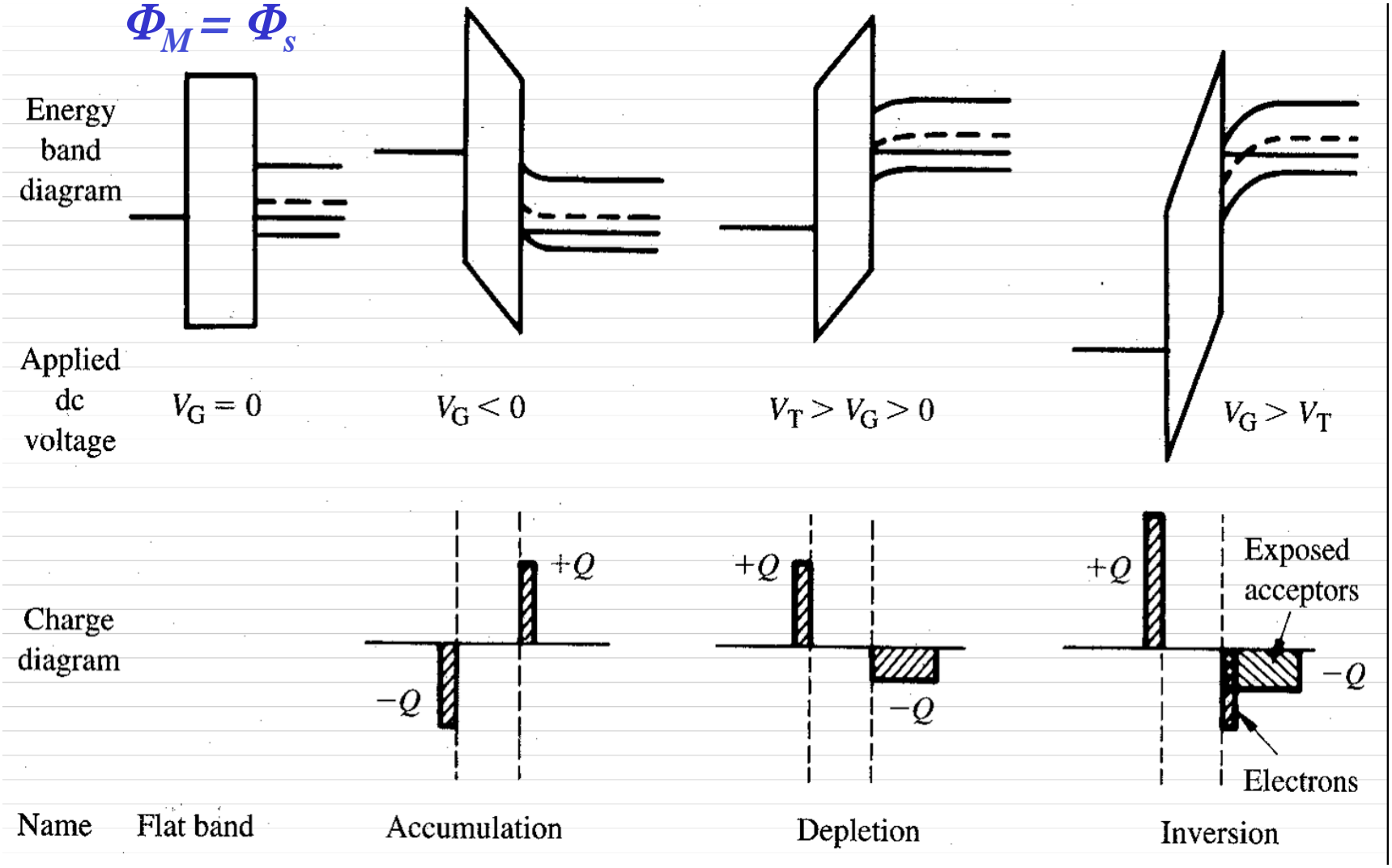
Equilibrium Considerations



Bringing 3 materials into contact, E_F is constant at thermal equilibrium just as in Schottky contact or P-N diode.

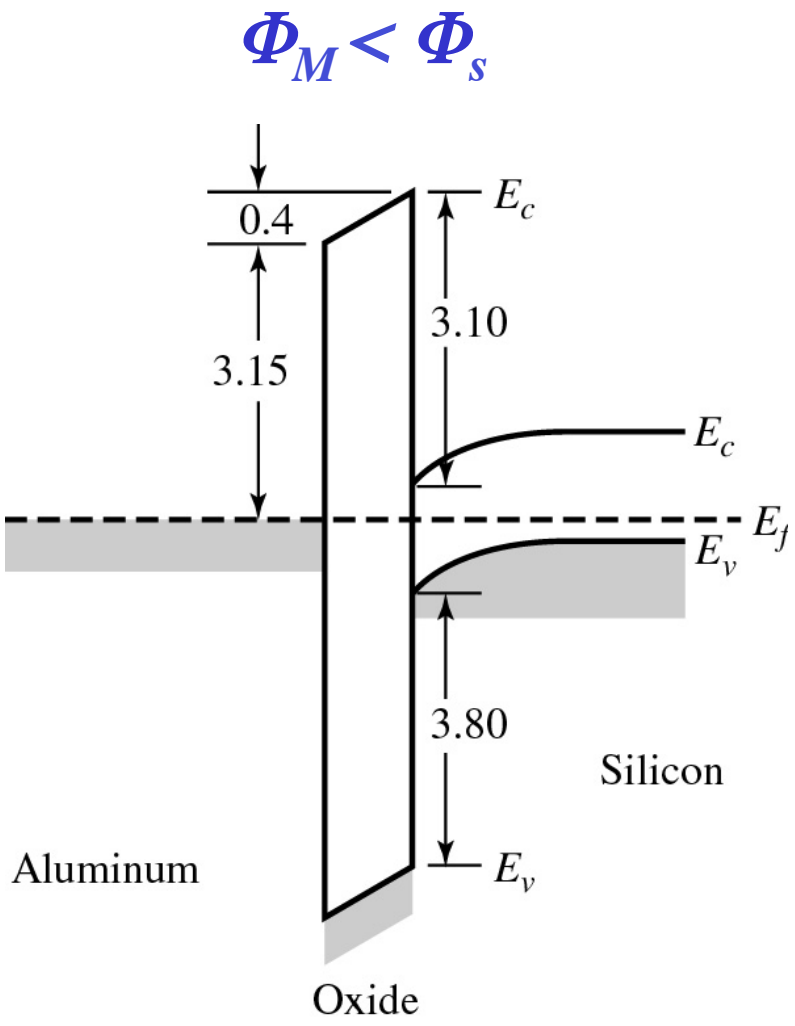
Currents **through** SiO_2 are very small, a long time (decades) is needed for equilibrium to be established. To realistically establish equilibrium, an alternative conduction path must be provided, e.g., the external circuit. This long storage time is the foundation for flash memory.

Bias Conditions for Ideal MOS Capacitor



Potential is dropped across SiO_2 and Si.

MOS Capacitor: Equilibrium, Applied V = 0



1) In this example, holes are at higher average energy in P-type Si than in metal ($\Phi_M < \Phi_s$). Holes go from Si to metal.

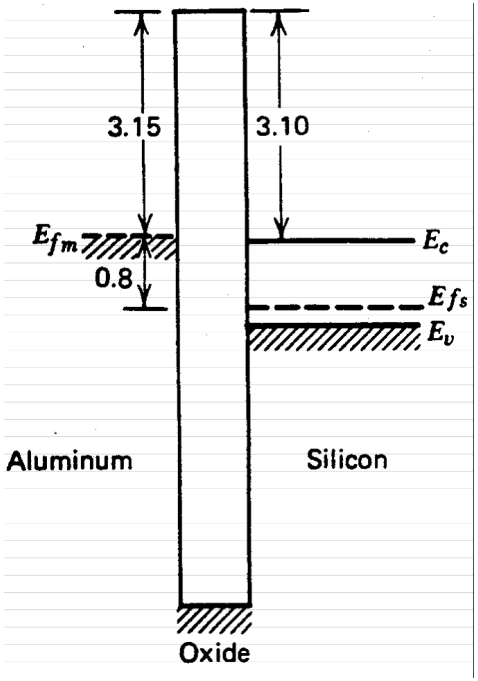
2) Abrupt transition in E_c and E_v levels at material interfaces.

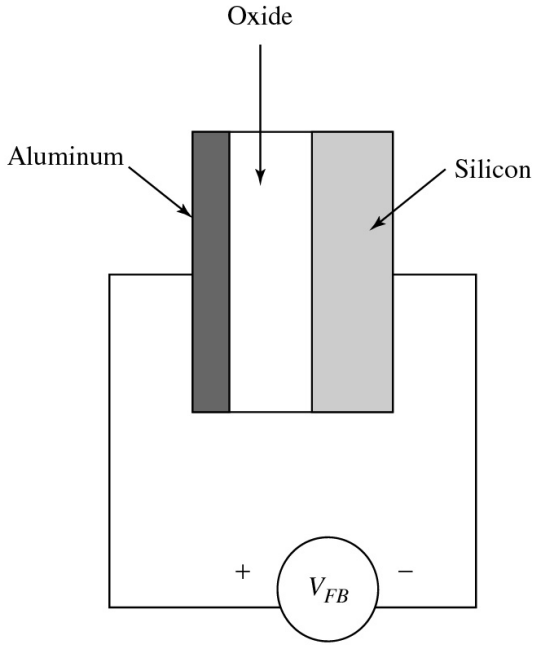
2) A potential $\Phi_M - \Phi_s$ is dropped across SiO_2 and in Si. Bands will bend down (becoming less P-type) at Si surface. This potential can be supported because no current flows through SiO_2.

3) Substantial barriers exist for carriers flowing from S → M and from M → S.

4) Near the Si surface, E_F is further from E_v than in bulk, the surface is depleted of holes (DEPLETION).

MOS Capacitor: Flat Band Bias $V = \Phi_{MS}$





Flat Band, Applied $V = \Phi_{MS}$ (< 0 for the example shown)

1) E_F is constant in Si because SiO_2 prevents any current flowing (i.e., Si is at equilibrium).

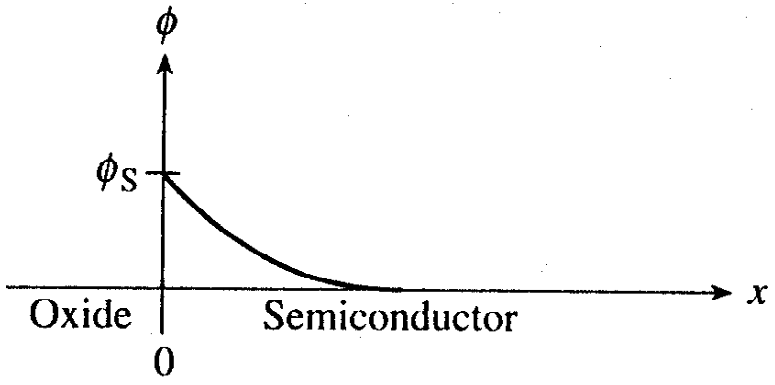
2) E_c and E_v are flat, and the hole concentration is uniform in Si. $\rho = 0$, electric field $\mathcal{E} = 0$ in Si, $\mathcal{E} = 0$ in SiO_2 (as indicated by flat E_c and E_v).

4) This is known as FLAT BAND, the voltage required to achieve this condition is $V_{FB} = \Phi_{MS}$

Potential and Surface Potential

$$\phi_S = \frac{1}{q}\left[E_i(bulk) - E_i(surface)\right]$$

where ϕ_s is the surface potential, not the semiconductor work-function, Φ_s.



(a)

Potential in the depletion region is:

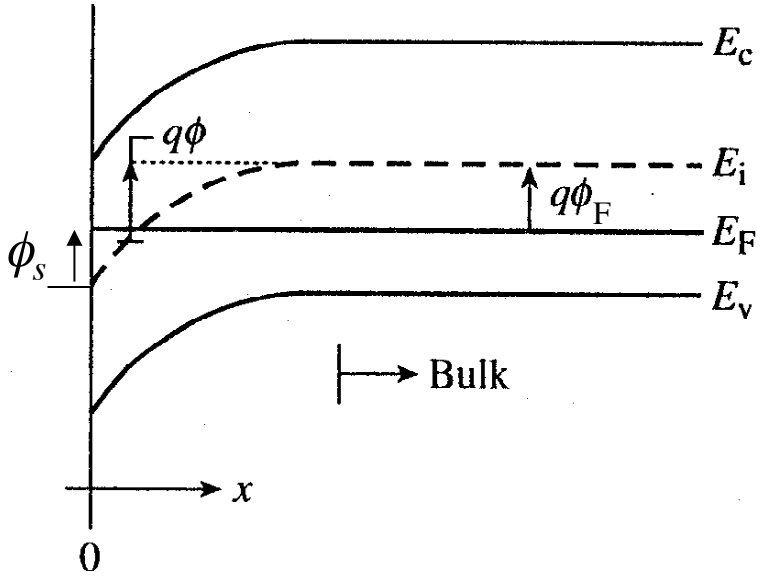
$$\phi(x) = \frac{1}{q}\left[E_i(bulk) - E_i(x)\right]$$

Potential in the bulk region is:

$$\phi_F = \frac{1}{q}\left[E_i(bulk) - E_F\right]$$

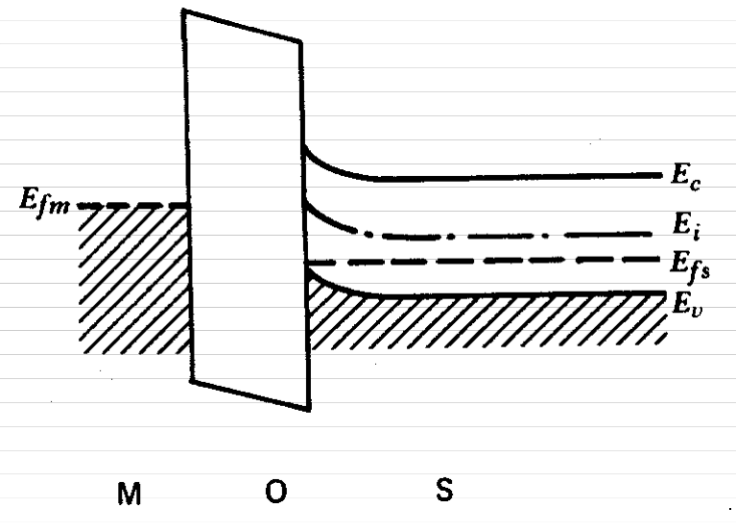
$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad \text{... p - type semiconduct}$$

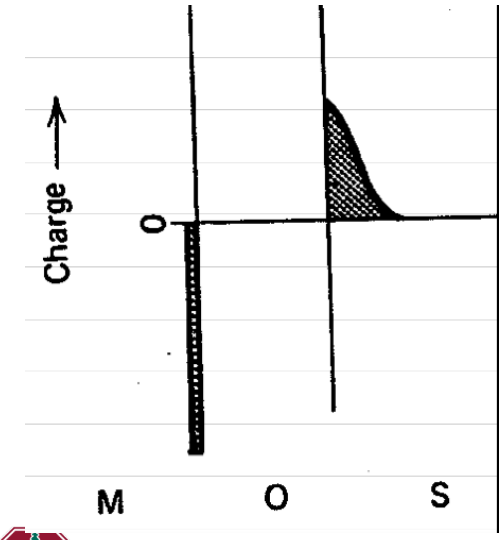
$$= \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) \quad \text{...n - type semiconduct}$$



Accumulation, Applied V < V_{FB}

(V_G more negative)



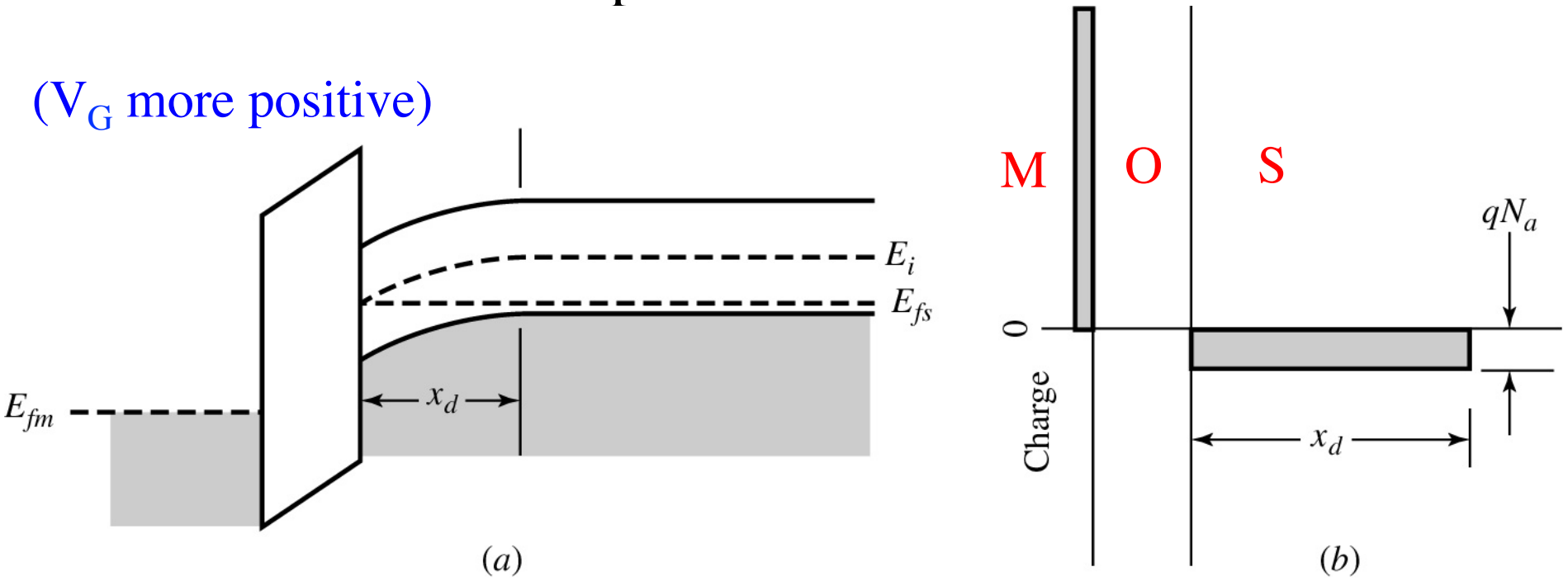


- E_F is still constant in Si as there is no current flow.
- E_F is closer to E_v at the surface. There are more holes accumulated at the surface than in the bulk (ACCUMULATION).
- The holes can be approximated as a thin sheet of charge at the Si surface. The Debye length L_D, is about the same or thinner than the typical SiO_2 thickness. The situation is similar to that of a parallel plate capacitor.

Depletion, Applied V > V_{FB}

Energy-band diagram of an MOS system with *p*-type silicon biased into depletion.

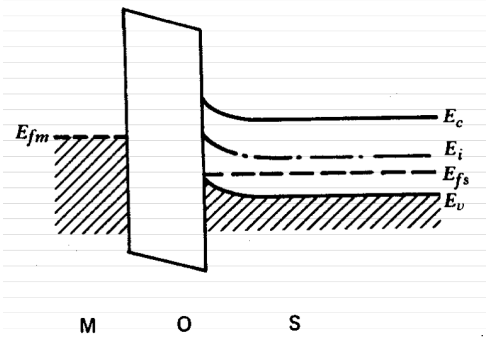
(V_G more positive)



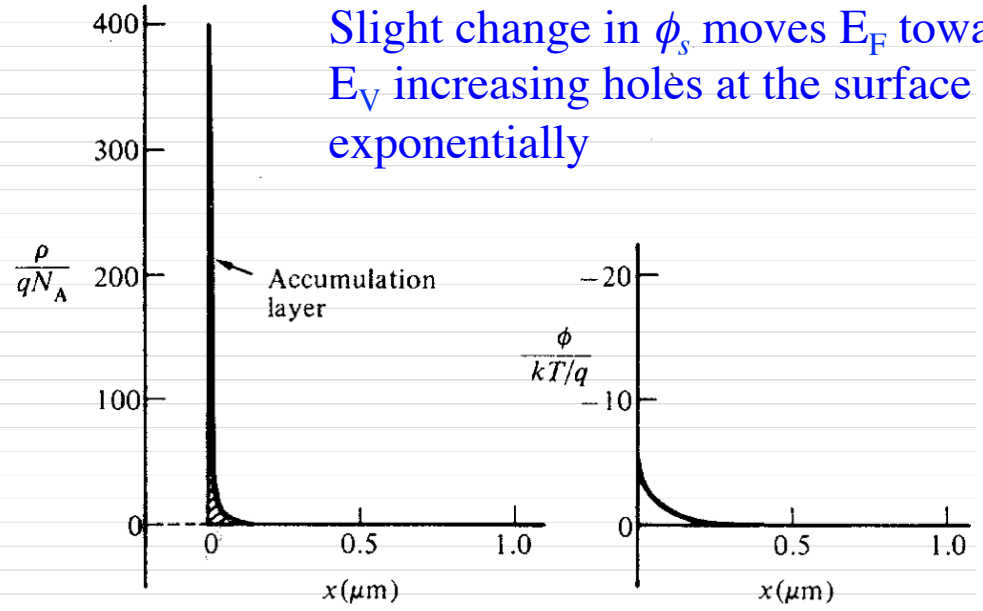
- Positive V_G repels holes away from the surface causing depletion.
- At the surface E_F is now close to E_i.

Charge Distribution and Potential

ACCUMULATION

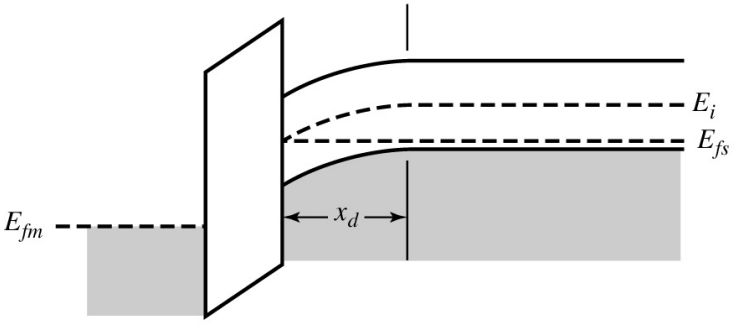


Slight change in ϕ_s moves E_F towards E_V increasing holes at the surface exponentially

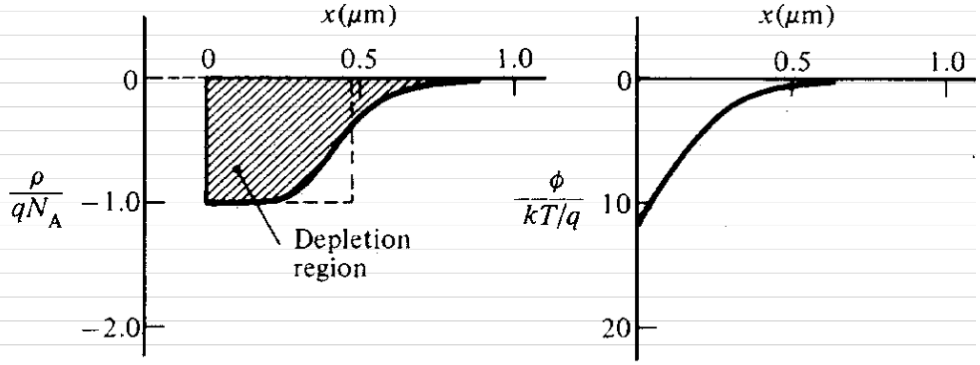


(a) Accumulation ($\phi_S = -6kT/q$)

DEPLETION



Charge in the depletion region limited to N_A



(b) Middle of depletion ($\phi_S = \phi_F = 12kT/q$)

The situation is similar to that of a Schottky contact under a reverse bias except that some of the voltage will be dropped across the SiO_2. Assume a uniform N_A and that the surface is depleted of holes (DEPLETION). From Poisson's Equation,

$$-\frac{dE}{dx} = \frac{d^2\phi}{dx^2} = -\frac{\rho}{K_s\varepsilon_0} = \frac{qN_A}{K_s\varepsilon_0}$$

By integrating the above equation, the electric field and the potential in the depletion region are:

$$E(x) = \frac{qN_A}{K_s\varepsilon_o}(W - x) \qquad (0 \le x \le W) \qquad (1)$$

$$\phi(x) = \frac{qN_A}{2K_s\varepsilon_o}(W - x)^2 \qquad (0 \le x \le W) \qquad (2)$$

From Gauss's Law, the electric displacement ***D*** must be constant across the Si/SiO_2 interface

$$D = K_o \; E_{ox} = K_s \; E_s$$

where K_o and K_s are dielectric constants of SiO_2 and Si, respectively and E_{ox} and E_s are electric fields in SiO_2 and Si, respectively.

This is the source behind the huge efforts today to produce a high K_o dielectric such that the electric field, which controls the surface charge density, will be much lower in the gate dielectric to block tunneling leakage.

At the surface of Si the electric field and surface potential are

$$E_s = \frac{qN_A W}{K_s \varepsilon_o} \qquad \phi_s = \frac{qN_A W^2}{2K_s \varepsilon_o} \tag{3}$$

In SiO_2 the electric field and potential drop are

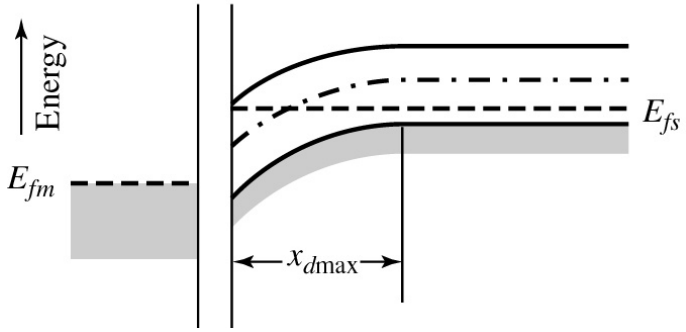
$$E_{ox} = \frac{qN_A W}{K_o \varepsilon_o} \qquad V_{ox} = E_{ox} x_o = \frac{qN_A W x_o}{K_o \varepsilon_o} \tag{4}$$

Total potential drop across the MOS system is

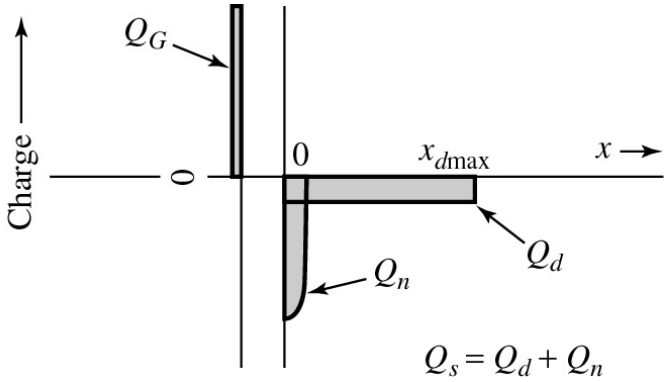
$$\begin{aligned} V &= V_{FB} + V_{ox} + \phi_s \\ &= V_{FB} + \frac{qN_A W x_o}{K_o \varepsilon_o} + \frac{qN_A W^2}{2K_s \varepsilon_o} \end{aligned} \tag{5}$$

W can be solved for known *V*, N_A, and x_o.

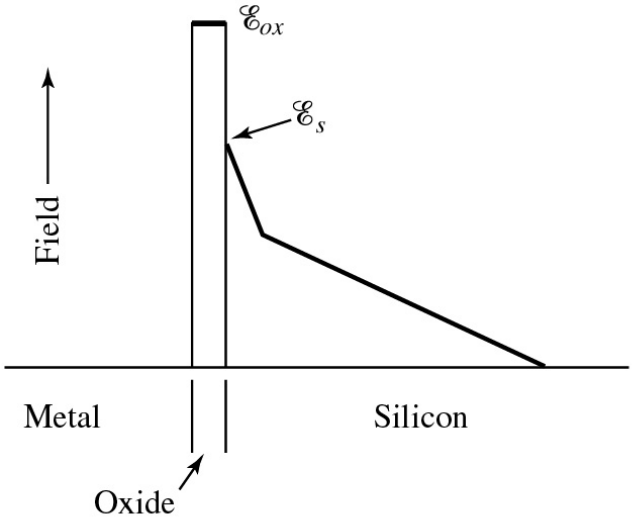
Inversion, Applied V >> V_{FB}



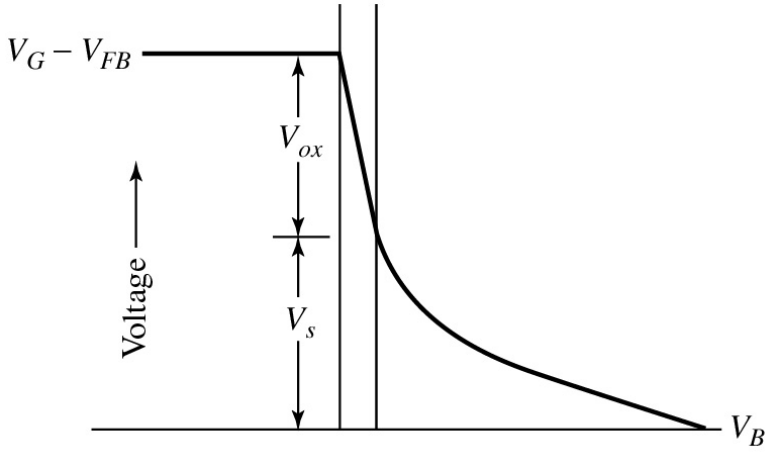
Energy-band diagram



space-charge configuration



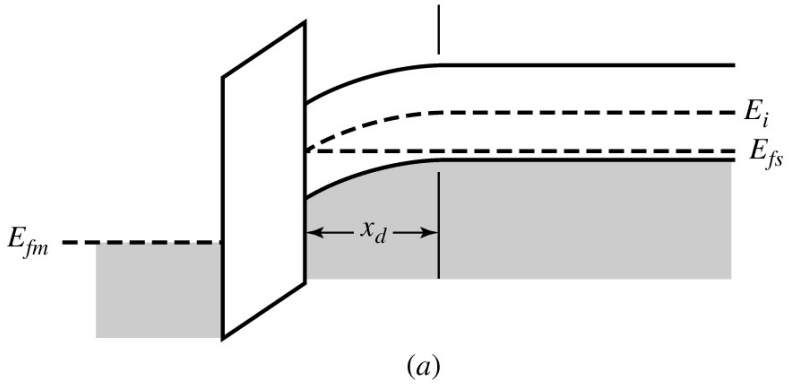
field



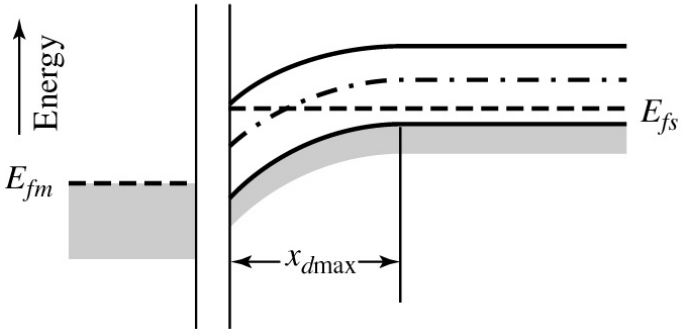
potential distribution

Unlike Schottky contacts, E_F can be defined and is constant in the Si, even with bias because the insulator blocks all current flow.

If $\phi_s = \phi_F$ (E_{fs} at E_i at the surface) the surface will become intrinsic. For $\phi_F < \phi_s < 2\,\phi_F$ (E_{fs} above E_i at the surface) the surface becomes lightly n-type (WEAK INVERSION).



For $\phi_s > 2\,\phi_F$, the surface will have an electron concentration higher than the acceptor (or hole) concentration in the bulk (STRONG INVERSION).



Since

$$n_s = n_i e^{\frac{q}{kT}(\phi_s - \phi_F)}$$

- For $\phi_s > 2\phi_F$, the electrons at the surface will become the dominant charge. Their distribution will be similar to that of holes under accumulation and can be approximated by a sheet of electrons at the Si surface.
- $\phi_s = 2\phi_F$ is defined as the onset of strong inversion.
- Beyond this point, the depletion width remains approximately the same because slight change in Fermi level causes large change in electron density. Hence bends don't bend anymore.

From equation (3)

$$2\phi_F = \frac{qN_A W_T^2}{2K_s\varepsilon_o}$$

where W_T is the Depletion layer width at onset of inversion

$$W_T = \sqrt{\frac{4K_s\varepsilon_o\phi_F}{qN_A}} \qquad (6)$$

The voltage required to reach the start of inversion from Eq. (5) is called the threshold voltage, V_T

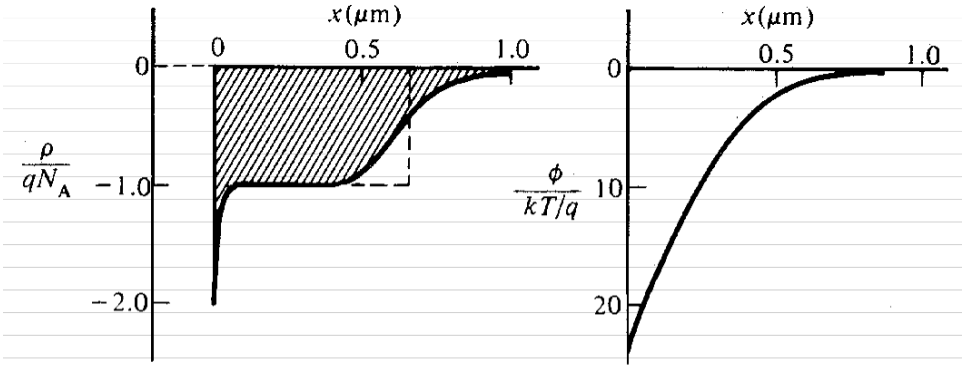
$$V_T = V_{FB} + V_{ox} + \phi_s$$

$$V_T = V_{FB} + \frac{x_o}{K_o \varepsilon_o}\sqrt{4K_s \varepsilon_o q N_A \phi_F} + 2\phi_F$$

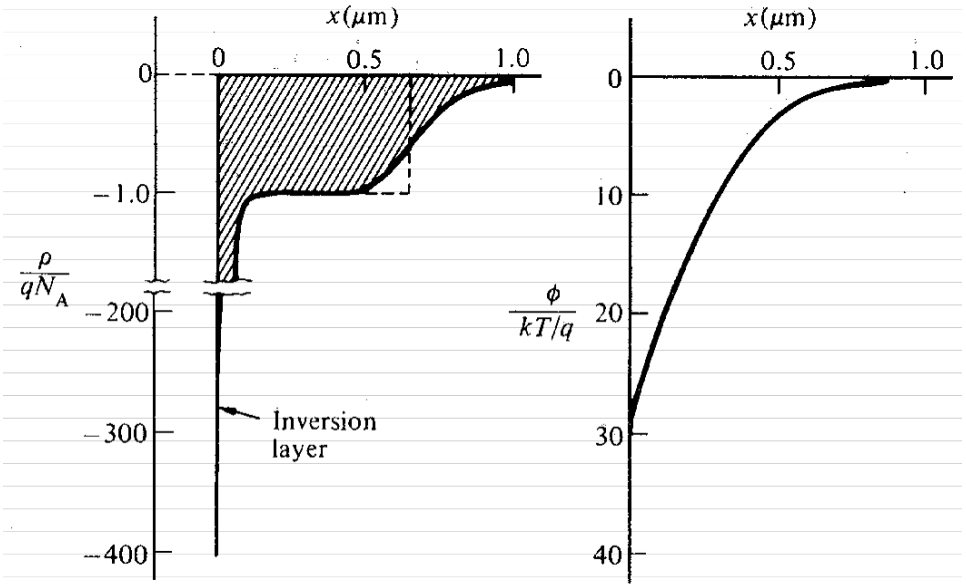
$$= V_{FB} + \frac{1}{C_{ox}}\sqrt{4K_s \varepsilon_o q N_A \phi_F} + 2\phi_F \qquad (7)$$

Gate capacitance per unit area

Charge Distribution and Potential



(c) Onset of inversion ($\phi_S = 2\phi_F = 24kT/q$)



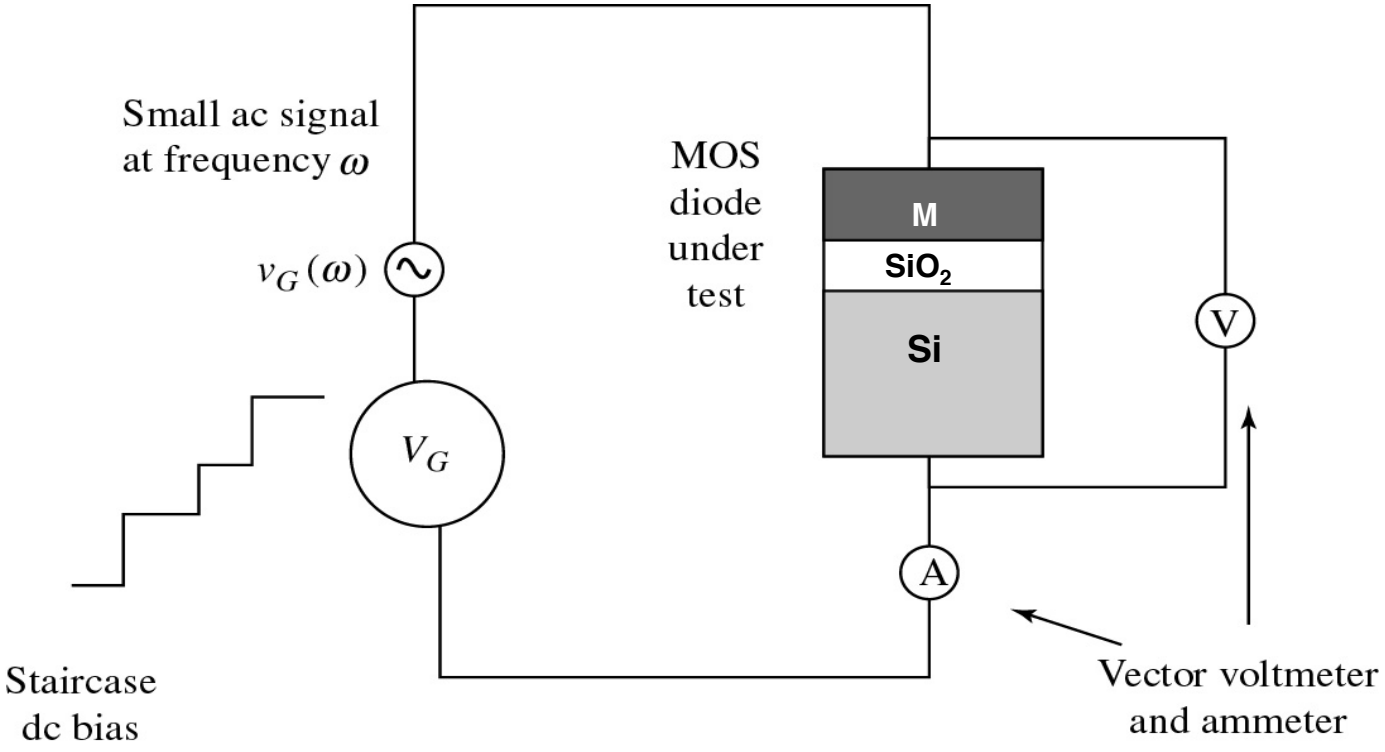
(d) Deep into inversion ($\phi_S = 2\phi_F + 6kT/q = 30kT/q$)

- Once inversion is reached, very little additional potential drops across the semiconductor because a small change in the surface potential increases the surface electron concentration immensely.

$$n_s = n_i e^{\frac{q}{kT}(\phi_s - \phi_F)}$$

- Any additional potential is dropped across the gate dielectric

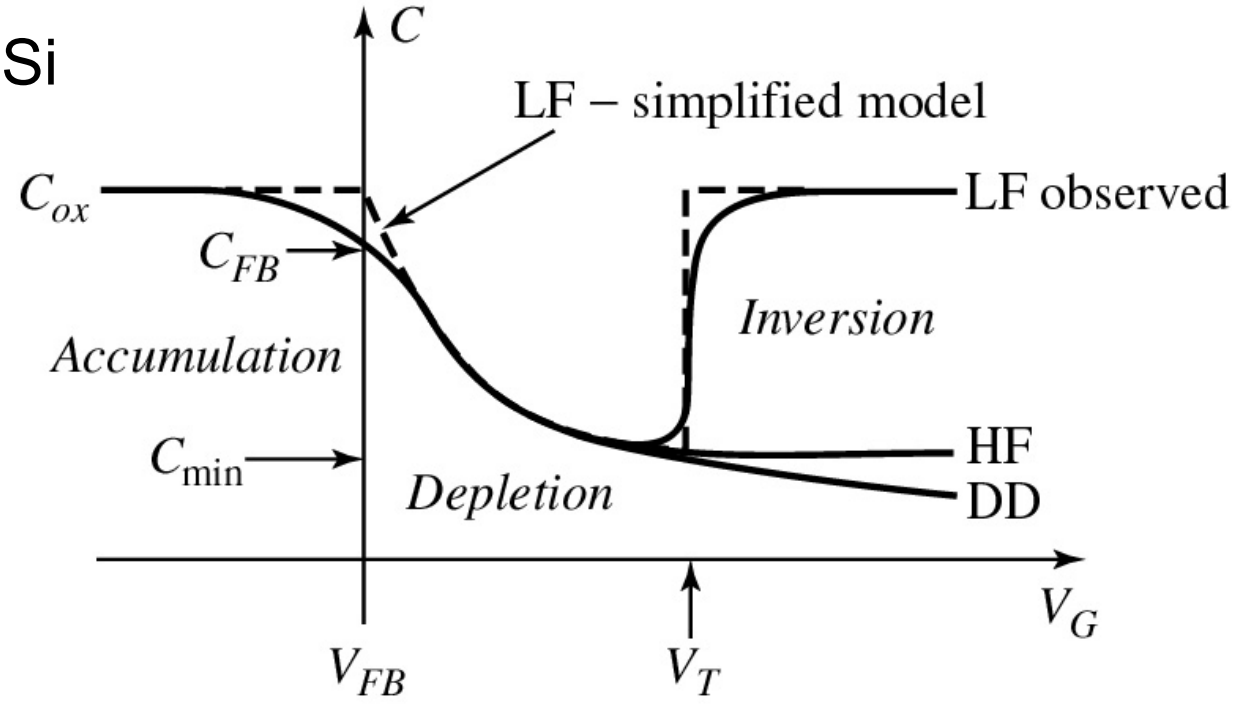
II. MOS *C-V* measurements



To measure the capacitance a DC bias is applied and a small AC signal is then superimposed allowing the measurement of small signal capacitance The DC bias is then swept from -ve to +ve in small increments and C is measured at each point. The DC bias determines the state of the MOS capacitor.

MOS *C-V* characteristics

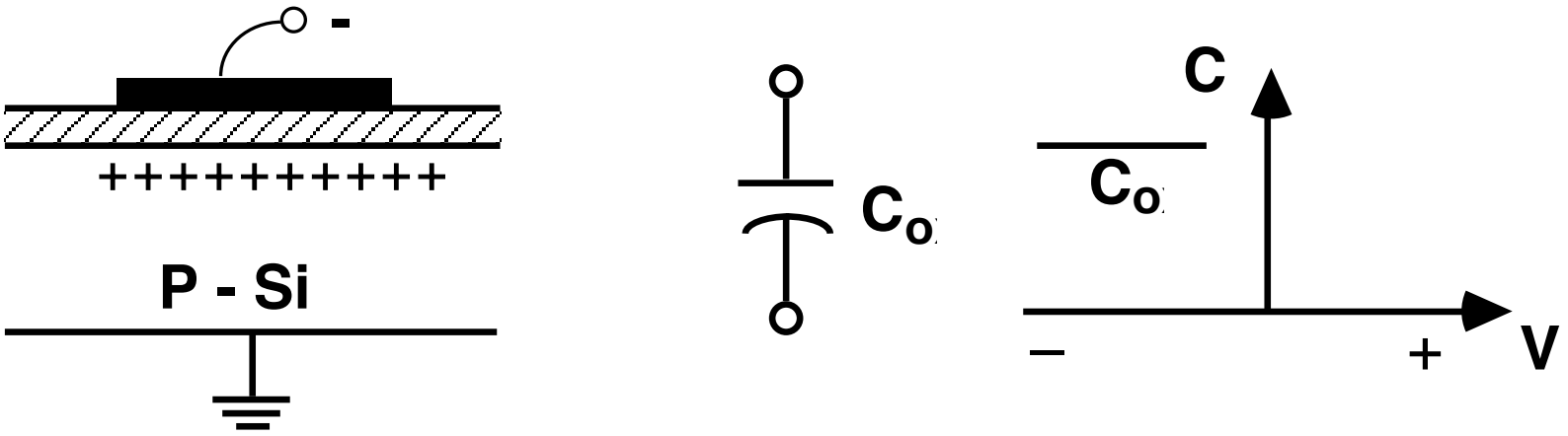
p-type Si



- The value of the measured capacitance depends upon the DC bias, the rate at which it is changing and the measurement frequency.
- The C-V characteristic for N-type Si is a mirror image of the characteristic above.

C-V Characteristics

1. Accumulation

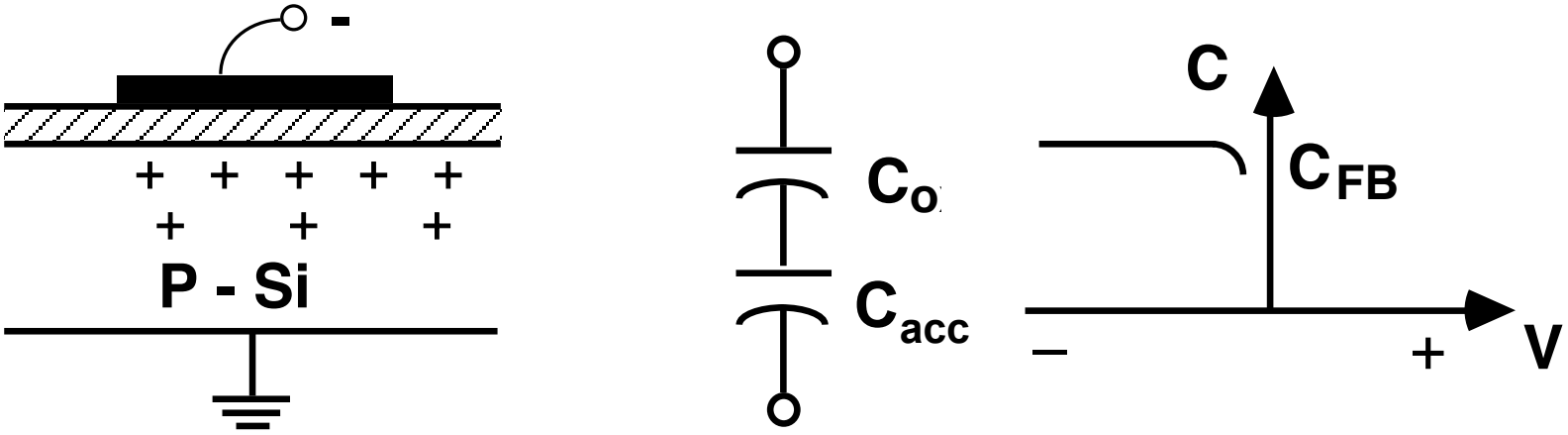


Capacitance is constant with V because in accumulation, the mobile carriers can follow the AC signal.

$$C' \approx C'_o = \frac{K_o \varepsilon_o}{x_o} \qquad (8)$$

where ′ indicates capacitance per unit area

2. Flat Band



At V_{FB} there is no charge in the device, but when a small AC voltage is applied, there will be charge that appears on the average a Debye length from the surface. In other words, the average charge will not appear right underneath the oxide, but at a Debye length away from the oxide. So the capacitance at V_{FB} is a combination of oxide capacitance C_o and Si accumulation capacitance $C_{acc.}$

$$C' = \left(\frac{1}{C'_o} + \frac{1}{C'_{acc}} \right)^{-1}$$

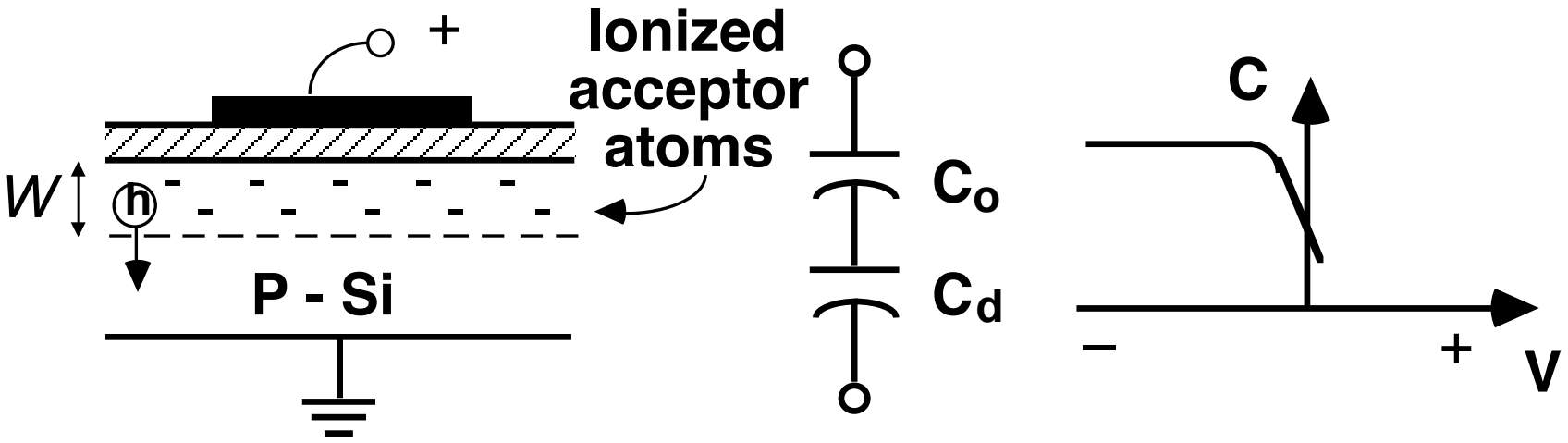
$$= \left(\frac{x_o}{K_o \varepsilon_o} + \frac{L_D}{K_s \varepsilon_o} \right)^{-1} \qquad (9)$$

where,

$$L_D = \sqrt{\frac{K_s \varepsilon_0 kT}{q^2 N_A}}$$

In reality, C_{acc} is present during accumulation also. However, when there are lots of carriers, Debye length decreases, so C_{acc} will increase to nearly infinity, which would cause C to be equal to C_o only.

3. Depletion



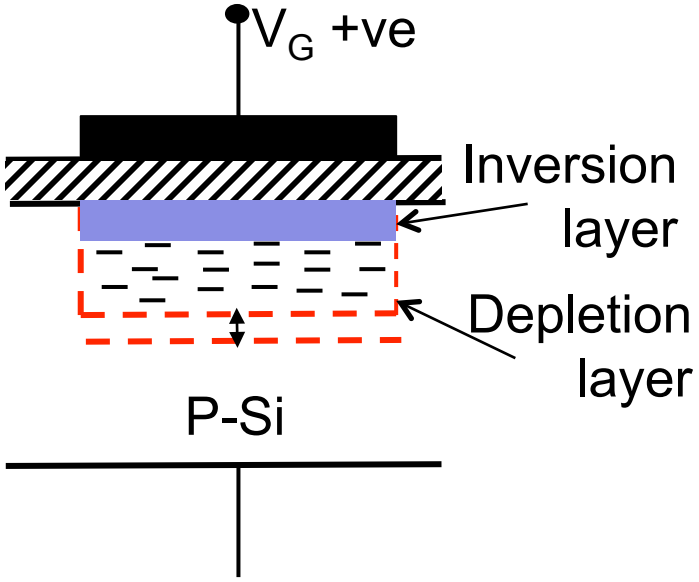
The only charge carriers that can follow the AC signal are at the back edge of the depletion region in the semiconductor.

$$C' = \left(\frac{1}{C'_o} + \frac{1}{C'_d} \right)^{-1} = \left(\frac{x_o}{K_o \varepsilon_o} + \frac{W}{K_s \varepsilon_o} \right)^{-1} \qquad (10)$$

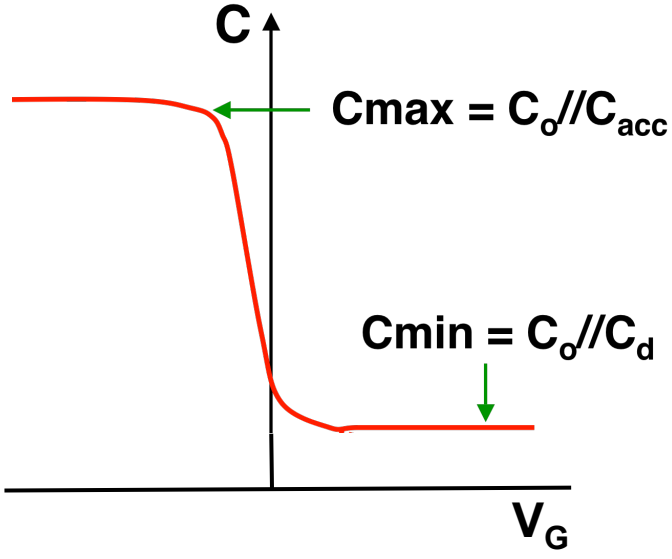
4. Inversion

Three types of response:

1. High measurement frequency with slow DC sweep
2. Rapid DC sweep
3. Low frequency with slow DC sweep



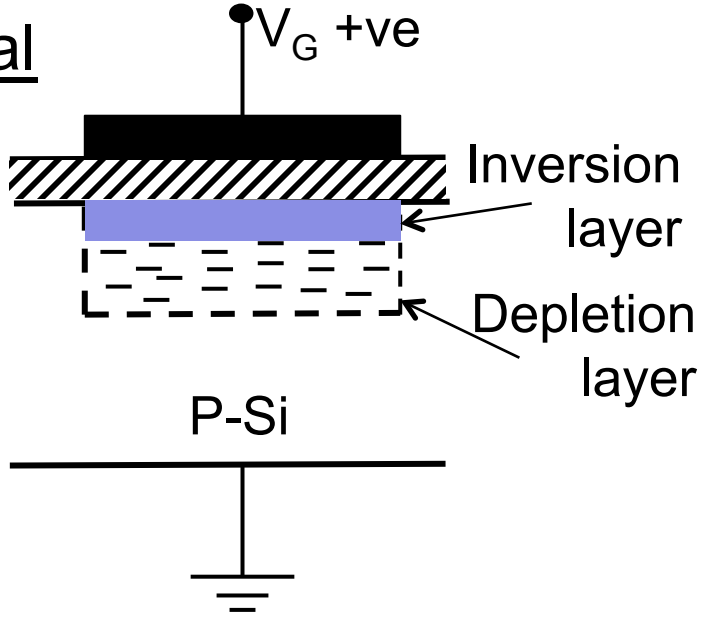
<u>Slow D.C. sweep, high frequency AC signal</u> (f > 1 KHz), mobile carriers at the back edge of the depletion region are modulated because the generation recombination processes can't keep up with the A.C. signal

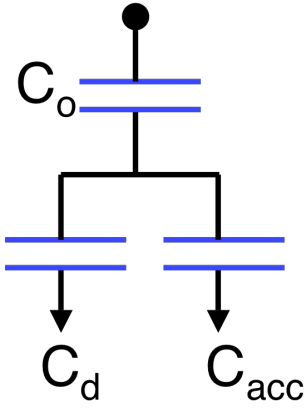


$$C'_{\min} = \left(\frac{1}{C'_o} + \frac{1}{C'_{d_{\min}}} \right)^{-1} = \left(\frac{x_o}{K_o \varepsilon_o} + \frac{W}{K_s \varepsilon_o} \right)^{-1}$$

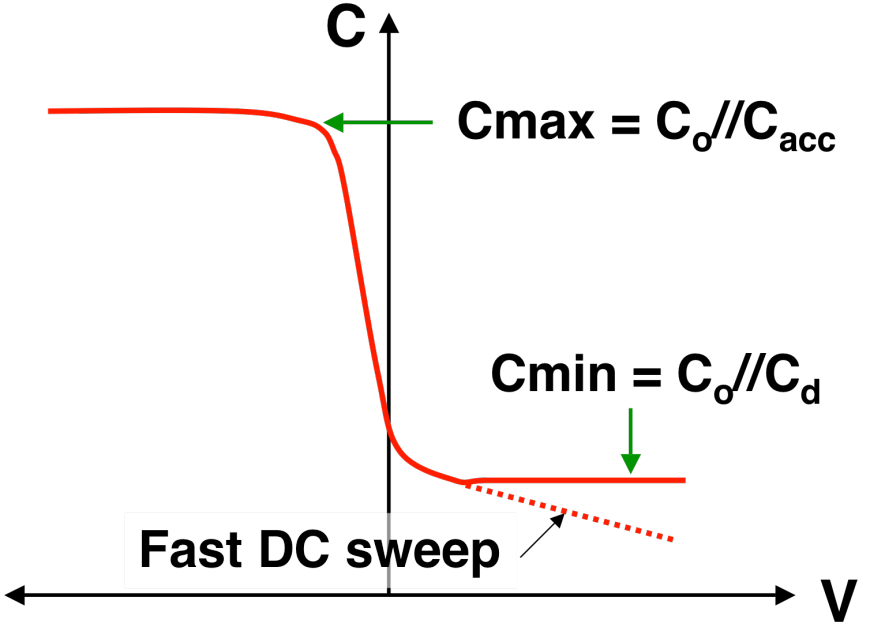
Fast DC sweep, high frequency AC signal

The generation process is too slow to keep up with the change in the DC gate bias. The capacitor goes into deep depletion and equation (10) continues to be valid. Eventually the generation process supplies carriers to the inversion layer and the capacitance returns to the normal high frequency value.



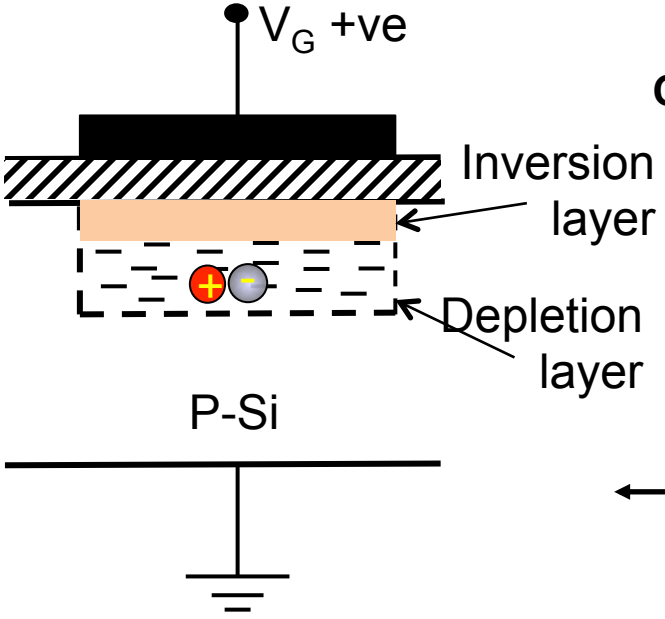


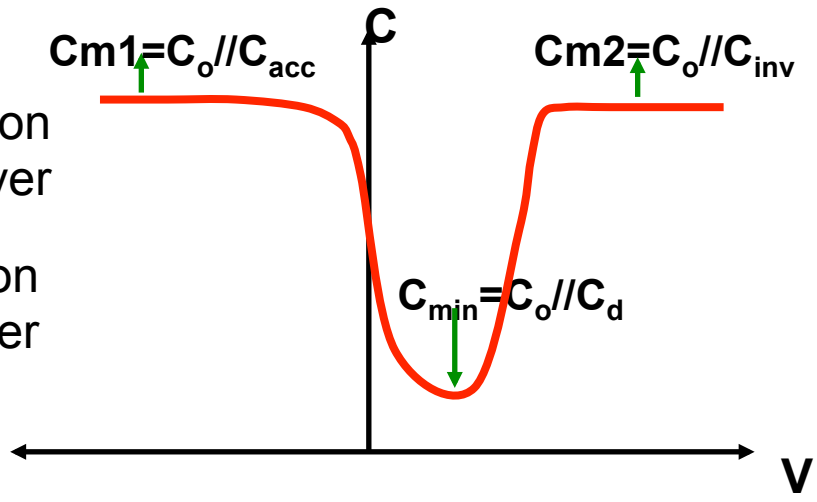
Note that C_d and C_{acc} do not occur simultaneously

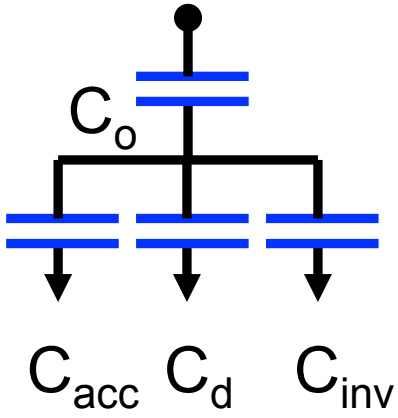


Low Frequency or Quasi-Static C-V

- Measurement is a very slowly ramped (quasi-static) DC input or a Very slow AC frequency superposed on a DC sweep
- Generation recombination processes can keep up with the A.C. s **W**
- Inversion layer (next to oxide) is modulated at AC frequency.
- Charge in the depletion layer is not modulated. C_{dep} does not enter the picture

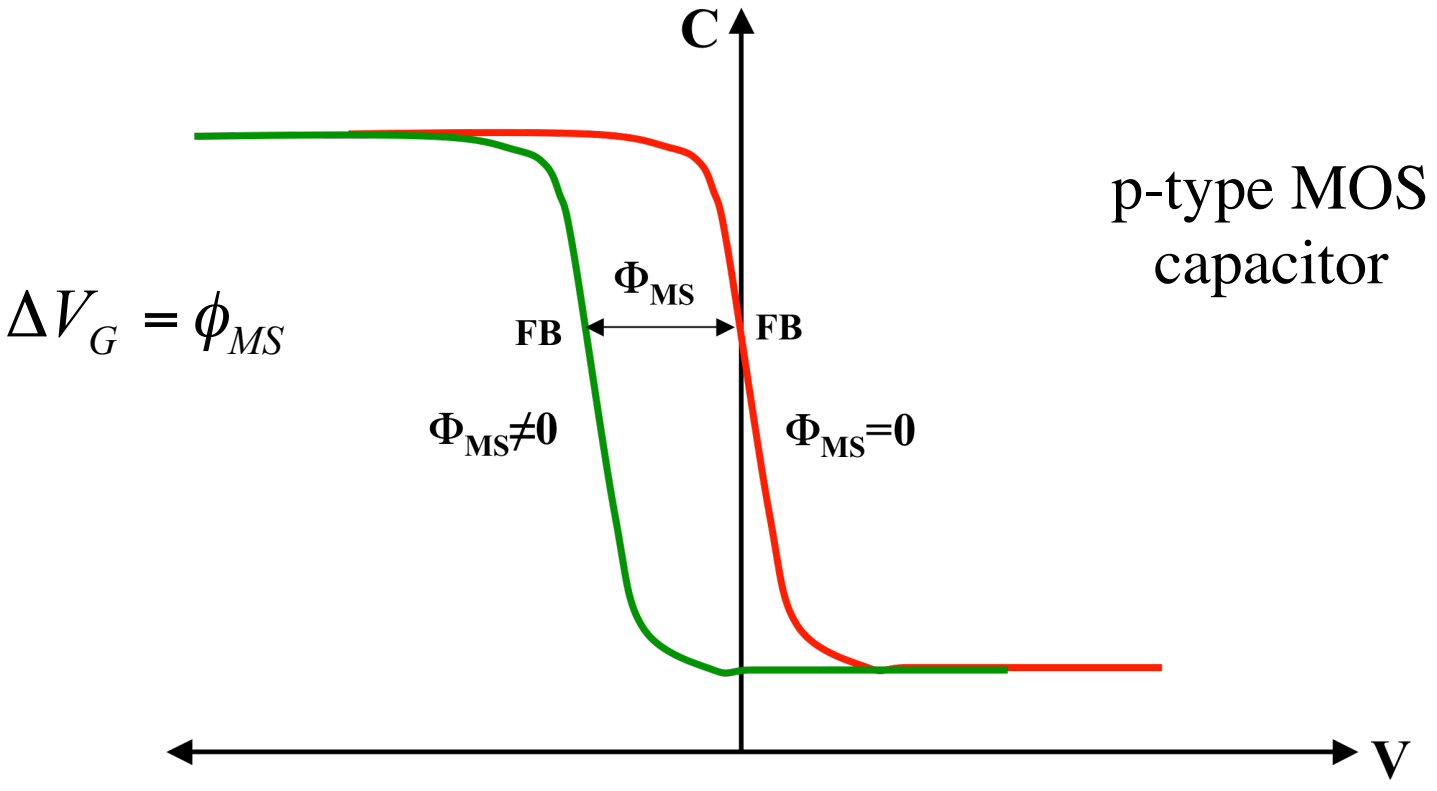






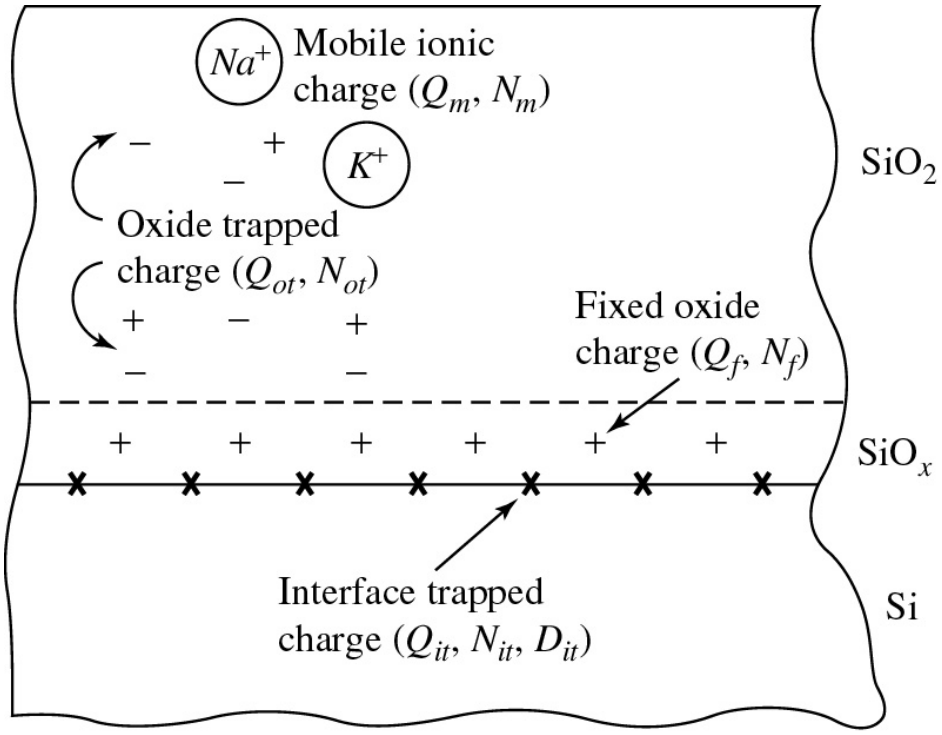
Note that C_d and C_{inv} can occur simultaneously but not with C_{acc}

Flatband Shift due to Work Function Difference

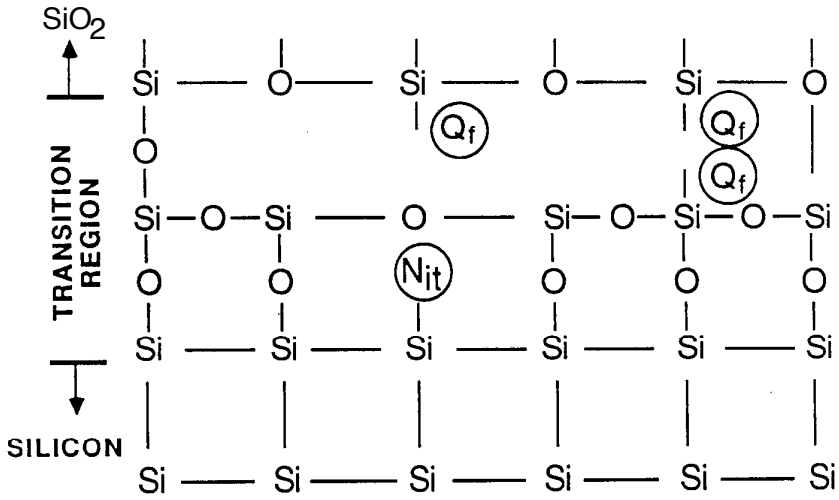


There will be a shift in the C-V curve from the ideal curve due to the differences in the metal-semiconductor work functions. This is generally negative because for most combinations, $\Phi_S > \Phi_M$.

Oxide and Interface Charges



Four categories of oxide charge in the MOS system. The symbols for the charge densities Q (C cm^{-2}), and state densities N (states cm^{-2}) or D (states cm^{-2} eV^{-1}) have been standardized.



Dangling bonds which are not passivated by oxygen give rise to interface energy states and fixed charge

Types and origins of charge:

1. Fixed interface charge, Q_f (Also known as Q_{ss}) Believed to be due to uncompensated silicon-silicon bonds, on the order of 10^{10} cm^{-2}.

2. Interface trapped-charge, Q_{it} Due to unterminated Si bonds, on the order of $10^{10} cm^{-2}$.

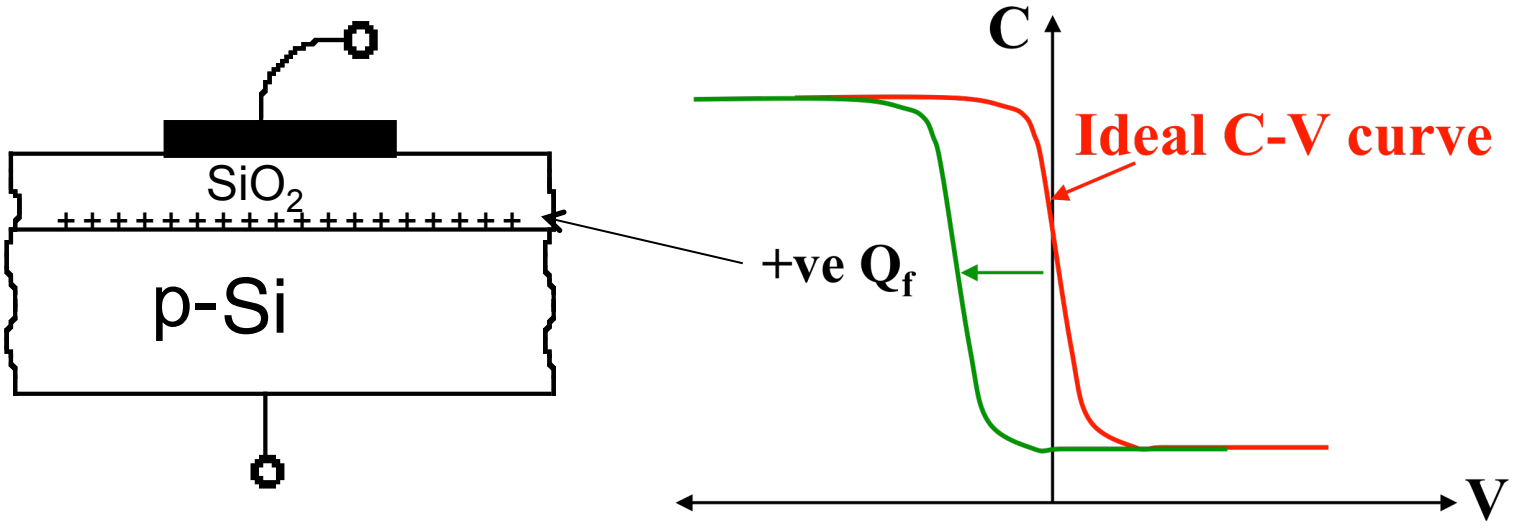
3. Oxide trapped-charge, Q_{ot} Due to defects in the SiO_2 network, usually negligible in today's MOS devices. Can be generated after a large amount of charges have passed through the SiO_2 and broken up the network.

4. Mobile charge Q_m Due to alkaline ions (e.g., Na^+, K^+), usually very low concentration ($\approx 10^9$ cm^{-2}) in today's technology.

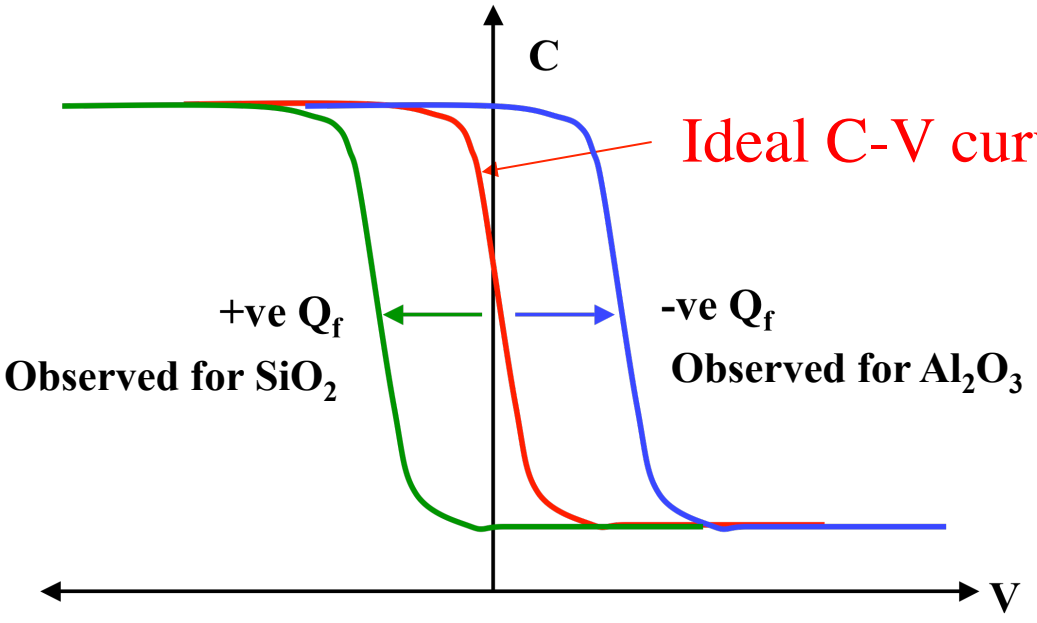
Effects on C-V characteristics:

1. Fixed Charge (Q_f)

For finite Q_f at the interface the flat-band voltage V_{FB} will be different from the theoretical value. This will cause a shift in the C-V curves. By measuring the complete C-V curves and comparing them with the ideal curves the shift will give the value of Q_f.



Fixed charge corresponds to a parallel shift in CV



$$\Delta V_{FB} = \frac{Q_F}{C'_o}$$

$$V_{FB} = \phi_{MS} - \frac{Q_F x_o}{K_o \varepsilon_o} = \phi_{MS} - \frac{Q_F}{C'_o}$$

$$V_T = \phi_{MS} - \frac{Q_F x_o}{K_o \varepsilon_o} + \frac{x_o}{K_o \varepsilon_o}\sqrt{4\varepsilon_s q N_A \phi_F} + 2\phi_F$$

For $x_o = 1000\,\text{Å}$ $\quad Q_F = 10^{11}\,cm^{-2}$ $\quad \Delta V_{FB} = 0.5V$

Effect of Flatband Shift

Negative Φ_{MS} shifts the C-V curve in the negative direction, which at zero bias results in,

1. Inversion layer in p-type material (N-MOS), which produces a channel at zero bias--normally ON

2. Accumulation layer in n-type material (P-MOS), which produces a strong blocking channel at zero bias--normally OFF

The consequences of this were the initial development of P-MOS rather than N-MOS, even though mobility favored N-MOS.

There were additional technological problems (positive charge in the oxide) which would shift the C-V curve similar to the example of negative Φ_{MS}. That favored P-MOS as well.

2. Oxide trapped-charge, Q_{ot}

For an arbitrary distribution of trapped-charge, Q_{ot} within the oxide. (For details see Mueller and Kamins)

$$\Delta V_{FB} = -\frac{1}{K_o \varepsilon_0}\int_0^{x_o} \rho(x) x dx$$

$$= -\frac{x_o}{K_o \varepsilon_o}\int_o^{x_o} \rho(x)\frac{x}{x_o} dx$$

$$= -\frac{Q_F}{C'_o} - \frac{1}{C'_o}\int_o^{x_o} Q_{ot}(x)\frac{x}{x_o} dx$$

Important for

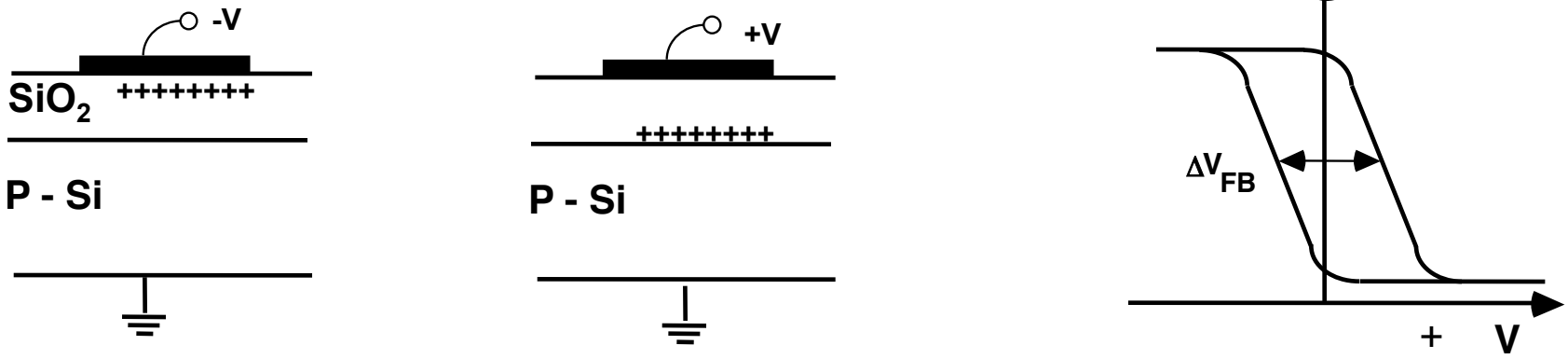
DoD applications (radiation hardness).

Flash memories

Hot carrier degradation of MOSFETs

3. Mobile Charge (Q_m)

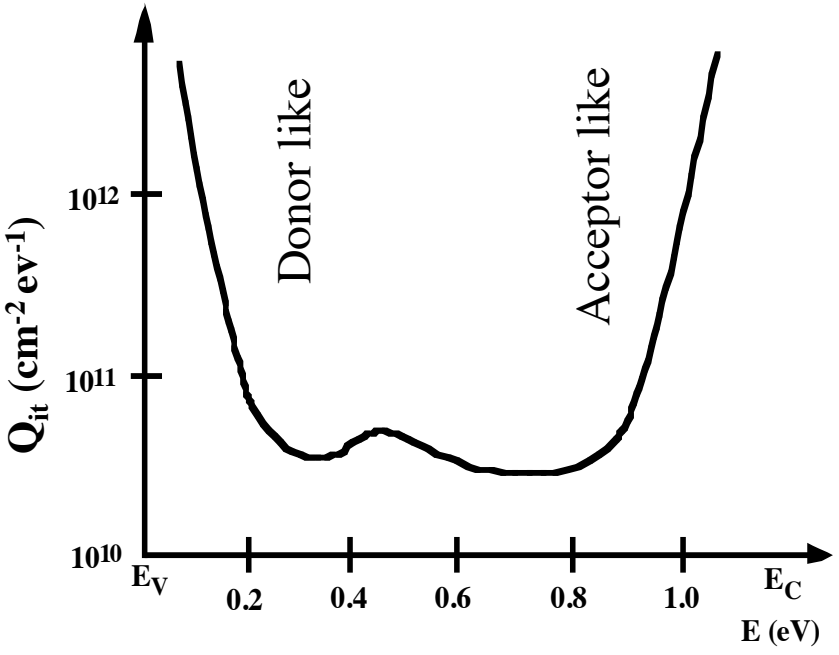
By bias-temperature stress, Q_m can be moved from the SiO_2-Si interface to the metal-SiO_2 interface. The wafer is heated at ~300°C and a small positive or negative gate bias, V_G of 5-10 V, is applied to move the mobile charge to the metal-SiO_2 interface (next to gate) or to the SiO_2 -Si interface (pos to gate). The shift in V_{FB} indicates that there is mobile charge and the magnitude of the shift can be used to estimate Q_m.

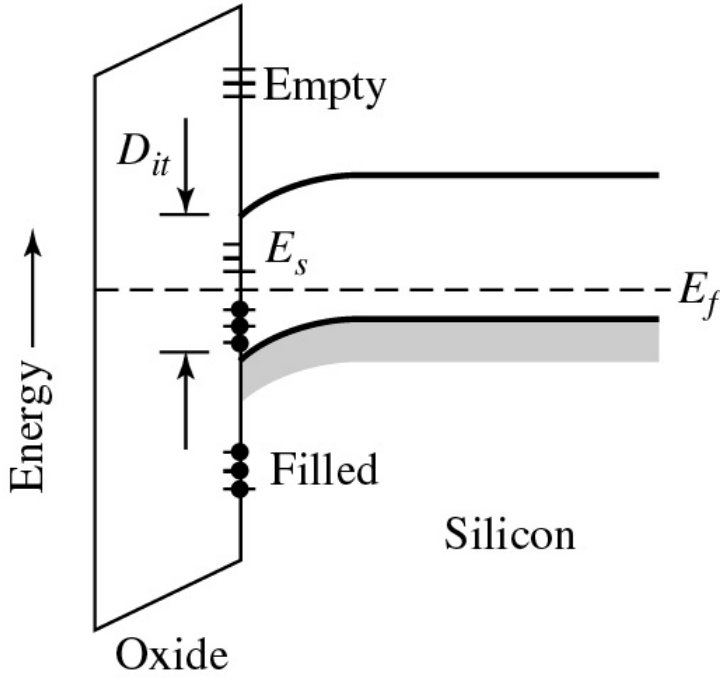


For 100Å SiO_2 1ppm N_A^+ (10^{16} cm^{-3}) $\Rightarrow Q_m = 10^{11}/cm^2$, $\Delta V_{FB} = 0.05V$
without great care, it is easy to have $>10^{13}$ ions, $\Rightarrow \Delta V_{FB} > 5V$!!!

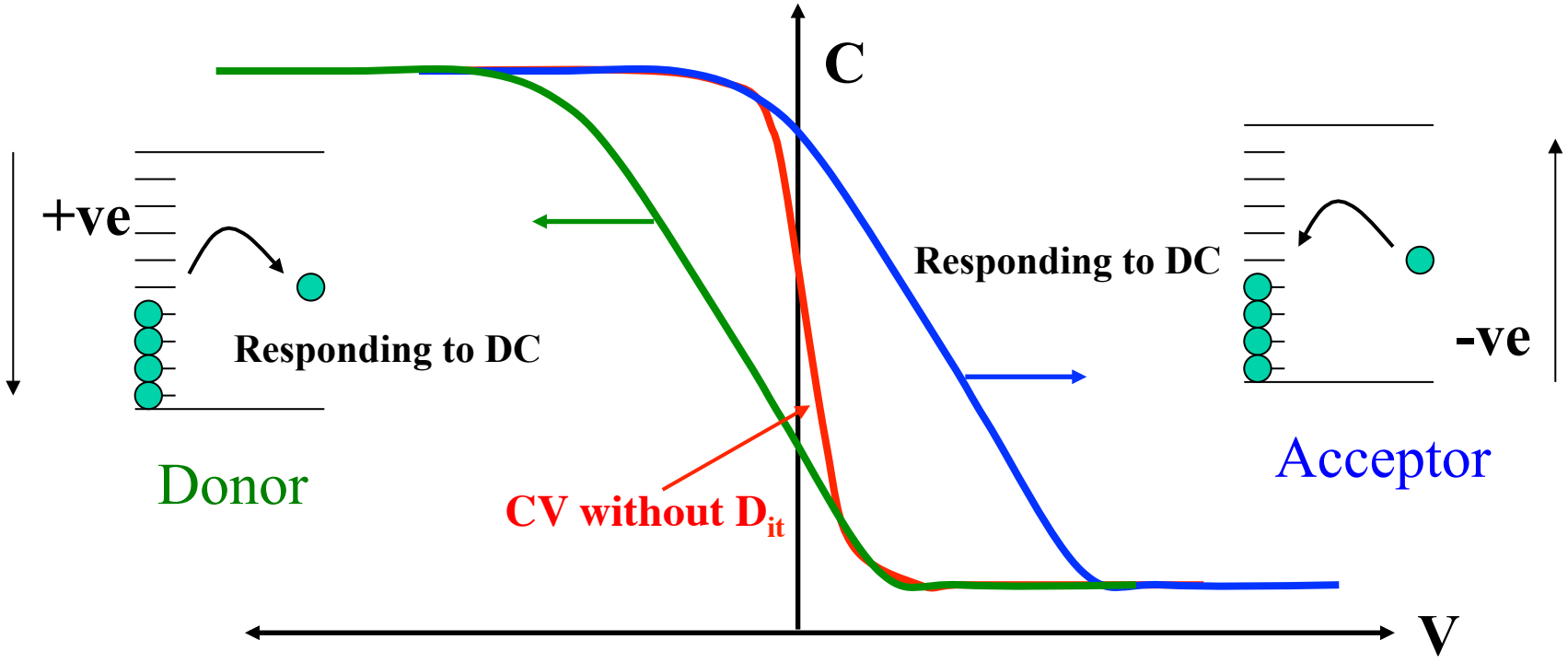
Interface Traps (Q_{it})

Interface traps are very similar to the traps in a Schottky diode which pin the Fermi level at mid-gap, these interface traps have energy levels distributed in the band gap with density D_{it} or Q_{it} (# of states cm^{-2} eV^{-1}). The charge state (occupancy) of the traps depends on the Fermi level.



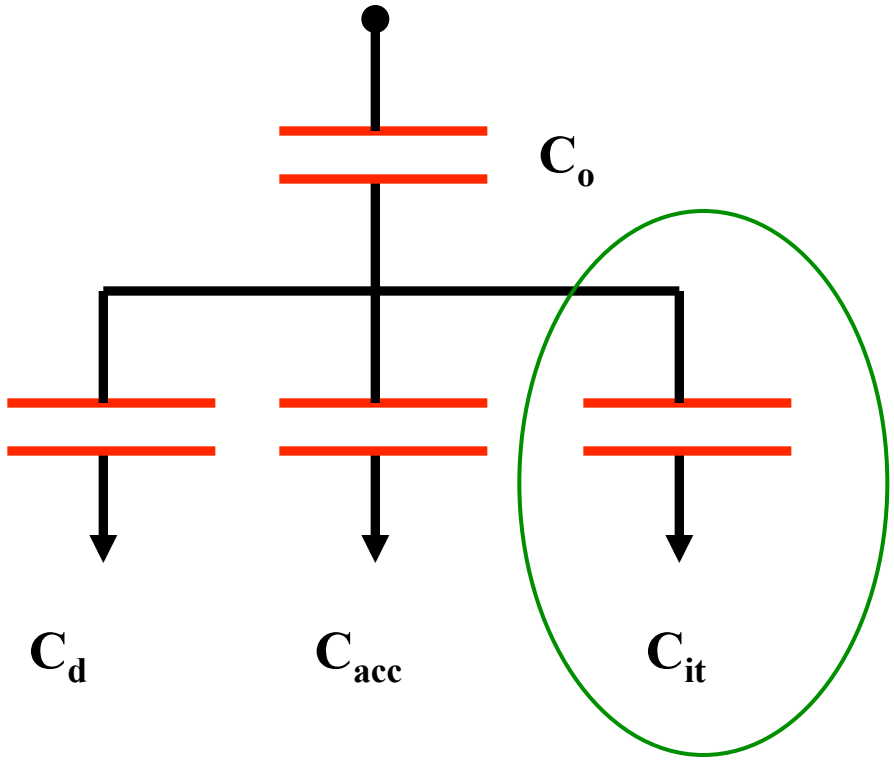


Effect of Interface Traps on High-Frequency C-V



- As the surface potential is swept from flat band towards depletion, the traps will try to pin the surface potential, i.e., it will take more gate voltage to move the surface potential through the traps.
  - Donor type traps are charged +ve when empty and neutral when full
  - Acceptor type traps are charged –ve when full and neutral when empty
- Very high frequency cannot modulate interface states. So, the C-V behaves like a V_t shift caused by the charged interface states responding to the slow DC sweep.

CV with D_{it} (Capacitance Model)



Since the interface states respond to the lower frequencies, we need to consider effect of C_{it} as well for lower frequency C-V.

Q_{IT} can be estimated by comparing the difference between the high-frequency C-V (when the traps cannot keep up with the high frequency AC signal) and the low-frequency C-V. In practice a slowly varying ramp is applied to the MOS capacitor and the resulting current is measured. For an ideal capacitor the capacitance is,

$$C = \frac{dQ}{dV} = \frac{dQ}{d(Kt)} = \frac{dQ/dt}{K} = \frac{I(t)}{K}$$

Where K is a constant giving rate of change of V. If there were no interface traps C should be constant and thus the current *I(t)* should be constant. However, if there are traps present they can trap or release the charges as the capacitor goes from accumulation to inversion. This generation - recombination current caused by the interface traps will change the capacitance.

$$C(t) = \frac{I(t) + I(N_{IT})}{K}$$

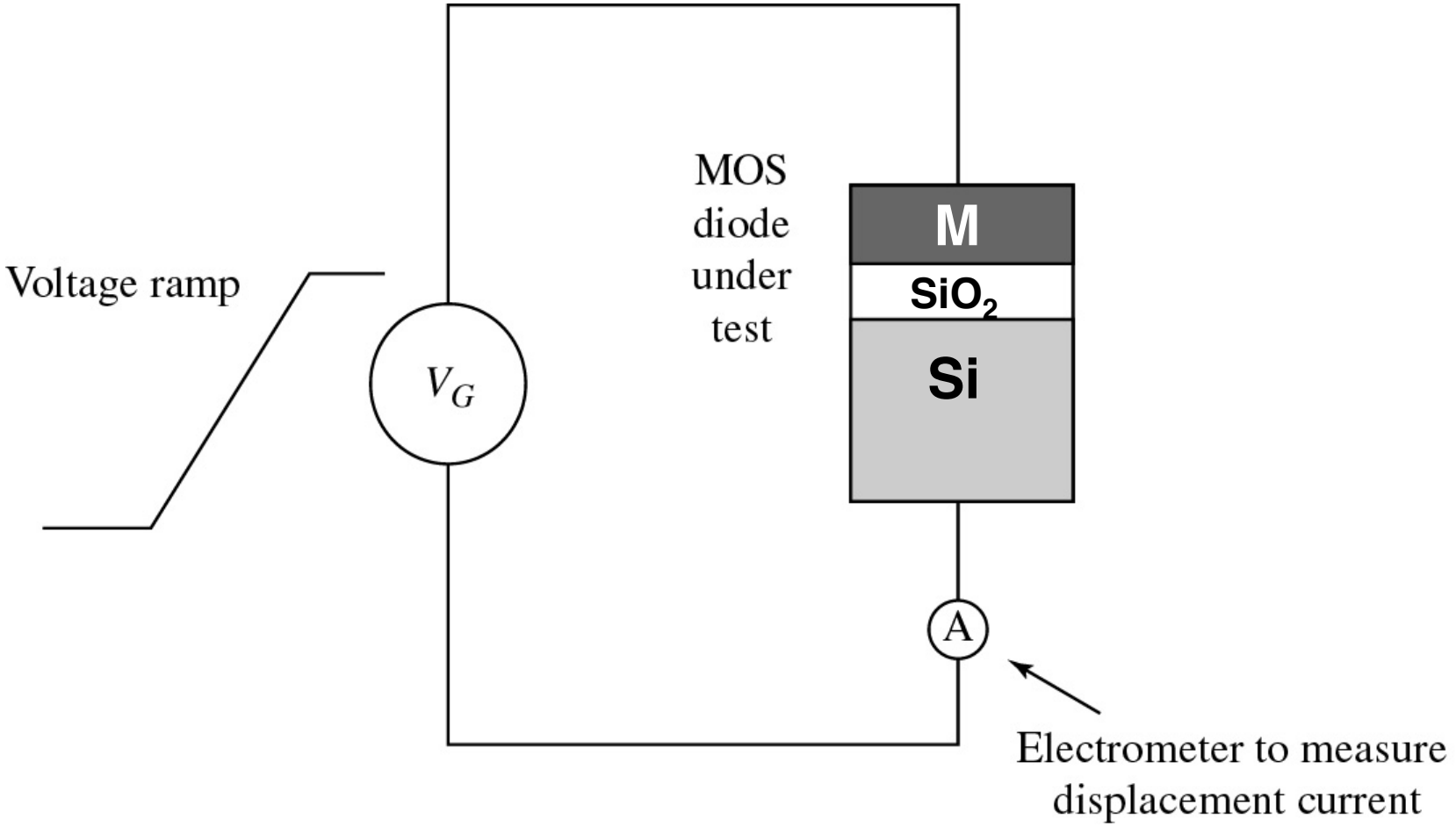
a measure of $I(N_{IT})$ can give the value of N_{IT}

Applications of MOS Capacitors?

A good chunk of electronics industry is spawned by MOS capacitor:

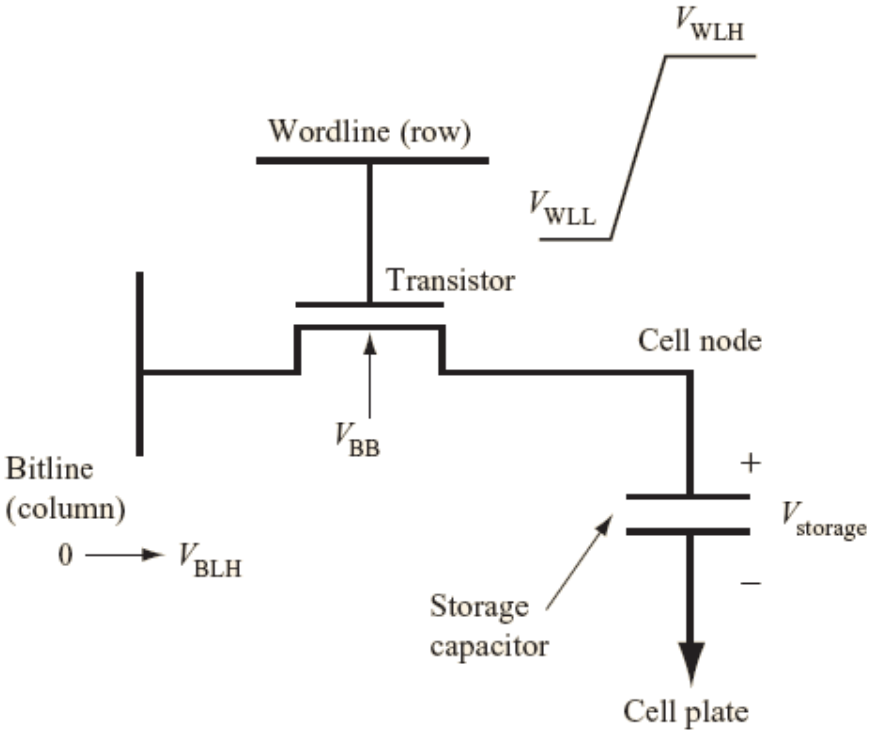
- ✓ With 2 p-n junctions added it makes a MOS transistor
- ✓ Heart of DRAM
- ✓ CCD imagers
- ✓ Analog to digital converters

Quasi-static *C-V* measurement apparatus used to obtain low-frequency *C-V* characteristics

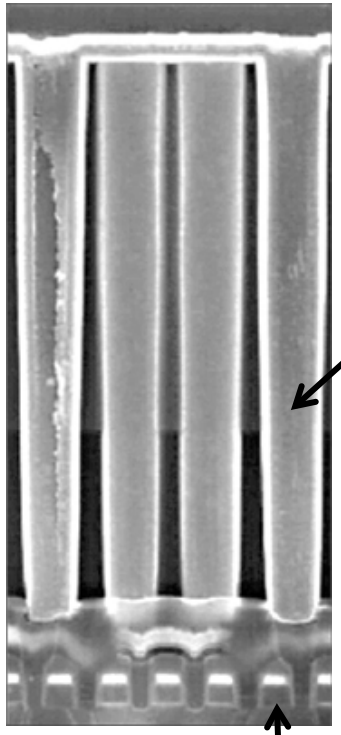


Dynamic Random Access Memory (DRAM)

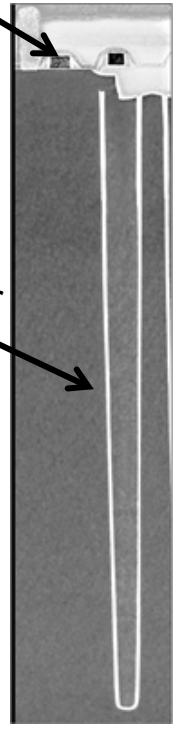
DRAM with one transistor and one capacitor. Charge is stored on the capacitor and sensed by the transistor. Binary data is represented by the presence or absence of the charge.



DRAM: Stacked Capacitor

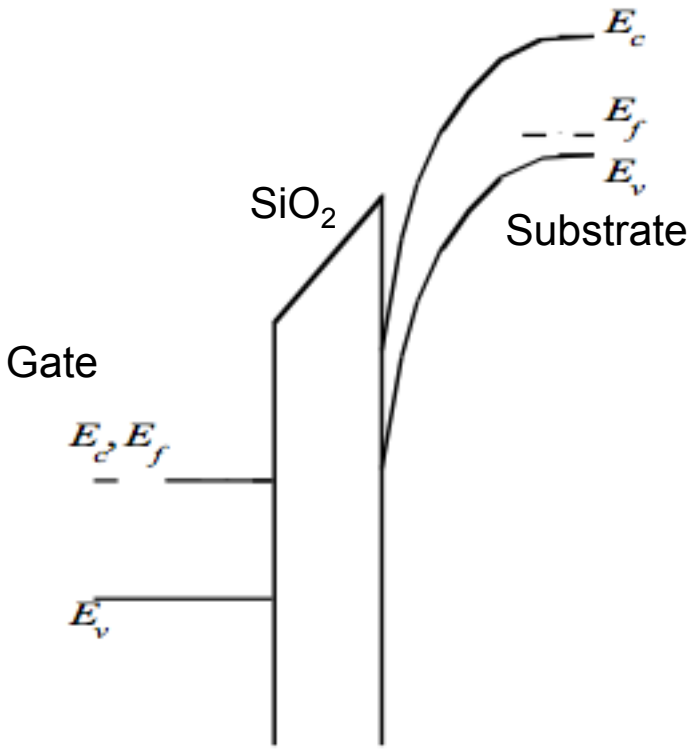


DRAM: Trenched Capacitor

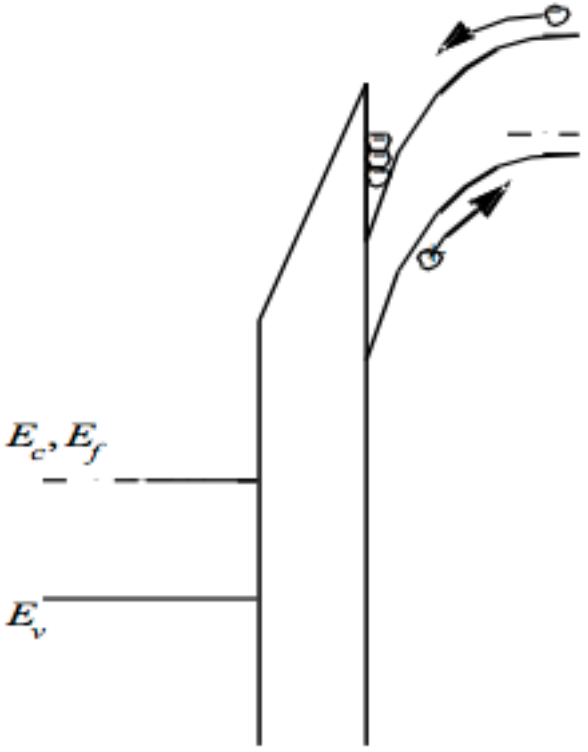


CCD Imager

Extensively used in digital cameras, imagers, etc.

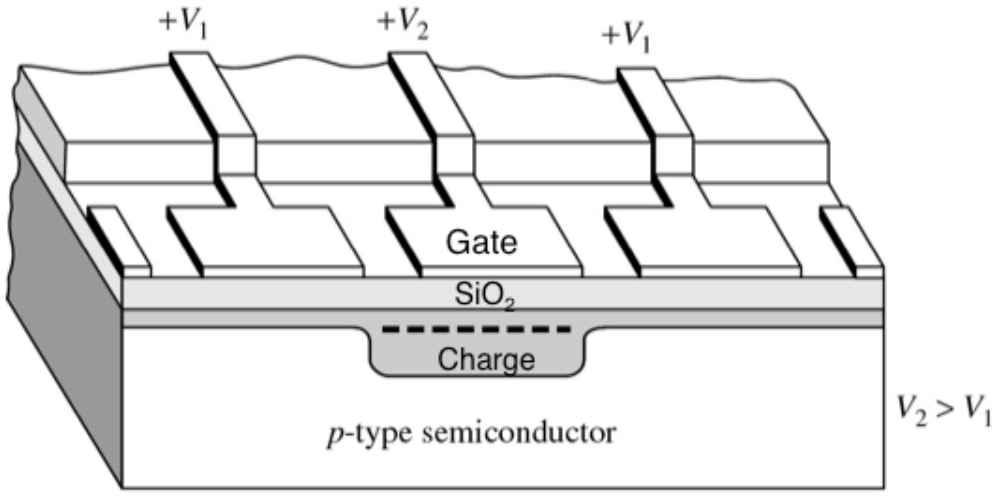


Deep depletion, Q_{inv}= 0

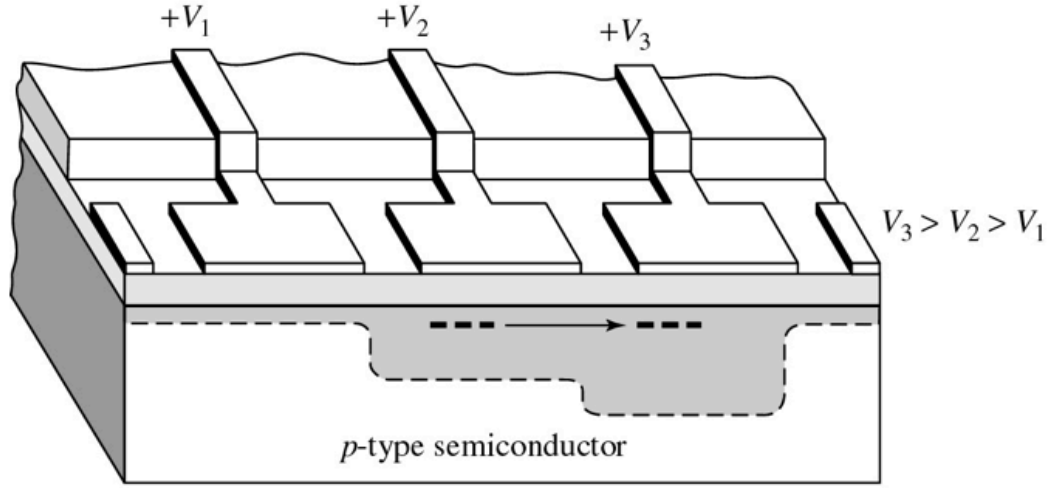


Exposed to light

Charge Coupled Device (CCD)



(a) Storage mode



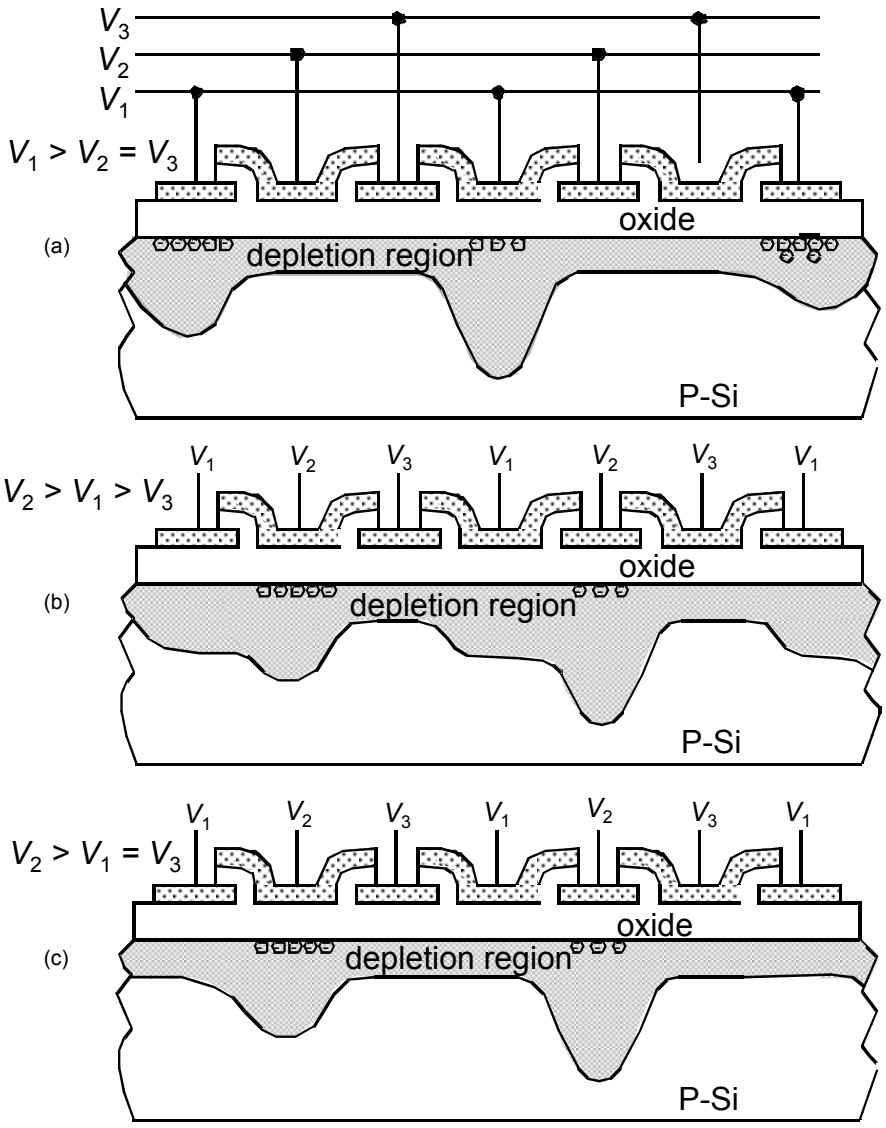
(b) Transfer mode

Basic transfer mechanism in an CCD.

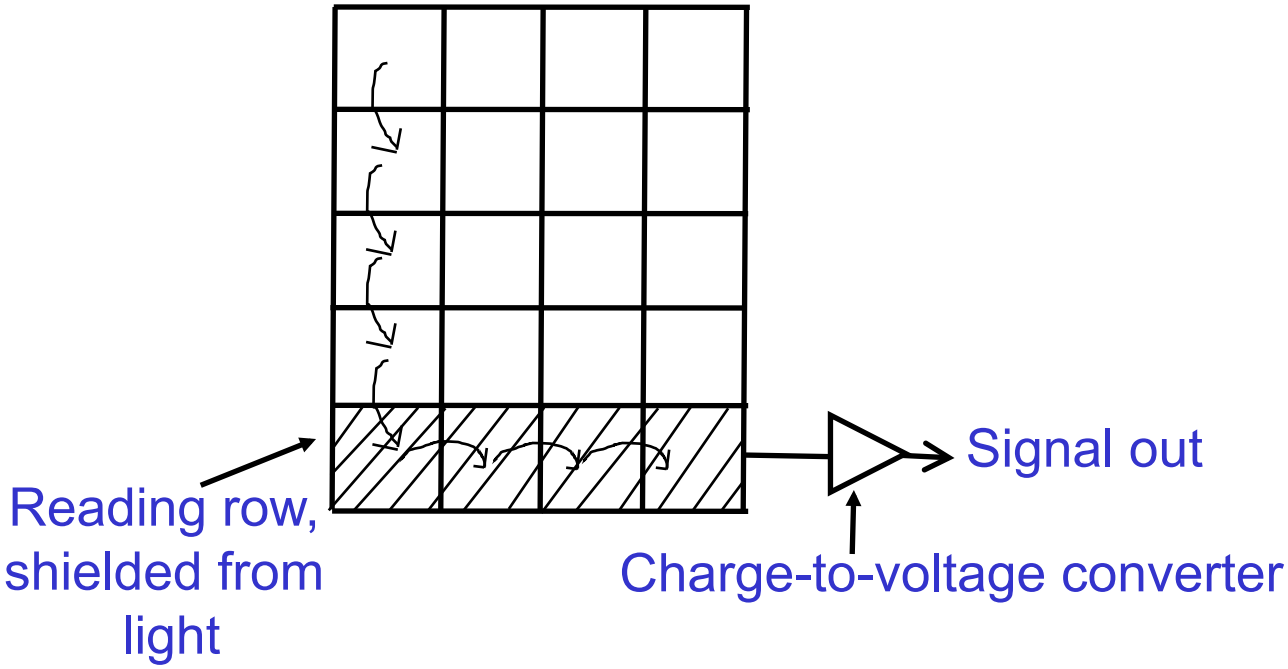
(a) In the storage mode, charge is held under the center gate, which has a channel beneath it.

(b) Application of $V_3 > V_2$ on the right-hand gate causes transfer of charge to the right.

CCD Charge Transfer

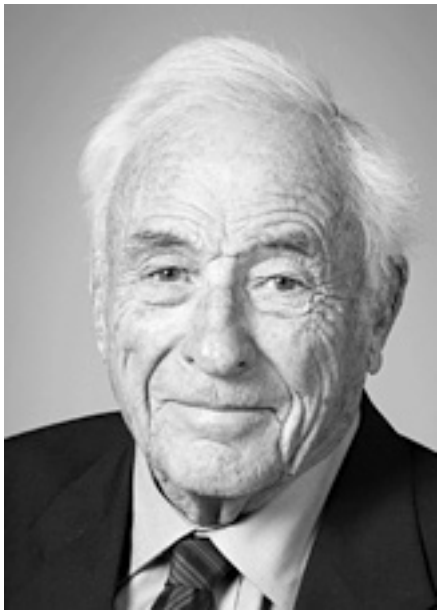


two-dimensional CCD imager



The reading row is shielded from the light by a metal film. The 2-D charge packets are read row by row.

Inventors of CCD Imagers



Willard S. Boyle

George E. Smith

Both of Bell Laboratories, received Physics Noble Prize in 2009 "*for the invention of an imaging semiconductor circuit – the CCD sensor*"

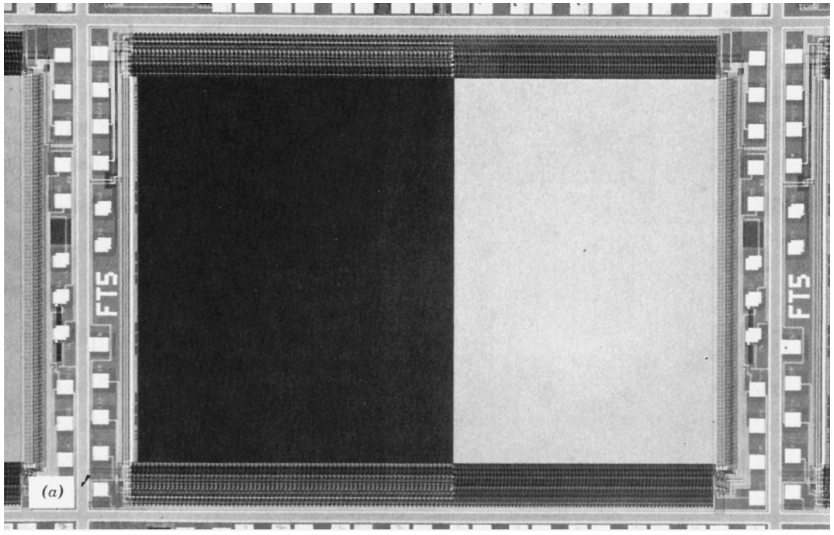
CCD Imager Chip

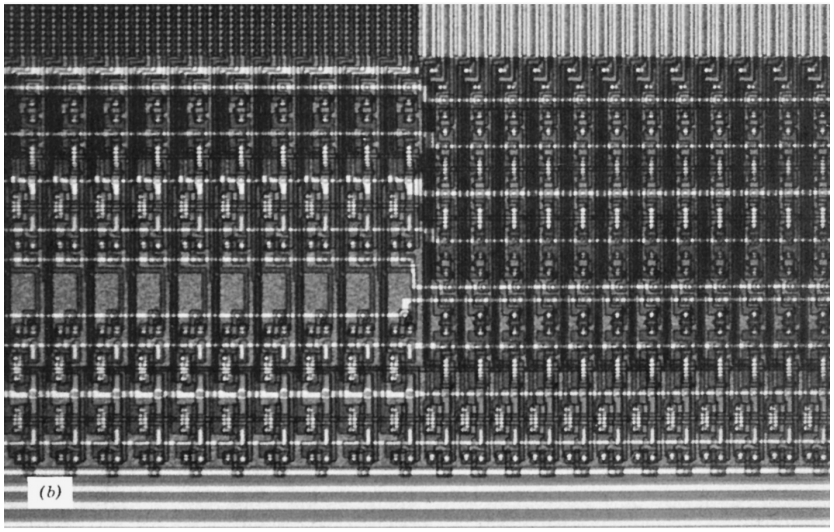
CCDs are extensively used in imaging applications, such as, digital camera, scanner, etc. An example is shown here:

a) A high-density frame-transfer CCD. The sensor array is on the left side of the chip and the light-shielded storage area is on the right. This CCD has 588 lines of 604 pixels each. The chip area is 38.22 mm^2.

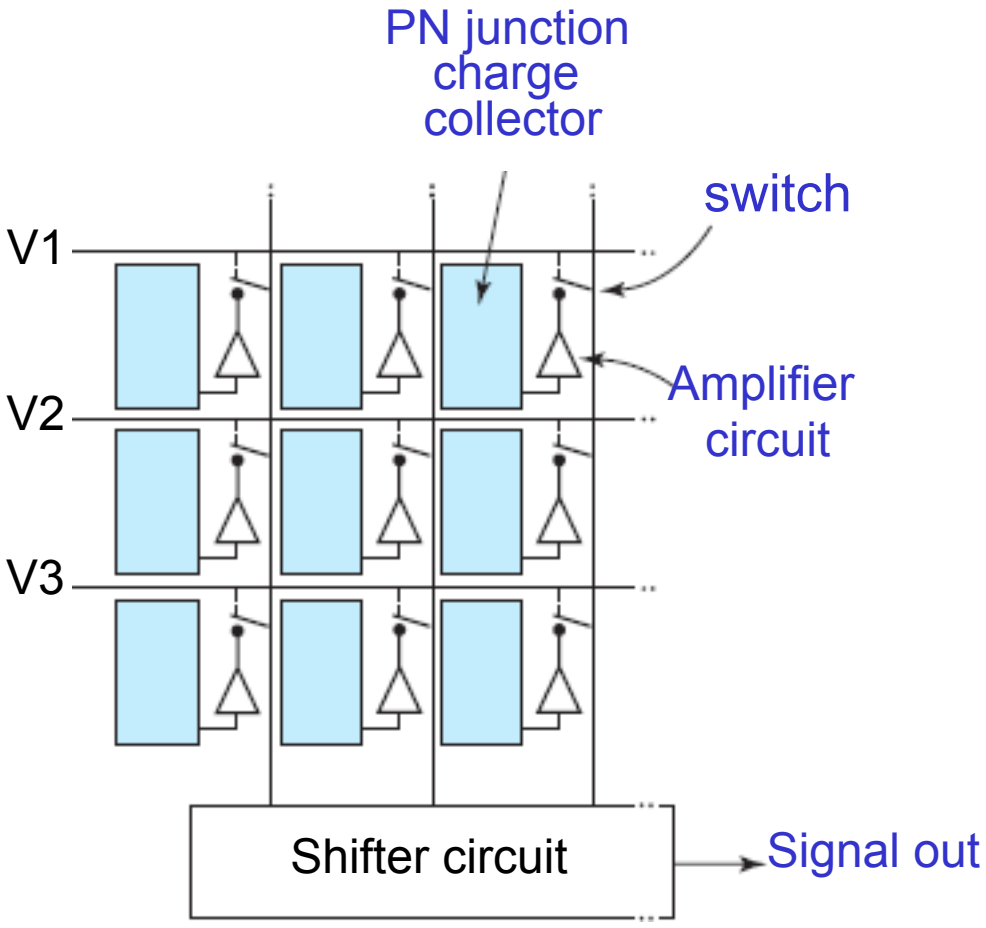
b) Peripheral CMOS circuitry for the CCD.

CCD with millions of pixels are commonly used in digital cameras today





CMOS Imager



CMOS imagers can be integrated with signal processing and control circuitries to further reduce system costs. However, The size constrain of the sensing circuits forces the CMOS imager to use very simple circuits

Higher end digital cameras use CMOS imagers

Analog to Digital Conversion

Integrated circuit for the conversion of analog signals to a digital representation (A to D). The circuit makes use of many precision MOS capacitors with different values of C. These capacitors work as a reference for comparison with the incoming analog signal digitized.