Impurity Doping

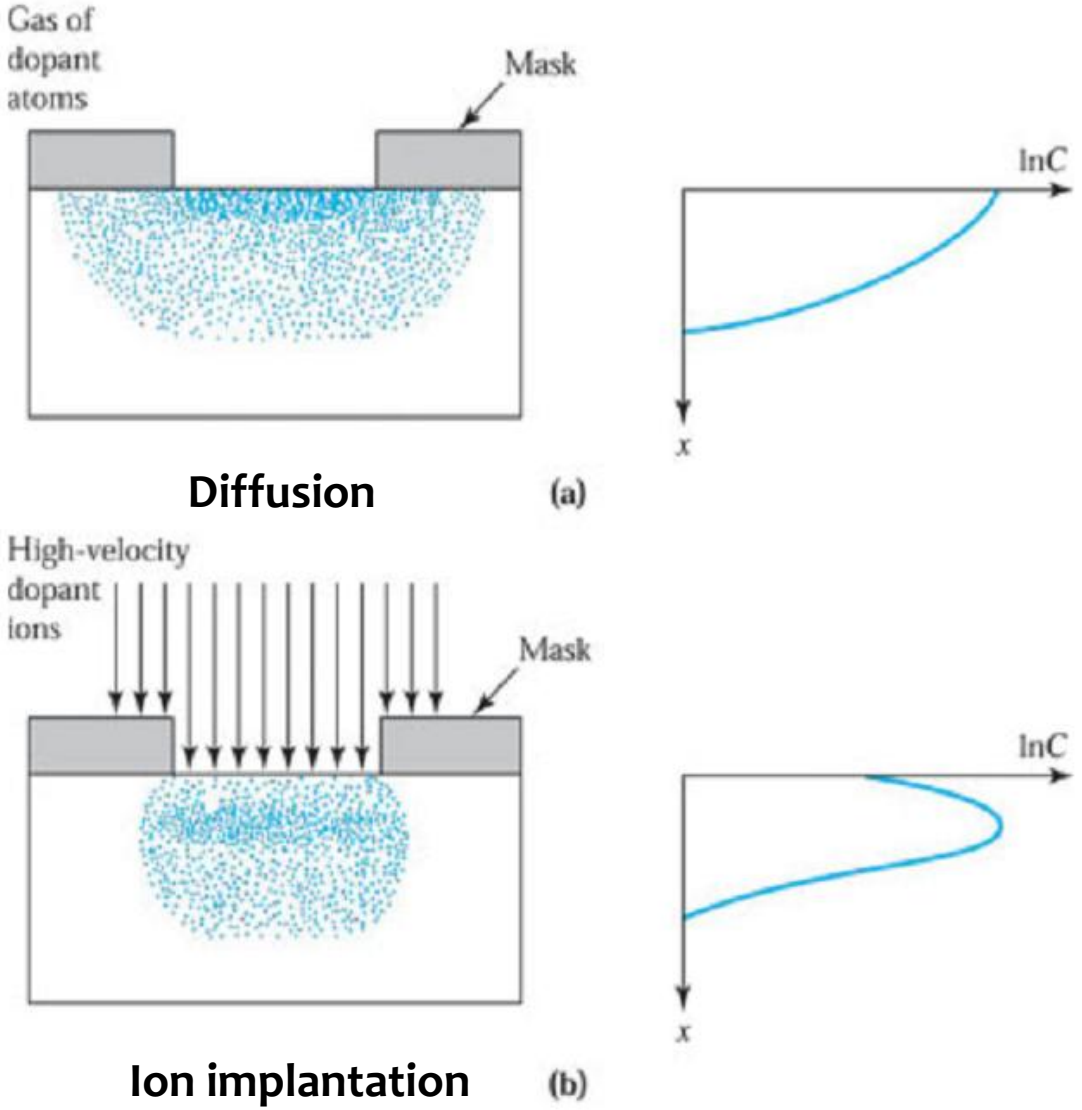
Semiconductor Devices – Physics and Technology

Chapter 14

Introduction

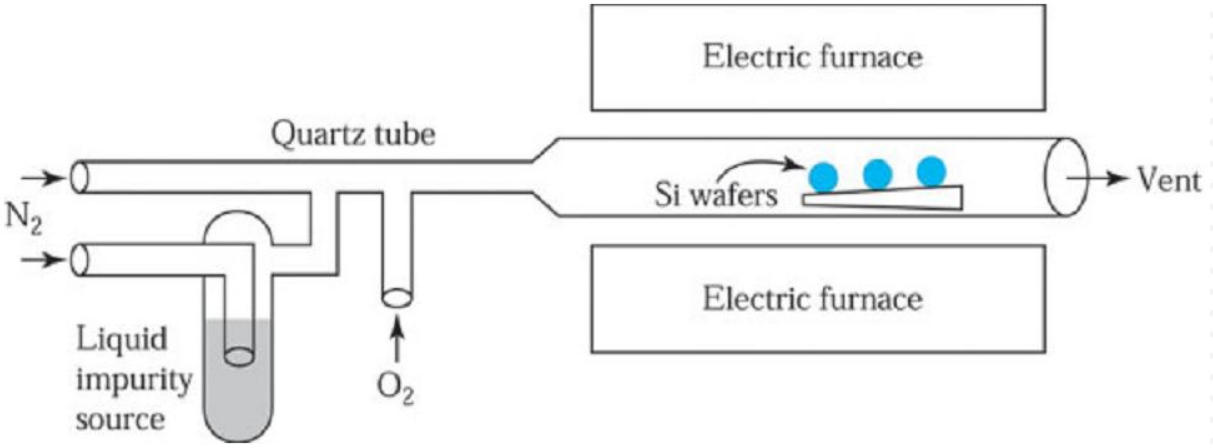
- Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials
- The practical use of impurity doping is primarily to change the electrical properties of the semiconductors
- Diffusion and ion implantation are the two key methods of impurity doping
  - In diffusion the dopant atoms are placed on or near the surface of the wafer by deposition from the gas phase of the dopant or by using doped-oxide sources. The doping concentration decreases monotonically from the surface, and the profile of the dopant distribution is determined mainly by the temperature and diffusion time
  - In ion implantation the dopant ions are implanted into the semiconductor by means of an ion beam. The doping concentration has a peak distribution inside the semiconductor and the profile of the dopant distribution is determined mainly by the ion mass and the implanted-ion energy.

Diffusion versus Ion Implantation Techniques



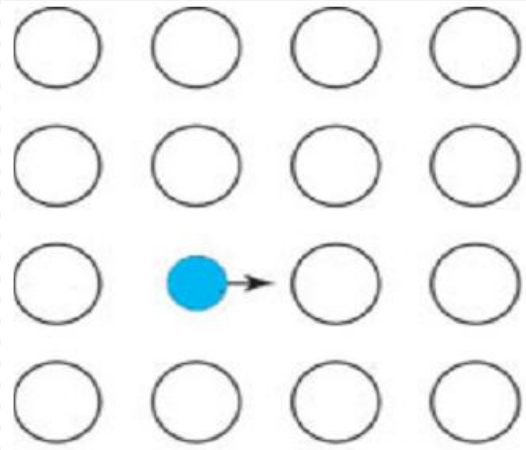
Basic Diffusion Process

- Diffusion of impurities is typically done by placing semiconductor wafers in a carefully controlled high-temperature quartz-tube furnace and passing a gas mixture that contains the desired dopant through it
- The temperature usually ranges between 800° and 1200°C
- For diffusion in silicon, boron is the most popular dopant for introducing a *p*-type impurity, whereas arsenic and phosphorus are used extensively as *n*-type dopants
- Figure shows a typical open-tube diffusion system

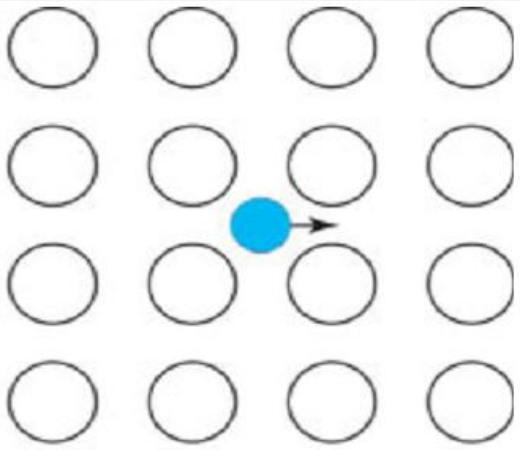


Diffusion Types

- Diffusion in a semiconductor can be visualized as atomic movement of the diffusant (dopant atoms) in the crystal lattice by vacancies or interstitials
- Figure shows the two basic atomic-diffusion models in a solid
- The open circles represent the host atoms occupying the equilibrium lattice positions and the solid dots represent impurity atoms



Vacancy mechanism



Interstitial mechanism

Diffusion Types (2)

- At elevated temperatures the lattice atoms vibrate around the equilibrium lattice sites
- There is a finite probability that a host atom acquires sufficient energy to leave the lattice site and become an interstitial atom, thereby creating a vacancy
- When a neighboring impurity atom migrates to the vacancy site, the mechanism is called vacancy diffusion
- If an interstitial atom moves from one place to another without occupying a lattice site, the mechanism is interstitial diffusion
- An atom smaller than the host atom often moves interstitially

Diffusion Equation

- The basic diffusion process of impurity atoms is similar to that of charge curriers (electrons and holes)
- We define a flux *F* as the number of dopant atoms passing through a unit area in a unit time and C as the dopant concentration per unit volume

$$F = -D\frac{\partial C}{\partial x},$$

where D is the diffusion coefficient or diffusivity

- The flux is proportional to the concentration gradient, and the dopant atoms will move (diffuse) away from a high-concentration region toward a lower-concentration region
- We can substitute this equation into the one-dimensional continuity equation under the condition that no materials are formed or consumed in the host semiconductor

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right)$$

Diffusion Equation

- When the concentration of the dopant atoms is low, the diffusion coefficient can be considered independent of doping concentration and the last equations becomes

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}.$$ (Flick's diffusion equation)

- The diffusion coefficients can be expressed as

$$D = D_0 \exp(\frac{-E_a}{kT}),$$

where T is the temperature, D_o is the diffusion coefficient in cm^2/s extrapolated to infinite temperature, and E_a is the activation energy eV

- For interstitial diffusion E_a is found to be between 0.5 and 2 eV, and between 3 and 5 eV for vacancy diffusion

Diffusion Profiles

- The diffusion profile of the dopant atoms is dependent on the initial and boundary conditions
- We will consider two important cases:
  - Constant-surface-concentration diffusion: Impurity atoms are transported from a vapor source onto the semiconductor surface and diffuse into the semiconductor wafers. The vapor source maintains a constant level of surface concentration during the entire diffusion period
  - Constant-total-dopant diffusion: A fixed amount of dopant is deposited onto the semiconductor surface and is subsequently diffused into the wafers

Constant-Surface-Concentration Diffusion

- The initial condition at time $t=0$ is

$$C(x,0) = 0,$$

which states that the dopant concentration in the host semiconductor is initially zero

- The boundary conditions are

$$C(0,t) = C_s,$$

$$C(\infty,t) = 0,$$

where C_s is the surface concentration (at $x = 0$), which is independent of time

- The second boundary condition states that at large distances from the surface there are no impurity atoms

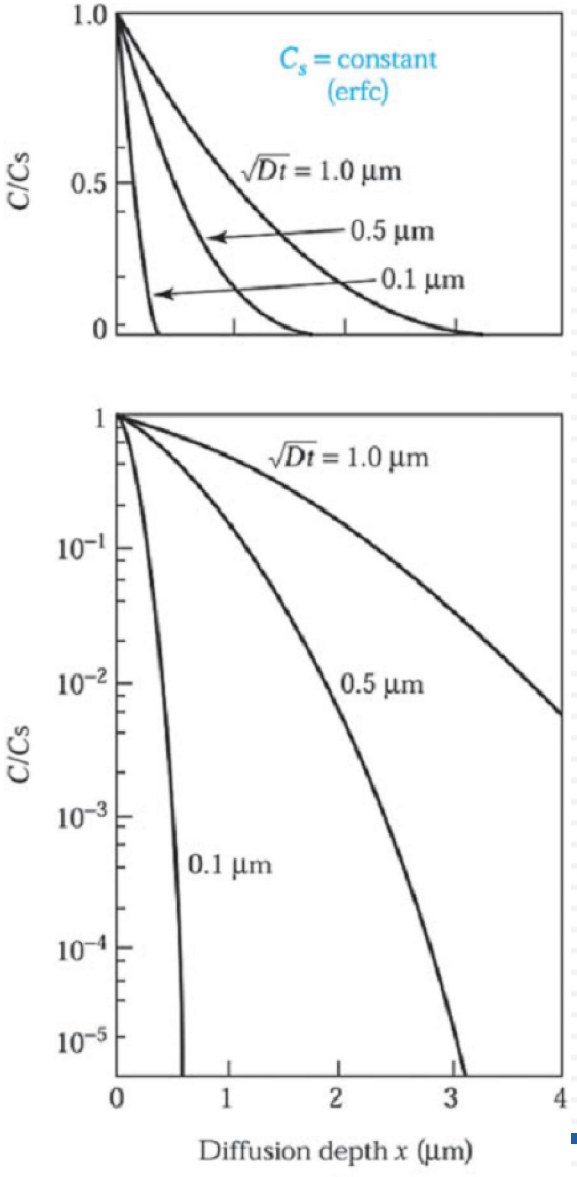
Constant-Surface-Concentration Diffusion (2)

- The solution of the diffusion equation that satisfies the initial and boundary conditions is given by

$$C(x,t) = C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right),$$

where *erfc* is the complementary error function and Dt is the diffusion length

- The diffusion profile for the constant-surface concentration condition is shown in Figure
- Note that as the time progresses, the dopant penetrates deeper into the semiconductor



Constant-Surface-Concentration Diffusion (3)

- The total number of dopant atoms per unit area of the semiconductor is given by

$$Q(t) = \int_0^\infty C(x,t)dx$$

$$Q(t) = \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt} \cong 1.13 C_s \sqrt{Dt}$$

- This expression can be interpreted as that the quantity $Q(t)$ represents the area under one of the diffusion profiles of the linear plot in the previous Figure
- These profiles can be approximated by triangles with height C_s and base $2\sqrt{Dt}$
- A related quantity is the gradient of the diffusion profile dC/dx

$$\left.\frac{dC}{dx}\right|_{x,t} = -\frac{C_s}{\sqrt{\pi Dt}} e^{-x^2/4Dt}$$

Constant–Total-Dopant Diffusion

- For this case, a fixed (or constant) amount of dopant is deposited onto the semiconductor surface in a thin layer and the dopant subsequently diffuses into the semiconductor
- The initial condition is $C(x,0) = 0$,
- The boundary conditions are

$$\int_0^\infty C(x,t)dx = S \quad , \quad C(\infty, t) = 0$$

where S is the total amount of dopant per unit area

- The solution of the diffusion equation that satisfies the initial and boundary conditions is a Gaussian distribution

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right).$$

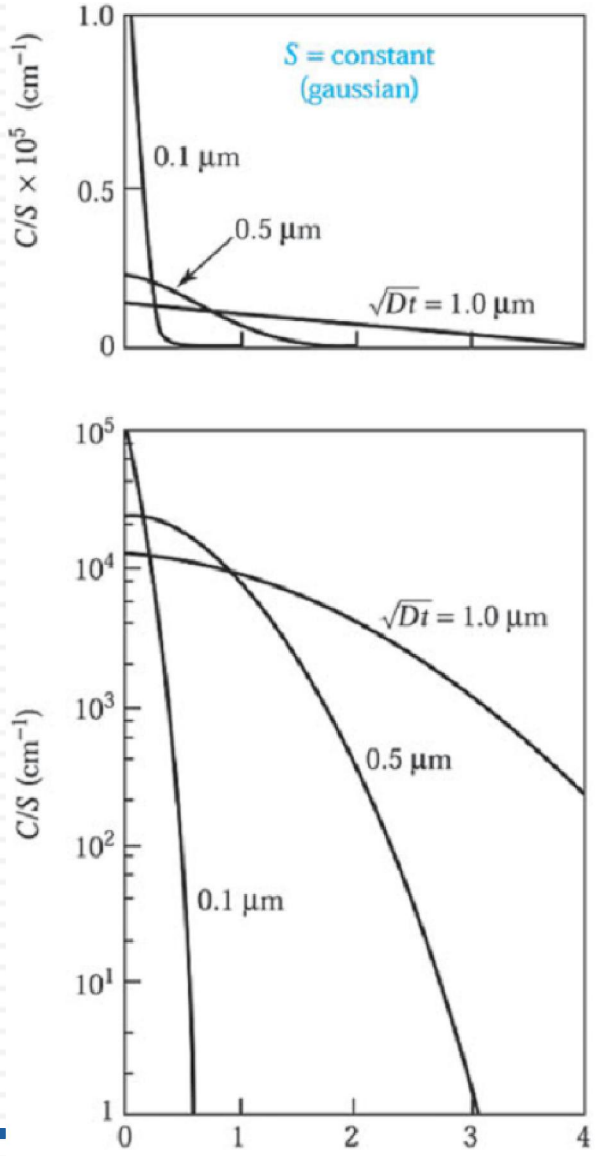
Constant–Total-Dopant Diffusion (2)

- Since the dopant will move into the semiconductor as time increases, to keep the total dopant S constant, the surface concentration at (*x=0*) must decrease

$$C_s(t) = \frac{S}{\sqrt{\pi Dt}}$$

- The gradient of the diffusion profile can be obtained by differentiating the concentration equation w.r.t *x*:

$$\left.\frac{dC}{dx}\right|_{x,t} = \frac{xS}{2\sqrt{\pi}(Dt)^{3/2}} e^{x^2/4Dt} = \frac{x}{2Dt} C(x,t)$$



Two-step diffusion process

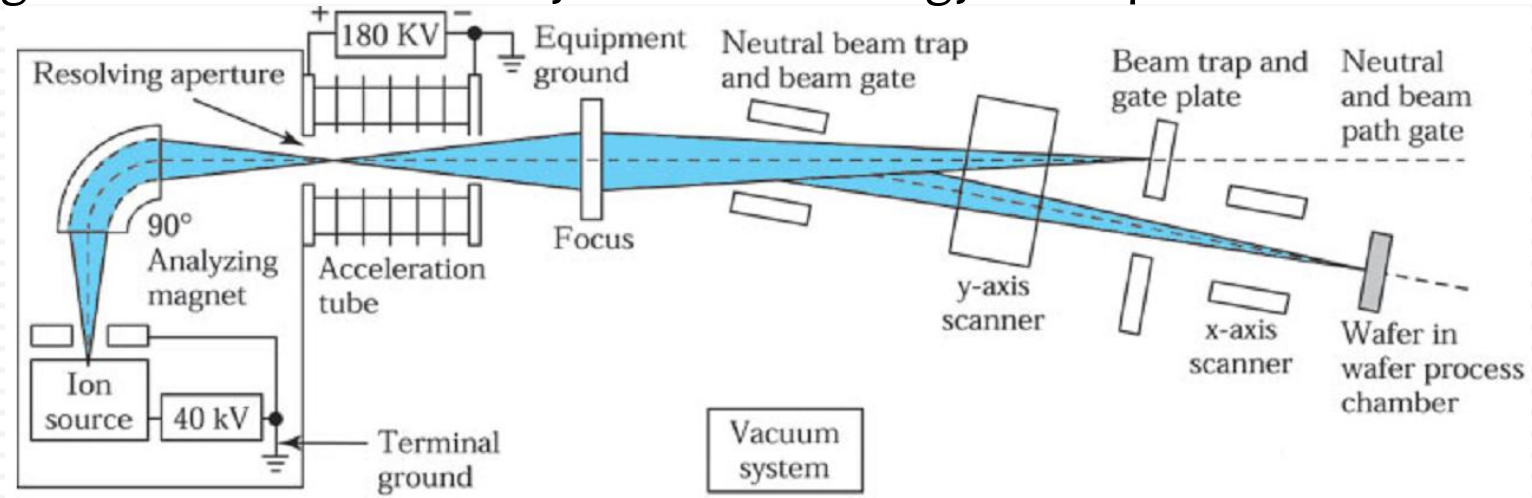
- In integrated-circuit processing, a two-step diffusion process is commonly used in which a predeposition diffused layer is first formed under a constant–surface–concentration condition
- This step is followed by a drive-in diffusion (also called redistribution diffusion) under a constant–total-dopant condition
- For most practical cases, the diffusion length $\sqrt{Dt}$ for the predeposition diffusion is much smaller than the diffusion length for the drive-in diffusion
- Therefore, we can consider the predeposition profile as a delta function at the surface, and we can regard the extent of the penetration of the predeposition profile as negligibly small compared with that of the final profile that results from the drive-in step.

Ion Implantation

- Ion implantation is the introduction of energetic charged particles into a substrate such as silicon
- Implantation energies are between 300 eV and 5 MeV, resulting in ion distributions with average depths ranging from 10 nm to 10 μm
- The main advantages of ion implantation are its more precise control and reproducibility of impurity dopings and its lower processing temperature than those of the diffusion process
- Basic CMOS processes usually use fifteen to seventeen ion implants per wafer

Ion Implantation (2)

- Figure shows schematically a medium-energy ion implantor



- An extraction voltage, around 40 kV, causes the charged ions to move out of the ion source chamber into a mass analyzer
- The magnetic field of the analyzer is chosen such that only ions with the desired mass-to-charge ratio can travel through it without being filtered
- The selected ions then enter the acceleration tube, where they are accelerated to the implantation energy
- The ion beam is then scanned over the wafer surface using electrostatic deflection plates and is implanted into the semiconductor substrate

Ion Implantation (3)

- The energetic ions lose their energies through collision with electrons and nuclei in the substrate and finally come to rest at some depth within the lattice
- The average depth can be controlled by adjusting the acceleration energy
- The dopant dose can be controlled by monitoring the ion current during implantation
- The principal side effect is the disruption or damage of the semiconductor lattice due to ion collisions
- Therefore, a subsequent annealing treatment is needed to remove these damages

Ion Distribution

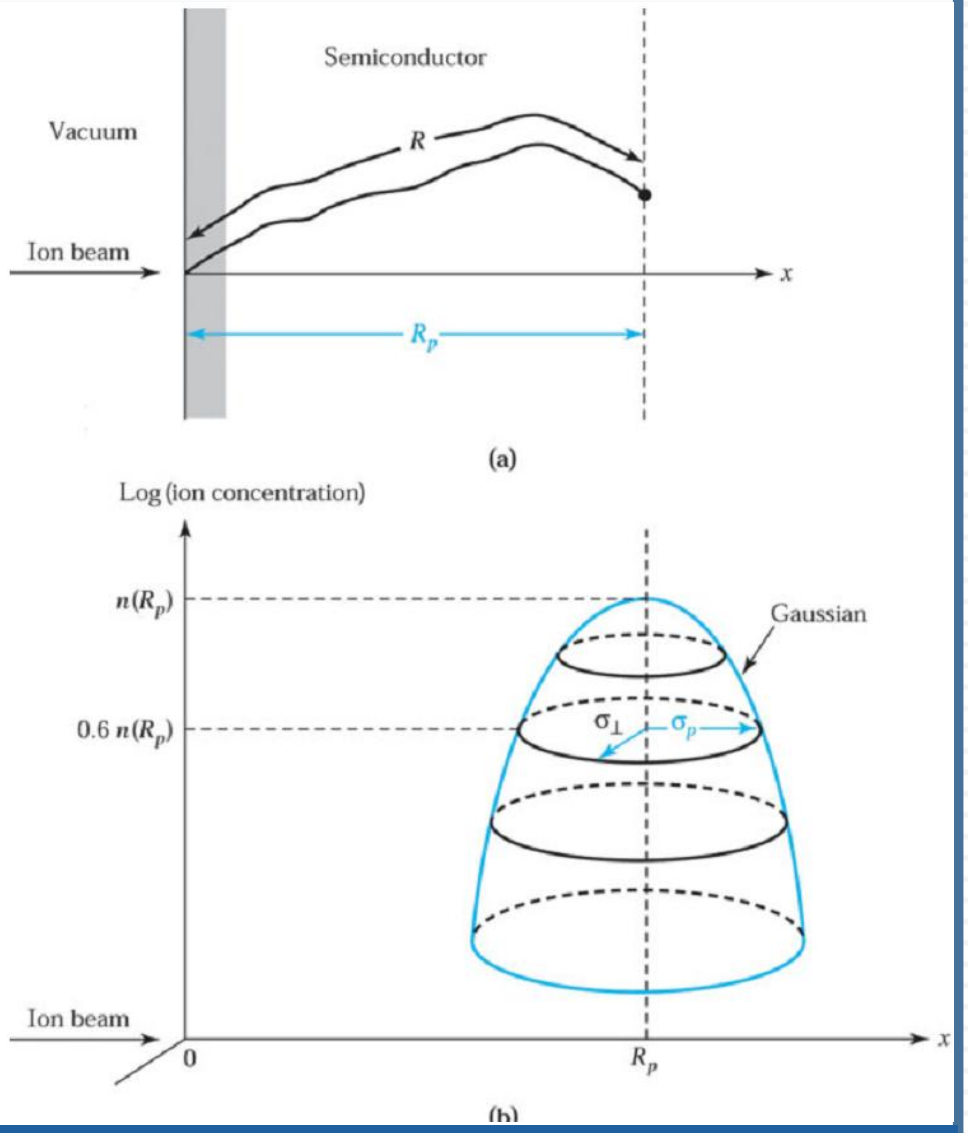
- The total distance that an ion travels in coming to rest is called its range *R* and the projection of this distance along the axis of incidence is called the projected range R_P
- The implanted impurity profile can be approximated by a Gaussian distribution function:

$$n(x) = \frac{S}{\sqrt{2\pi}\sigma_p} \exp\left[- \frac{(x - R_p)^2}{2\sigma_p^2} \right],$$

where σ and σ_p are constants called the lateral and projection straggles, respectively; *S* is the ion dose per unit area

Ion Distribution (2)

- Figure shows a schematic of the ion range R and projected range R_p, and the distribution of the implanted ions
- for diffusion, the maximum concentration is at $x = 0$, whereas for ion implantation the maximum concentration is at the projected range R_p



Implant Damage and Annealing

- When energetic ions enter a semiconductor substrate, they lose their energy in a series of nuclear and electronic collisions and finally come to rest
- The electronic-energy loss can be accounted for in terms of electronic excitations to higher energy levels or of the generation of electron-hole pairs. However, electronic collisions do not displace semiconductor atoms from their lattice positions
- Only nuclear collisions can transfer sufficient energy to the lattice that host atoms are displaced, resulting in implant damage
- These displaced atoms may possess large fractions of the incident energy, and can in turn cause cascades of secondary displacement of nearby atoms to form a tree of disorderalong the ion path
- When the displaced atoms per unit volume approach the atomic density of the semiconductor, the material becomes amorphous.

Annealing

- Because of the damaged region and the disorder cluster that result from ion implantation, semiconductor parameters such as mobility and lifetime are severely degraded
- In addition, most of the ions as implanted are not located in substitutional sites
- To activate the implanted ions and restore mobility and other material parameters, we must anneal the semiconductor at an appropriate combination of time and temperature
- Annealing is a heat treatment that alters the microstructure of a material, causing changes in properties
- In conventional annealing, we use an open-tube batch-furnace system similar to that for thermal oxidation

Annealing (2)

- This process requires long time and high temperature to remove the implant damages
- However, conventional annealing may cause substantial dopant diffusion and cannot meet the requirement for shallow junctions and narrow doping profiles
- Rapid thermal annealing (RTA) is an annealing process that employs a variety of energy sources with a wide range of times, from 100 seconds down to nanoseconds—all short compared with conventional annealing
- RTA can activate the dopant fully with minimal redistribution
- In RTA, wafer is heated quickly under atmospheric conditions or at low pressure to reduce transient-enhanced diffusion which is the very large increase in dopant diffusivity in ion-implanted silicon resulting from the implantation process