SEMICONDUCTOR TECHNOLOGY

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Crystal Growth and Epitaxy

Semiconductor Devices – Physics and Technology
Chapter 11

Introduction

- Silicon (Si) and Gallium Arsenide (GaAs) are the most commonly used semiconductors
- We will describe common techniques for growing single crystals of Si
- Specifically, we will cover the following topics:
  - Basic techniques to grow silicon single-crystal ingots
  - Wafer-shaping steps from ingots to polished wafers
  - Material characterization and silicon wafer defects
  - Basic techniques of epitaxy, that is, growing a single-crystal layer on a single-crystal substrate

SILICON CRYSTAL GROWTH FROM THE MELT

- The Czochralski process is the most common method for semiconductor single crystal growth
- The starting material for silicon is a relatively pure form of sand (SiO_2) called quartzite. This is placed in a furnace with various forms of carbon (coal, coke, and wood chips)

$$SiC\ (solid) + SiO_2\ (solid) \rightarrow Si\ (solid) + SiO\ (gas) + CO\ (gas)$$

- This process produces metallurgical-grade silicon with a purity of about 98%
- Next, the silicon is treated with hydrogen chloride (HCl) to form trichlorosilane ($SiHCl_3$)

$$Si\ (solid) + 3HCl\ (gas) \xrightarrow{300^oC} SiHCl_3\ (gas) + H_2\ (gas)$$

Starting Material

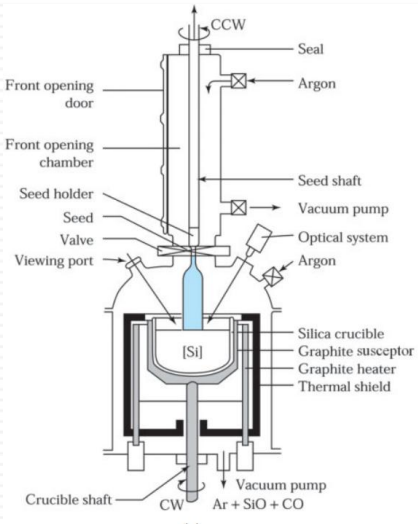
- The $SiHCl_3$ is a liquid at room temperature
- Fractional distillation of the liquid removes the unwanted impurities
- The purified $SiHCl_3$ is then used in a hydrogen reduction reaction to prepare the electronic-grade silicon (EGS):

$$SiHCl_3(gas) + H_2(gas) \rightarrow Si(solid) + 3HCl(gas)$$

- The EGS, a polycrystalline material of high purity, is the raw material used to prepare device-quality, single-crystal silicon
- Pure EGS generally has impurity concentrations in the parts-per-billion range

The Czochralski Technique

- The Czochralski technique uses an apparatus called a crystal puller:
  - a furnace, which includes a fused-silicon (SiO_2) crucible, a graphite susceptor, a rotation mechanism, a heating element, and a power supply
  - a crystal-pulling mechanism that includes a seed holder and a rotation mechanism
  - an ambient control that includes a gas source, a flow control, and a exhaust system
- The main goal is to produce a single-crystal Si from the polycrystalline EGS



The Czochralski Technique (2)

- Polycrystalline EGS is placed in the furnace and heated to 1500°c to form silicon melt
- A suitably oriented seed crystal is suspended over the crucible in a seed holder and inserted to the melt
- The seed holder is slowly withdrawn from the melt with a rotating movement
- The molten silicon adhering to the crystal freezes or solidifies, using the crystal of the seed crystal as a template
- Progressive freezing at the solid-liquid interface yields a large single crystal
- The desired impurity concentration is obtained by adding impurities to the melt in the form of heavily doped silicon prior to crystal growth

Distribution of Dopant

- A known amount of dopant is added to the melt to obtain the desired concentration
- For silicon, boron and phosphorus are the most common dopants for *p*- and *n*-type materials, respectively
- As a crystal is pulled from the melt, the doping concentration of solid Si is usually different from Si melt at the interface
- The ratio of the dopant concentrations in the solid and liquid silicon at the interface is defined as the *equilibrium segregation coefficient* $k_0 = \frac{C_s}{C_l}$

where C_s, C_l: dopant concentrations in the solid and liquid Si

- K_o *has a fixed value* less than 1 for most dopants indicating that during growth the dopants are rejected into the melt

Distribution of Dopant

- Consider a crystal being grown from a melt having an initial weight M_0 with an initial doping concentration C_0 in the melt
- At a given point of growth:
  - weight of crystal has been grown = M (*gm*),
  - the amount of dopant remaining in the melt = S (*gm*)
- For an incremental amount of the crystal with weight dM, the corresponding reduction in the dopant ($-dS$) from the melt is $C_s dM$, where C_s is the doping concentration in the crystal:

$$-dS = C_s dM$$

- The remaining weight of the melt is $M_0 - M$, and the doping concentration in the liquid C_l is given by

$$C_l = \frac{S}{M_0 - M}$$

- Dividing the equations and substituting $k_0 = C_s/C_l$ yields

Distribution of Dopant (2)

$$\frac{dS}{S} = -k_0\left(\frac{dM}{M_0 - M}\right)$$

- Given the initial weight of the dopant, $C_0 M_0$, we can integrate

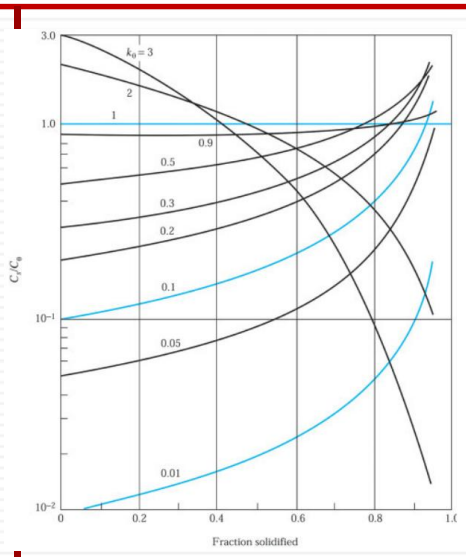
$$\int_{C_0 M_0}^{S} \frac{dS}{S} = k_0 \int_0^M \frac{-dM}{M_0 - M}$$

$$C_s = k_0 C_0 \left(1 - \frac{M}{M_0}\right)^{k_0 - 1}$$

- Check example 1 (Page 361, Sze)

Distribution of Dopant Curves

- Figure shows curves for growth from the melt showing the doping concentration in a solid as a function of the fraction solidified
- As crystal growth progresses
  - a composition initially at k_oC_o will increase continually for $k_o < 1$
  - and decrease continually for $k_o > 1$
  - when $k_o \cong 1$, a uniform impurity distribution can be obtained



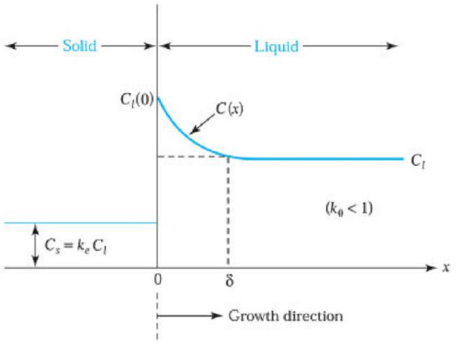
Effective Segregation Coefficient

- Effective segregation coefficient k_e is the ratio of C_s and the impurity concentration far away from the interface

$$k_e = \frac{C_s}{C_l} = \frac{k_0}{k_0 + (1 - k_0)e^{-v\delta/D}}$$

where D is the dopant diffusion coefficient in the melt, v is the crystal growth velocity, δ is the melt width to be crystallized

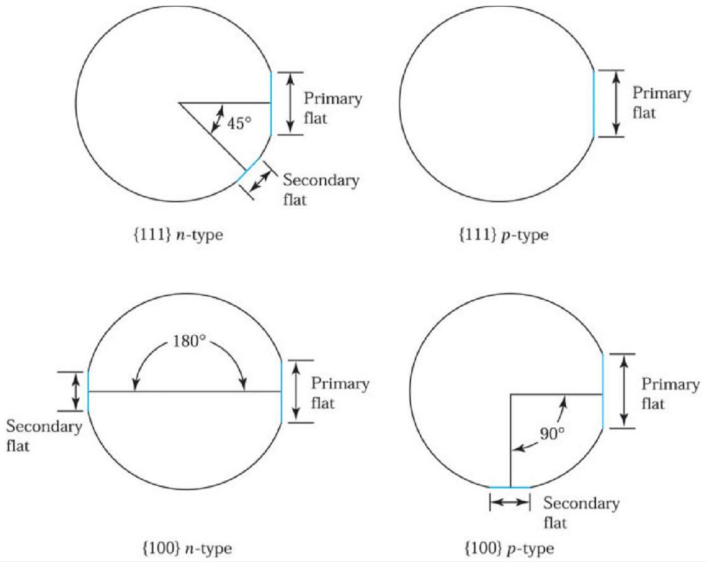
- Uniform doping distribution ($k_e \rightarrow 1$) in the crystal can be obtained by employing a high pull rate and low rotation speed (since δ is inversely proportional to the rotation speed)



Material Characterization

- After a crystal is grown, the first shaping operation is to remove the seed and the other end of the ingot, which is last to solidify
- The next operation is to grind the surface so that the diameter of the material is defined
- After that, one or more flat regions are ground along the length of the ingot
- These regions, or flats, mark the specific crystal orientation of the ingot and the conductivity type of the material
- The largest flat, the primary flat, allows a mechanical locator in automatic processing equipment to position the wafer and to orient the devices relative to the crystal

Wafer Shaping

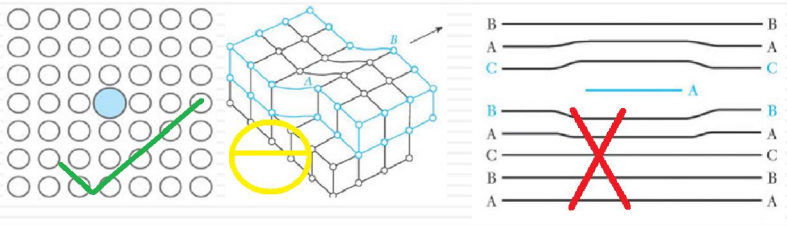


Wafer Shaping (2)

- After slicing, both sides of the wafer are lapped using a mixture of Al_2O_3 and glycerine to produce a typical flatness uniformity within 2 μm
- The lapping operation usually leaves the surface and edges of the wafer damaged and contaminated
- The damaged and contaminated regions can be removed by chemical etching
- The final step of wafer shaping is polishing to provide a smooth, specular surface where device features can be defined by lithographic processes

Crystal Defects

- A real crystal (such as a silicon wafer) differs from the ideal crystal in:
  - It is finite; thus, surface atoms are incompletely bonded.
  - Furthermore, it has defects, which strongly influence the electrical, mechanical, and optical properties of the semiconductor.
- There are four categories of defects: point defects, line defects, area defects, and volume defects



Treating Crystalline Silicon Defects

- Crystal silicon must contain undesirable impurities such as Oxygen and Carbon due to the fabrication process
- Certain precipitates can capture harmful impurities; this is called gettering
- Gettering is a general term meaning a process that removes harmful impurities or defects from the region in a wafer where devices are fabricated
- It is difficult to reduce the concentrations of impurities by purifying the wafers and by excluding metal contaminants from manufacturing environments
- There are two basic methods for gettering
  - Intrinsic gettering, which makes use of oxygen precipitates to getter metal atoms within the wafer bulk
  - The other, called extrinsic gettering, is created on the wafer backside by many methods such as ion implantation. Once the backside damage sites are created, any subsequent high-temp processing step will allow the metal atoms to diffuse to the backside where they can be trapped

Treating Crystalline Silicon Defects (2)

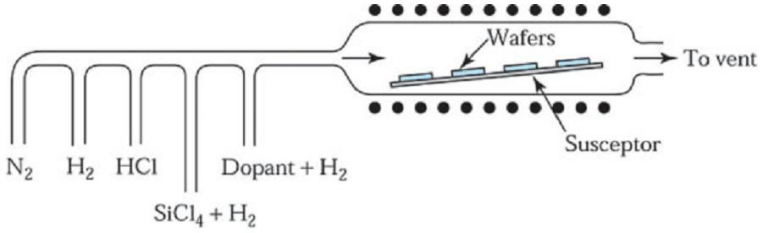
- When the wafer is subjected to high-temperature treatment (e.g., 1050°C in N_2), oxygen evaporates from the surface
- This lowers the oxygen content near the surface
- The treatment creates a defect-free (or denuded) zone for device fab
- The depth of the defect-free zone depends on the time and temperature of the thermal cycle and on the diffusivity of oxygen in Silicon.

EPITAXIAL-GROWTH TECHNIQUES

- In an epitaxial process, the substrate wafer acts as the seed crystal
- The epitaxial layer can be grown at a temperature substantially below the melting point
- When a lightly doped crystalline layer is grown over a substrate that is heavily doped, then a higher breakdown voltage is achieved, and at the same time the collector resistance is kept low.
- The epitaxial layer raises the transistor's breakdown voltage while dramatically increasing its switching speed
- The common techniques for epitaxial growth are
  - Chemical-vapor deposition (CVD)
  - Molecular-beam epitaxy (MBE)

Chemical-Vapor Deposition (CVD)

- The mechanism of CVD involves a number of steps
  a) The reactants such as the gases and dopants are transported to the substrate region
  b) They are transferred to the substrate surface where they are adsorbed
  c) A chemical reaction occurs, catalyzed at the surface, followed by growth of the epitaxial layer
  d) The gaseous byproducts are desorbed into the main gas stream, and
  e) The reaction byproducts are transported out of the reaction chamber



CVD for Silicon

- The overall reaction of silicon tetrachloride ($SiCl_4$) that results in the growth of silicon layers is

$$SiCl_4\ (gas) + 2H_2\ (gas) \leftrightarrows Si\ (solid) + 4HCl\ (gas)$$

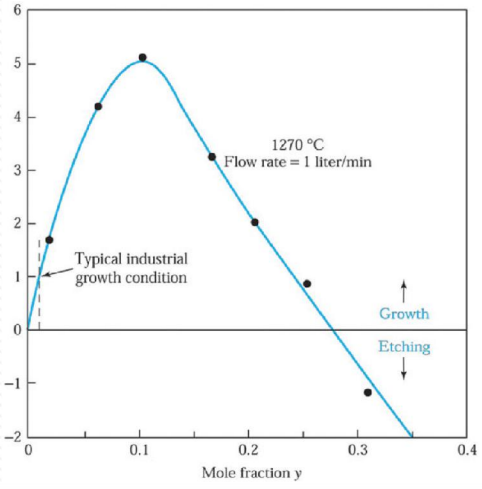
- The typical reaction temperature is 1200°C
- The dopant is introduced at the same time as the silicon tetrachloride during epitaxial growth
- Gaseous diborane (B_2H_6) is used as the p-type dopant, whereas phosphine (PH_3) and arsine (AsH_3) are used as n-type dopants
- Gas mixtures are used with hydrogen as the diluent to allow control of flow rates for the desired doping concentration

CVD for Silicon (2)

- An additional competing reaction is taking place along with the first reaction

$$SiCl_4\ (gas) + Si\ (solid) \leftrightarrows 2SiCl_2\ (gas)$$

- As a result, if the $SiCL_4$ concentration is too high, etching rather than growth of silicon will take place
- Figure shows the effect of the concentration of silicon tetrachloride in the gas on the reaction
- The *mole fraction* is defined as the ratio of the number of molecules of a given species to the total number of molecules



Summary

- Several techniques are available to grow single crystals of silicon and gallium arsenide. For silicon crystals, we use sand (SiO_2) to produce polycrystalline silicon, which then serves as the raw material in a Czochralski puller
- A seed crystal with the desired orientation is used to grow a large ingot from the melt
- Over 90% of silicon crystals are prepared by this technique
- During crystal growth, the dopant in the crystal will redistribute
- A key parameter is the segregation coefficient, i.e., the ratio of the dopant concentration in the solid to that in the melt. Since most coefficients are less than 1, the melt becomes progressively enriched with the dopant as the crystal grows.

Summary (2)

- After a crystal is grown, it usually goes through wafer-shaping operations to give an end product of highly polished wafers with a specified diameter, thickness, and surface orientation
- A real crystal has defects that influence the electrical, mechanical, and optical properties of the semiconductor.
- These defects are point defects, line defects, area defects, and volume defects
- We also discussed means to minimize such defects
- A technology closely related to crystal growth is the epitaxial process where the substrate wafer is the seed
- High-quality, single-crystal films can be grown at temperatures 30%–50% lower than the melting point
- We explained the CVD method to grow epitaxial layer on Si

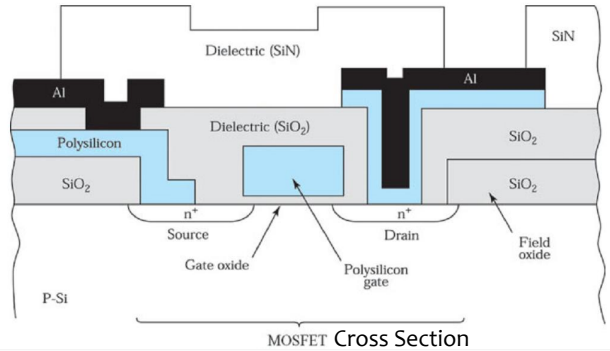
Film Formation

Semiconductor Devices – Physics and Technology

Chapter 12

Introduction

- To fabricate discrete devices and integrated circuits, we use many different kinds of thin films classified into:
  - Thermal oxides
  - Dielectric layers
  - Polycrystalline silicon
  - Metal films



MOSFET Cross Section

Outline

- In this section we will cover the following topics:
  - The thermal oxidation process to form silicon dioxide (SiO_2)
  - Chemical-vapor deposition techniques to form dielectrics and polysilicon films
  - Metallization and related global planarization

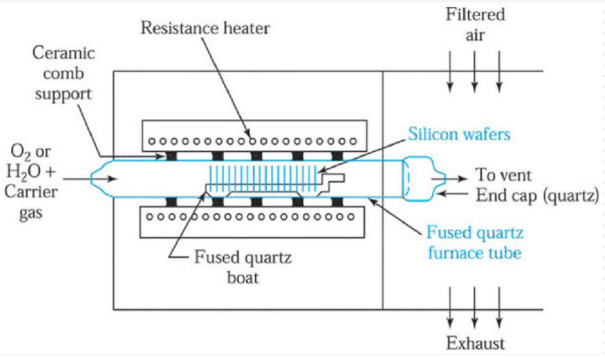
Thermal Oxidation

- The gradient of a thin layer of silicon dioxide on a silicon wafer is a basic feature of the planar technology
- Semiconductors can be oxidized by various methods including:
  - thermal oxidation,
  - electrochemical anodization,
  - and plasma reaction
- Thermal oxidation is the key process in modern silicon integrated-circuit technology

Thermal Oxidation

- The basic thermal oxidation setup is shown in Figure
- The reactor consists of a resistance-heated furnace, a cylindrical fused-quartz tube containing the silicon wafers held vertically in a slotted quartz boat, and a source of either pure dry oxygen or pure water vapor

❑ The oxidation temperature is generally in the range of 900°-1200 °C and the typical gas flow rate is about 1 liter/min.

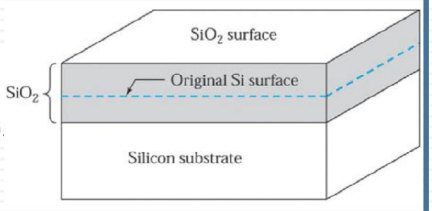


Kinetics of Growth

- The following chemical reactions describe the thermal oxidation of silicon in oxygen or water vapor:

$$Si(solid) + O_2\,(gas) \rightarrow SiO_2\,(solid),$$

$$Si(solid) + 2H_2O\,(gas) \rightarrow SiO_2\,(solid) + 2H_2\,(gas).$$



- Example:

If a silicon oxide layer of thickness x is grown by thermal oxidation, what is the thickness of silicon being consumed? The molecular weight of Si is 28.9 g/mol, and the density of Si is 2.33 g/cm^3. The corresponding values for SiO_2 are 60.08 g/mol and 2.21 g/cm^3

Example

SOLUTION The volume of 1 mol of silicon is

$$\frac{\text{Molecular weight of Si}}{\text{Density of Si}} = \frac{28.9\ \text{g/mole}}{2.33\ \text{g/cm}^3} = 12.06\ \text{cm}^3/\text{mol}.$$

The volume of 1 mol of silicon dioxide is

$$\frac{\text{Molecular weight of } SiO_2}{\text{Density of } SiO_2} = \frac{60.08\ \text{g/mol}}{2.21\ \text{g/cm}^3} = 27.18\ \text{cm}^3/\text{mol}.$$

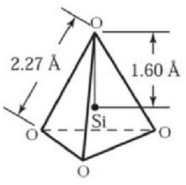
Since 1 mol of silicon is converted to 1 mol of silicon dioxide,

$$\frac{\text{Thickness of Si} \times \text{area}}{\text{Thickness of } SiO_2 \times \text{area}} = \frac{\text{volume of 1 mol of Si}}{\text{volume of 1 mol of } SiO_2},$$

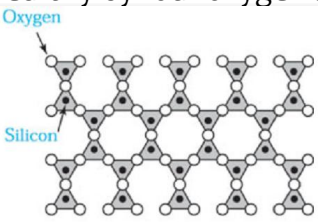
$$\boxed{\frac{\text{Thickness of Si}}{\text{Thickness of } SiO_2} = \frac{12.06}{27.18} = 0.44,}$$

Kinetics of Growth (2)

- The basic structural unit of thermally grown silicon dioxide is a silicon atom surrounded tetrahedrally by four oxygen atoms

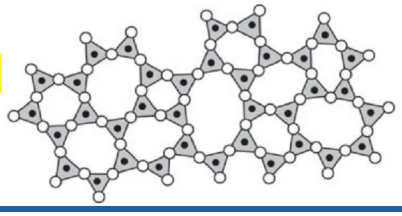


Basic structural unit of SiO2



Quartz crystal lattice

Amorphous structure of SiO2



Kinetics of Growth (3)

- Silicon dioxide (Silica) has several crystalline structures (e.g., quartz) and an amorphous structure
- When silicon is thermally oxidized, the silicon dioxide structure is amorphous
- Typically amorphous silica has a density of 2.21 g/cm^3 compared with 2.65 g/cm^3 for quartz
- The basic difference between the crystalline and amorphous structures is that the former is a periodic structure, extending over many molecules, whereas the latter has no periodic structure at all

Basic Model for the Thermal Oxidation of Silicon

- The kinetics of thermal oxidation of silicon can be studied using the simple model illustrated in Figure
- The flux F_1 can be written as

$$F_1 = D\frac{dC}{dx} \cong \frac{D(C_0 - C_s)}{x},$$

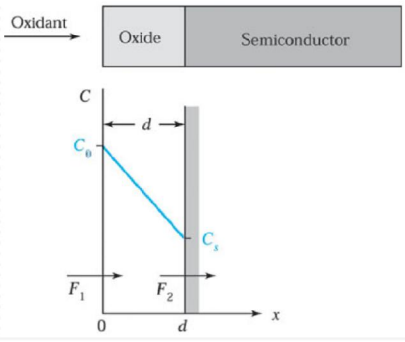
F_1: Flux of the oxidant *(mol/cm^2.s)*

C_o: *equilibrium bulk concentration of the species (Oxygen or water vapor) at the oxidation temperature (molecules/cm^3)*

C_s: *species concentration at the silicon surface (molecules/cm^3)*

D: diffusion coefficient of the oxidizing species (cm^2/s)

x: thickness of the oxide layer



Expression for Thermal Oxidation Thickness

- At the silicon surface, the oxidizing species reacts chemically with silicon
- Assuming the rate of reaction is proportional to the concentration of the species at the silicon surface, the flux F_2 is given by

$$F_2 = \kappa C_s,$$

κ: surface reaction rate constant for oxidation

- At steady state $F_1 = F_2 = F$

$$F = \frac{DC_0}{x + (D/\kappa)}$$

- The growth rate of the oxide layer thickness is given by

$$\frac{dx}{dt} = \frac{F}{C_1} = \frac{DC_0 / C_1}{x + (D/\kappa)}$$

Expression for Thermal Oxidation Thickness (2)

C_1: the number of molecules of the oxidizing species in a unit volume of the oxide (C_1 =2.2×10^{22} molecules/cm^3 for O_2 and 4.4×10^{22} molecules/cm^3 for H_2o)

- We can solve this differential equation subject to the initial condition $x(0)=d_o$, where d_o is the initial oxide thickness

$$x^2 + \frac{2D}{\kappa}x = \frac{2DC_0}{C_1}(t+\tau),$$

where $\tau \equiv (d_0^2 + 2Dd_0/\kappa)C_1 / 2DC_0$

- The oxide thickness after an oxidizing time tis given by

$$x = \frac{D}{k}\left[\sqrt{1 + \frac{2C_0\kappa^2(t+\tau)}{DC_1}} - 1\right]$$

Expression for Thermal Oxidation Thickness (3)

- For small values of *t*, the equation can be approximated to

$$x \cong \frac{C_0 \kappa}{C_1}(t+\tau),$$

- For large values of *t*, it can be approximated to

$$x \cong \sqrt{\frac{2DC_0}{C_1}(t+\tau)}.$$

- During the early stages of oxide growth, when the surface reaction is the rate-limiting factor, the oxide thickness varies linearly with time
- As the oxide layer becomes thicker, the oxidant must diffuse through the oxide layer to react at the silicon-silicon dioxide interface and the reaction becomes diffusion limited
- The oxide growth then becomes proportional to the square root of the oxidizing time, which results in a parabolic growth rate

Expression for Thermal Oxidation Thickness (4)

- The thickness equation is often written in a more compact form

$$x^2 + Ax = B(t+\tau).$$

where $A = 2D/\kappa$, $B = 2DC_0/C_1$ and $B/A = \kappa C_0/C_1$

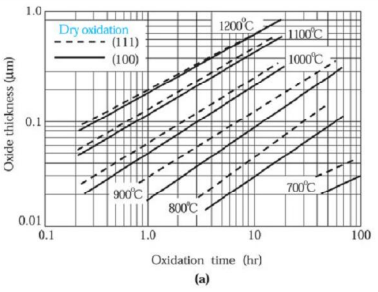
For small values of t,

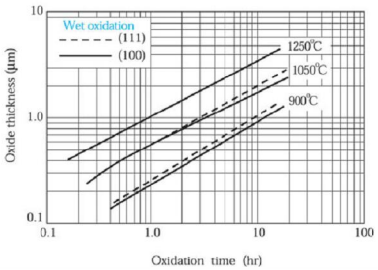
$$x = \frac{B}{A}(t+\tau)$$

and for larger values of t,

$$x^2 = B(t+\tau).$$

- The term *B*/*A* is referred to as the linear rate constant and *B* as the parabolic rate constant (both are function of Temperature)



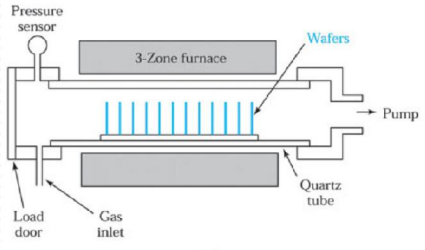


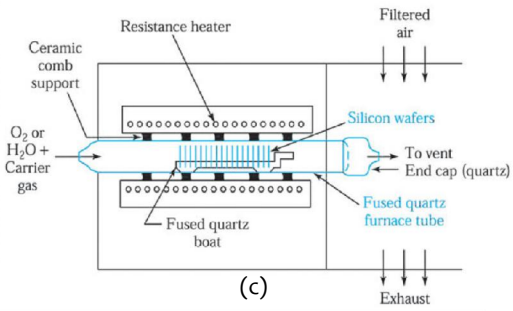
CHEMICAL VAPOR DEPOSITION

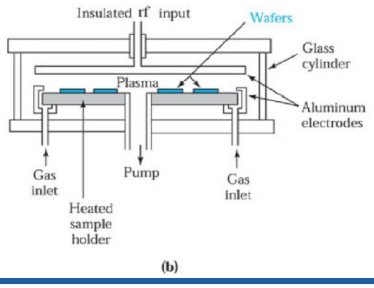
- CVD is used to deposit both dielectric films such as silica glass and nitride and conducting films such as tungsten
- There are three commonly used deposition methods:
  - atmospheric-pressure CVD,
  - low-pressure CVD (LPCVD): it reduces unwanted gas-phase reactions and improve film uniformity across the wafer. However, it suffers from low deposition rates
  - and plasma-enhanced chemical vapor deposition (PECVD, or plasma deposition): plasma energy is added to the thermal energy of a conventional CVD system (Plasma is ionized gas). The main advantage of this reactor is its low deposition temperature. However, its capacity is limited, especially for large-diameter wafers. Another limitation of plasma deposition involves the potential charge imbedded in the film.

CVD Reactors

- Deposition method reactors:
  a) Hot-wall LPCVD reactor
  b) Parallel-plate RF plasma deposition reactor
  c) Atmospheric pressure CVD reactor







CVD Processes

- CVD is a method of forming a thin solid film on a substrate by the reaction of vapor-phase chemicals that contain the required constituents
- The CVD process can be generalized in a sequence of steps:
  - (1) Reactants are introduced into the reactor;
  - (2) Gas species are activated and dissociated by mixing, heating, plasma, or other means;
  - (3) Reactive species are adsorbed on the substrate surface;
  - (4) Adsorbed species undergo chemical reaction or react with other incoming species to form a solid film;
  - (5) Reaction byproducts are desorbed from the substrate surface;
  - (6) Reaction byproducts are removed from the reactor

CVD of Silicon Dioxide

- CVD silicon dioxide does not replace thermally grown oxides because the best electrical properties are obtained with thermally grown films
- CVD oxides are used instead to complement thermal oxides
- A layer of undoped silicon dioxide is used to insulate multilevel metallization, to mask ion implantation and diffusion, and to increase the thickness of thermally grown field oxides
- Low-temperature (300°-500°C) CVD and LPCVD chemical reactions for silicon dioxide is:

$$SiH_4 + O_2 \xrightarrow{450^{O}C} SiO_2 + 2H_2,$$

- Low-temp CVD is suitable for depositing dioxide layers over low-melting temperature materials such as aluminum

CVD of Silicon Dioxide (2)

- For intermediate-temperature deposition (500°-800°C), silicon dioxide can be formed by decomposing $Si(OC_2H_5)_4$, in an LPCVD reactor:

$$Si(OC_2H_5)_4 \xrightarrow{700^{O}C} SiO_2 + \text{byproducts},$$

- This deposition is suitable for polysilicon gates requiring a uniform insulating layer with good step coverage.
- The good step coverage is a result of enhanced surface mobility at higher temperatures.
- The oxides can be doped by adding small amounts of the dopant hydrides (phosphines, arsine, or diborane), similar to the process in epitaxial growth

CVD of Silicon Dioxide (3)

- For high-temperature deposition (900°C), silicon dioxide is formed by reacting dichlorosilane, $SiCl_2H_2$, with nitrous oxide at reduced pressure

$$SiCl_2H_2 + 2N_2O \xrightarrow{900^{O}C} SiO_2 + 2N_2 + 2HCl.$$

- This deposition gives excellent film uniformity and is sometimes used to deposit insulating layers over polysilicon
- Different CVD methods yields silicon dioxide materials with different properties such as density, refractive index, and dielectric constant that can fit different jobs in various fabrication processes

CVD of Silicon Nitride

- Silicon nitride films can be deposited by an intermediate-temperature (750°C) LPCVD process or a low-temperature (300°C) plasma-assisted CVD process
- The LPCVD films are of stoichiometric composition (Si_3N_4) with high density (2.9–3.1 g/cm^3).
- These films can be used to passivate devices because they serve as good barriers to the diffusion of water and sodium
- Because of the low deposition temperature, silicon nitride films can be deposited over fabricated devices and serve as their final passivation
- The plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium diffusion

CVD of Silicon Nitride (2)

- In the LPCVD process, dichlorosilane and ammonia react at reduced pressure to deposit silicon nitride at temperatures between 700° and 800°C

$$3SiCl_2H_2 + 4NH_3 \xrightarrow{\sim 750^{O}C} Si_3N_4 + 6HCl + 6H_2$$

- Good film uniformity and high wafer throughput (the number of wafers processed per hour) are advantages of the reduced-pressure process
- As in oxide deposition, silicon nitride deposition is controlled by temperature, pressure, and reactant concentration.

CVD of Silicon Nitride (3)

- In the plasma-assisted CVD process, silicon nitride is formed either by reacting silane and ammonia in an argon plasma or by reacting silane in a nitrogen discharge
- The plasma dissociates the precursors and creates high-energy forms of the reactant species that accelerate the reaction rate at a much lower temperature
- Ions and electrons are charged species associated with plasma

$$SiH_4 + NH_3 \xrightarrow{300^0\,C} SiNH + 3H_2,$$

$$2SiH_4 + N_2 \xrightarrow{300^0\,C} 2SiNH + 3H_2.$$

- Other dielectric materials with high and low dielectric constants to serve various needs can be created using CVD

CHEMICAL VAPOR DEPOSITION OF POLYSILICON

- Using polysilicon as the gate electrode in MOS devices is a significant development in MOS technology
- One important reason is that polysilicon surpasses aluminum in electrode reliability
- A low-pressure reactor operated between 600° and 650°C is used to deposit polysilicon by pyrolyzing silane according to the following reaction

$$SiH_4 \xrightarrow{600^O\,C} Si + 2H_2.$$

- Process parameters that affect the polysilicon structure are deposition temperature, dopants, and the heat cycle applied following the deposition step
- A columnar structure results when polysilicon is deposited at temperatures of 600°–650°C. This structure is comprised of polycrystalline grains ranging in size from 0.03 to 0.3 μm at a preferred orientation of (110)

CHEMICAL VAPOR DEPOSITION OF POLYSILICON

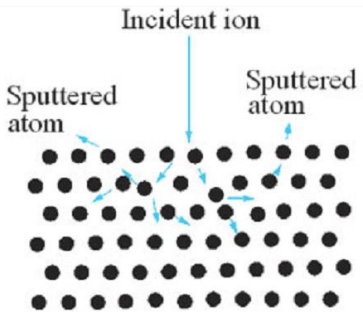
- When phosphorus is diffused at 950°C, the structure changes to crystallite and the grain size increases to between 0.5 and 1.0 μm
- When the temperature is increased to 1050°C during oxidation, the grains reach a final size of 1–3 μm
- Although the initially deposited film appears amorphous when deposition occurs below 600°C, growth characteristics similar to the polycrystalline-grain columnar structure are observed after doping and heating.
- Polysilicon can be doped by diffusion, ion implantation, or the addition of dopant gases during deposition, referred to as in-situ doping
- The implantation method is most commonly used because of its lower processing temperatures

Metallization - Physical-Vapor Deposition

- The primary semiconductor applications of physical-vapor deposition (PVD) technology are the deposition of metal and compounds
- The most common methods of PVD of metals are:
  - evaporation,
  - e-beam evaporation,
  - plasma spray deposition,
  - and sputtering
- Evaporation occurs when a source material is heated above its melting point in an evacuated chamber
- The evaporated atoms then travel at high velocity in straight-line trajectories
- The source can be made molten by resistance heating, by RF heating, or with a focused electron beam

Metallization - Physical-Vapor Deposition (2)

- Sputtering involves the transport of material from a target to a substrate
- It is accomplished by the bombardment of the target surface with gas ions, typically Ar but occasionally other inert gas species (Ne, Kr) or reactive species such as oxygen or nitrogen
- Particles of atomic dimension from the target are ejected as a result of momentum transfer between incident ions and the target



CVD Metal Deposition

- CVD is attractive for metallization because it offers coatings that are conformal, has good step coverage, and can coat a large number of wafers at a time
- The basic CVD setup is the same as that used for the deposition of dielectrics and polysilicon
- LPCVD is capable of producing conformal step coverage over a wider range of topographical profiles, often with lower electrical resistivity than that from PVD

CVD Tungsten

- Tungsten is used both as a contact plug and as a first-level metal
- The CVD tungsten film is known for its excellent step coverage
- The CVD tungsten process has been a key technology enabling multilevel interconnection metallization
- Tungsten can be deposited by using WF_6 as the W source gas, since it is a liquid that boils at room temperature
- WF_6 can be reduced by silicon, hydrogen, or silane. The basic chemistry for CVD-W is as follows

$$WF_6 + 3H_2 \rightarrow W + 6HF \text{ (hydrogen reduction)},$$
$$2WF_6 + 3Si \rightarrow 2W + 3SiF_4 \text{ (silicon reduction)},$$
$$2WF_6 + 3SiH_4 \rightarrow 2W + 3SiF_4 + 6H_2 \text{ (silane reduction)}$$

Aluminum Metalization

- Aluminum and its alloys are used extensively for metallization in integrated circuits because they satisfy the low-resistance requirements
- Aluminum also adheres well to silicon dioxide
- However, the use of aluminum in integrated circuits with shallow junctions often creates problems such as spiking and electromigration
- The Al film can be deposited by a PVD or CVD method

Chemical-Mechanical Polishing

- In recent years, the development of chemical-mechanical polishing (CMP) has become increasingly important for multilevel interconnection because it is the only technology that allows global planarization (i.e., making a flat surface across the whole wafer)
- It offers many advantages over other types of technologies—better global planarization over large or small structures, reduced defect density, and reduced plasma damage
- The CMP process consists of moving the sample surface against a pad that carries slurry between the sample surface and the pad. Abrasive particles in the slurry cause mechanical damage on the sample surface, loosening the material for enhanced chemical attack or fracturing off pieces of surface into the slurry where they dissolve or are swept away
- The process is tailored to provide an enhanced material removal rate from high points on surfaces, thus affecting the planarization because most chemical actions are isotropic

Chemical-Mechanical Polishing (2)

- Mechanical grinding alone can theoretically achieve the desired planarization but is not desirable because of extensive associated damage to the material surfaces
- There are three main parts of the process: the surface to be polished, the pad—the key medium enabling the transfer of mechanical action to the surface being polished—and the slurry, which provides both chemical and mechanical effects.