Alexandria University
Faculty of Engineering
Electrical Engineering Department
Spring Final Exam, January 2015

جامعة الإسكندرية
كلية الهندسة
قسم الهندسة الكهربية
امتحان نهاية الفصل الدراسي الأول (يناير ٢٠١٥)

Course Title and Code Number:
Semiconductor Devices (EE336)
Third Year (Communications and Electronics)
Time Allowed: 90 Mins

اسم المقرر والرقم الكودي له:
النبآئط شبه الموصلة (EE336)
السنة الدراسية الثالثة (اتصالات و الكترونيات)
الزمن: ٩٠ دقيقة

Info and Equation Sheets Are Allowed:

Attempt All Questions: **(45 marks)**

Question 1: **(15 marks)**

a) A pn junction diode has the doping profile sketched in Figure 1. Mathematically $N_D - N_A = N_0(e^{\alpha x} - 1)$, where N_0 and α are constants.

   I. Give a concise statement of the depletion approximation.

   II. Invoking the depletion approximation, sketch the charge density inside the diode.

   III. Establish an expression for the electric field $\mathcal{E}(x)$ inside the depletion region.

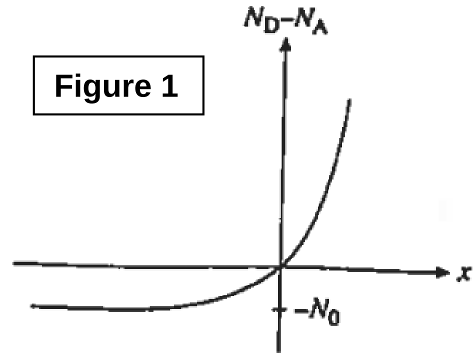

Figure 1

b) Figure 2 is a dimensioned plot of the steady state carrier concentrations inside a step pn junction diode maintained at room temperature.

   I. Is the diode forward or reverse biased? Do low level injection conditions prevail in the quasineutral regions of the diode? Explain how you arrived at your answer.

   II. What are the p-side and n-side doping concentrations?

   III. Determine the diode current I and applied voltage V_A assuming $I_0=100nA$.

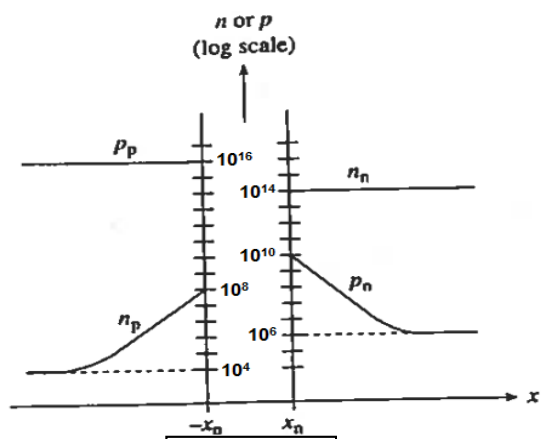

Figure 2

Question 2: **(15 marks)**

a) The doping profile inside the semiconductor component of an MS diode is linearly graded; i.e., $N_D(x) = ax$.

   I. Derive solution for $\rho(x)$, $\mathcal{E}(x)$, $V(x)$, and W inside the semiconductor.

   II. Indicate how V_{bi} is to be determined and computed.

   III. Establish an expression for the junction depletion region capacitance.

b) The electron and hole currents inside a pnp BJT biased in the active mode are plotted in Figure 3. All the currents are referenced to I_1, the hole current injected into the base. Determine:

   I. The emitter efficiency (γ), the base transport factor (α_T), the common emitter d.c. current gain (β_{dc}).

   II. The base current (I_B).

III. Derive the I-V_A relationship for the above transistor connected in the configurations shown in Figure 4 by appropriately using the Ebers-Moll model. The current I should be expressed only in terms of V_A and the Ebers-Moll parameters.

IV. Develop expressions for $\Delta p_B(0)/\Delta p_{B0}$ and $\Delta p_B(W)/\Delta p_{B0}$ in terms of V_A and the Ebers-Moll parameters.

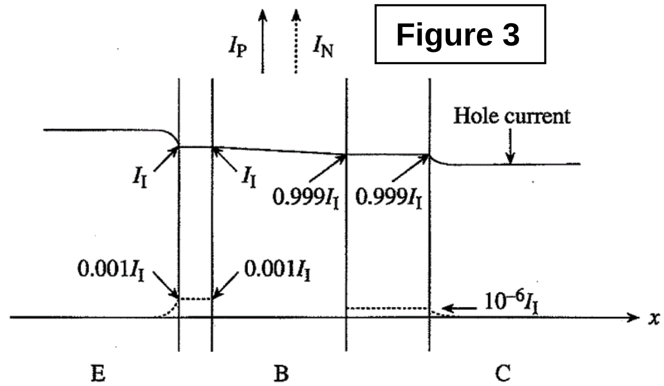

Figure 3

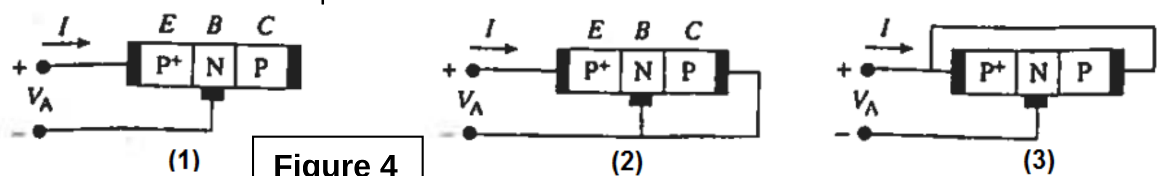

Figure 4

Question 3: **(15 marks)**

a) The energy band diagram for an ideal x_o = 0.2µm MOS-C operated at T = 300°K is sketched in Figure 5. Note that the applied gate voltage causes band bending in the semiconductor such that E_F = E_i at the Si-SiO$_2$ interface. Invoke the delta-depletion approximation as required in answering the questions that follow.

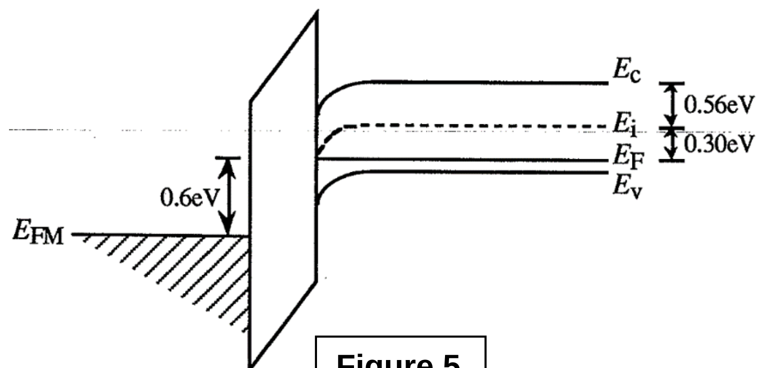

Figure 5

I. Sketch ρ, $\mathcal{E}$, V inside the semiconductor as a function of position.

II. What is the electron concentration at the Si-SiO$_2$ interface?

III. Calculate N_D, ϕ_s, V_G, and the voltage drop ($\Delta\phi_{ox}$) across the oxide at the pictured bias point.

IV. What is the normalized small-signal capacitance, C/C_o, of the MOS-C at the pictured bias point?

b) Suppose a battery $V_B \geq 0$ is connected between the gate and drain of an ideal n-channel MOSFET as pictured in Figure 6. Using the square law results,

I. Sketch I_D versus V_D ($V_D \geq 0$) for $V_B = V_T/2$, $2V_T$;

II. Sketch I_D versus V_B ($0 \geq V_B \geq 5V$) for V_D=0, 5V.

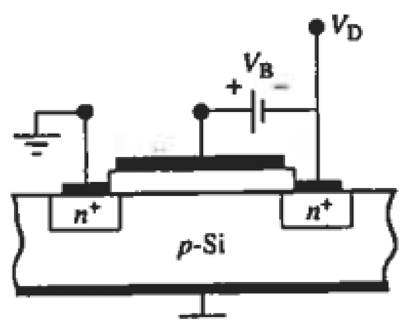

Figure 6

Good Luck

Examiner: ***Dr. Mohammed Morsy***