Alexandria University
Faculty of Engineering
Electrical Engineering Department

Sheet 5 Semiconductor Memories

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1) Consider the DRAM circuit shown in Figure 1 in the text. The threshold voltage of the two pre-charge transistors is 2 V. Calculate the steady state voltages of V_D in Region I and Region II of Figure 2 by assuming the following:
   C = 50 fF
   C_D = 400 fF
   V(C) = V(C/2) =V_Y = 0 V in region I
   While PC is high, no other transistor connected to D or $\overline{D}$ is on.

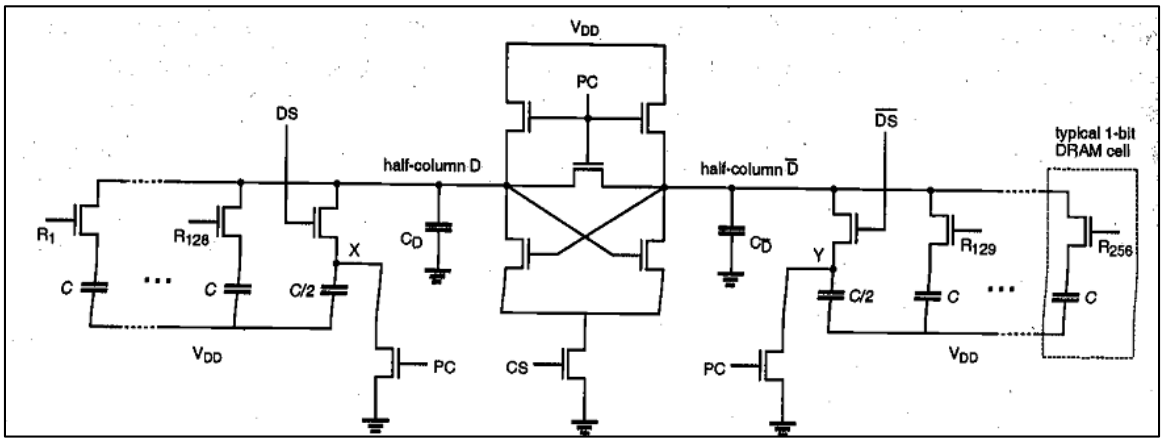

Figure 1

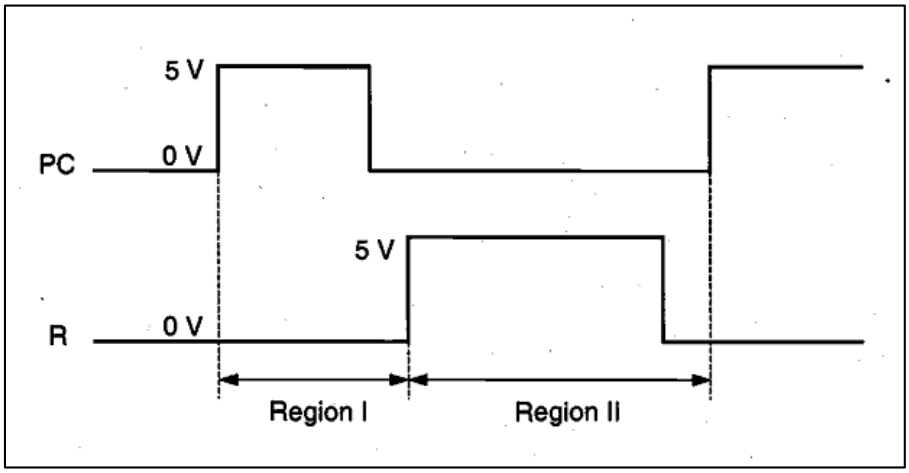

Figure 2

2) A single-transistor DRAM cell is represented by the following circuit diagram (Figure 3). The bit line can be pre-charged to VDD^2 by using a clocked pre-charge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to VDD or 0 V during the WRITE operation with word line at VDD. Using the parameters given:

$V_{T0} = 1$ V
$\gamma = 0.3\ V^{1/2}$
$\left|2\emptyset_f\right| = 0.6\ V$

a) Find the maximum voltage across the storage capacitor Cs after WRITE-I operation, i.e., when the bit line is driven to VDD = 5 V.
b) Assuming zero leakage current in the circuit, find the voltage at the bit line during READ- operation after the bit line is first pre-charged to VDD/2.

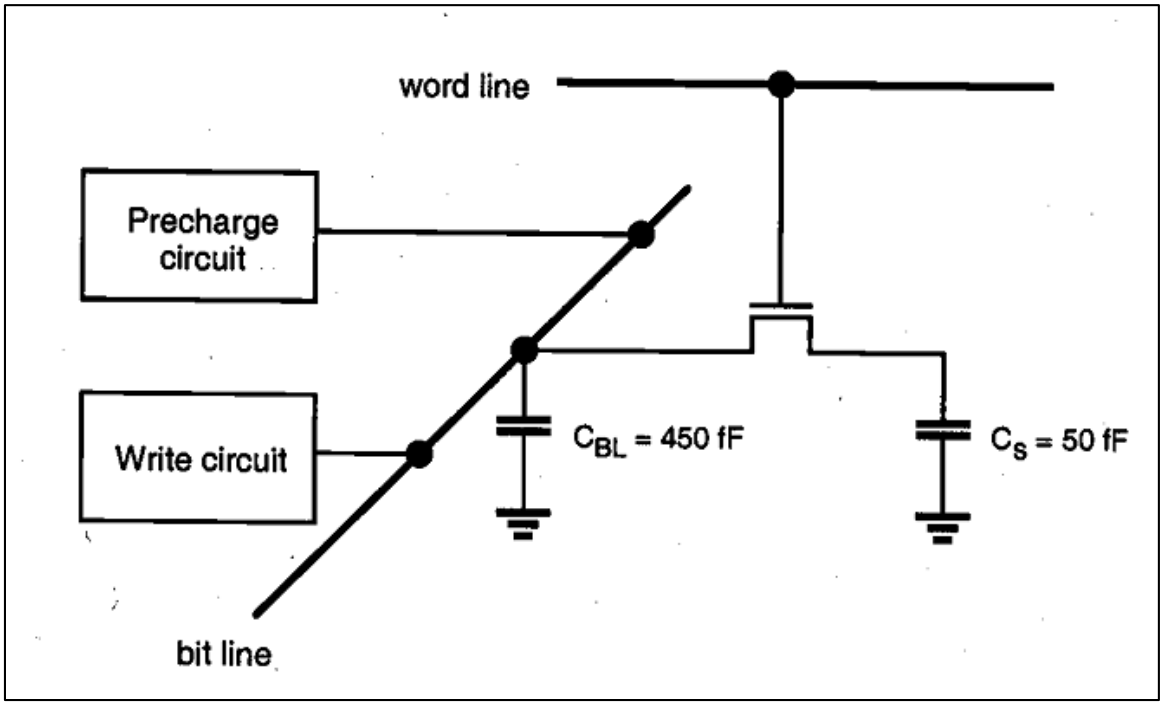

Figure 3

3) A dynamic CMOS Read Only Memory (ROM) has been designed with a core array consisting of 64 rows with a pitch of 12 m and 64 columns with a pitch of 10 μm, as shown on Figure 4. Each column is pre-charged to 5 V by a PMOS transistor during the interval of zero clock phase and then is pulled down after the clock signal switches to 5 V by one or more NMOS transistors (i.e., NOR implementation) with high gate inputs on the appropriate rows. All of the NMOS transistors have channel widths W= 4 μm and source/drain lengths Y = 5 μm. As a designer, you are to determine the propagation delay time from a particular input (on row 64) going high to a particular bit-line output (on column 64) going low t_{pHL} between 50% points. Assume that the input signal to row 64 becomes valid-high only after the pre-charge operation is finished, as shown in the timing diagram. Also, assume that row 64 is running over 30 NMOS transistors and column 64 has 20 NMOS transistors connected to it. For delay calculation, assume that only one NMOS transistor is pulling down. Also assume that PMOS is strong enough to fully charge the pre-charging node during the pre-charge phase of the clock signal and to neglect its drain parasitic capacitance. Device parameters are given:

C_{jsw} = 250 pF/m
Cj0 = 80 μF/m^2
Cox = 350 μF/m^2
L_D = 0.5 μm
K_{eq} = 1.0 for worst-case capacitance
C_{metal} = 2 pF/cm and R_{metal} =0.03 Ω/sq.
C_{po1y} =2 .2 pF/cm and R_{poly} = 25 Ω /sq.
Polysilicon line width = 2 μm
Metal line width = 2 μm
k'_n = 20 μA/V^2
k'_p = 10 μA/V^2
V_{Tn} = - V_{Tp} = 1 V

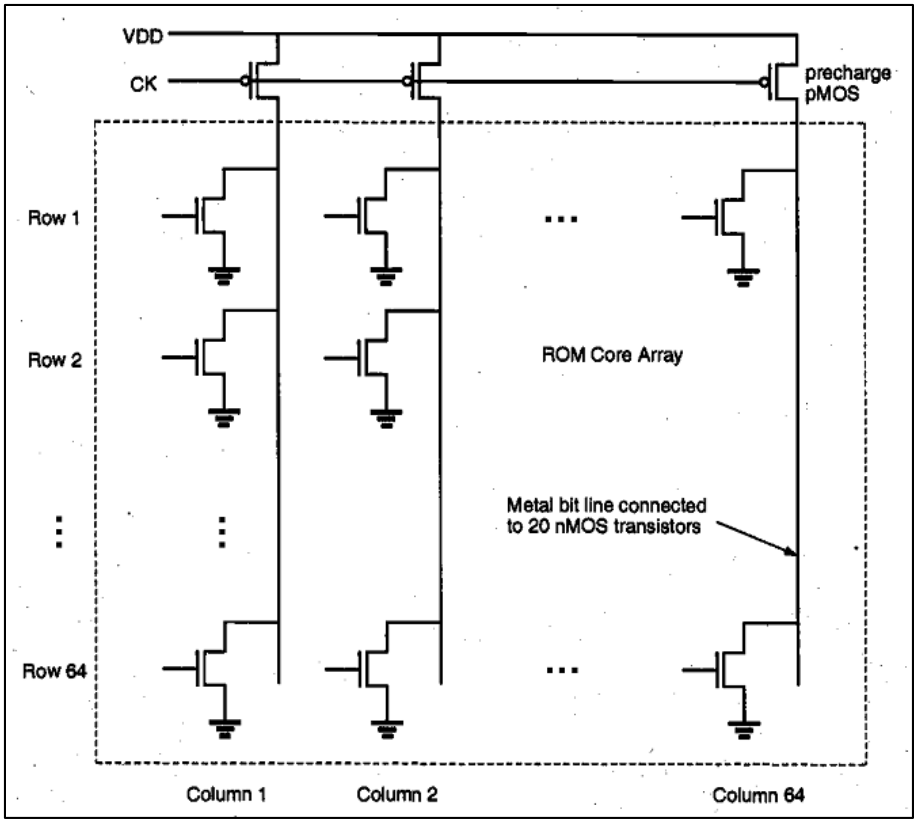

Figure 4

4) Consider the CMOS SRAM cell shown in Figure 5. Transistors Ml and M2 have (W/L) values of 4/4. Transistors M3 and M4 have (W/L) values of 2/4. M5 and M6 are to be sized such that the state of the cell can be changed for Vc < 0.5 V. Assuming that M5 and M6 are the same size, calculate the required (W/L).
Use the following parameters:

$V_{T0,n}$ = 0.7 V
$V_{T0,p}$ = -0.7 V
K'_n = 20 µA/V^2
kp = 10 µA/V^2
γ = 0.4 $V^{1/2}$
$|2\emptyset_f| = 0.6\,V$

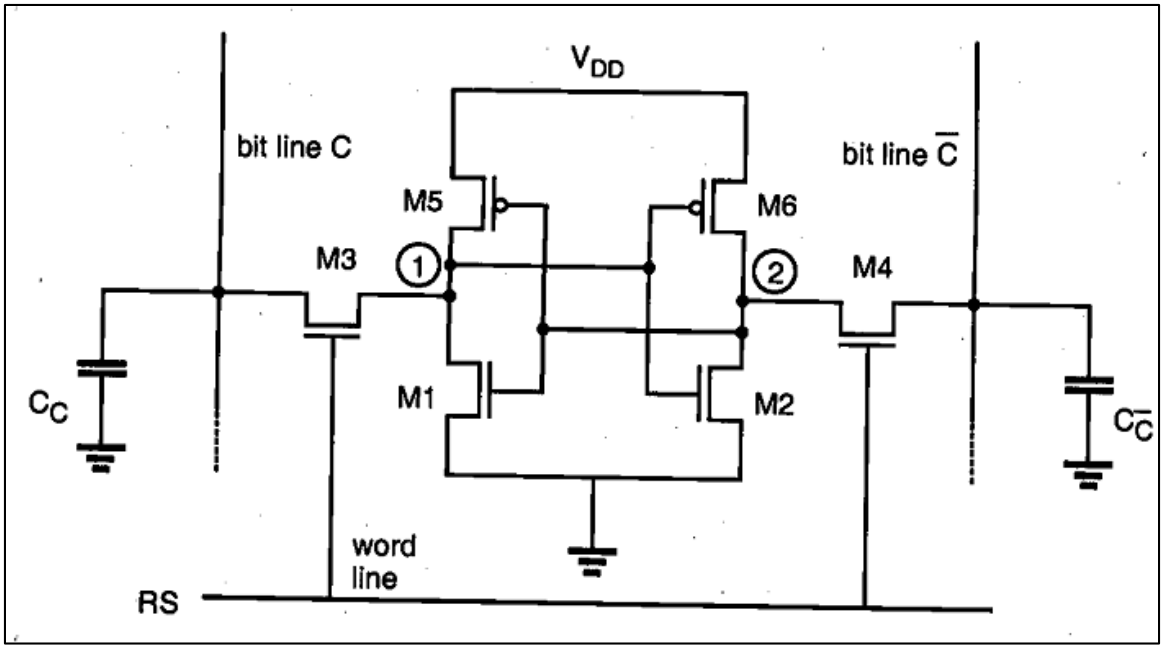

Figure 5

5) Draw circuit diagrams of the row decoder and the column decoder for an EPROM with 4 rows and 2 columns. Use NMOS technology. Develop formulas for the row and column delays in the EPROM. Define any terms in your formulas which are not obvious.

6) Consider an 8k x 8k SRAM, which has 64k (= 65536) memory cells and 8 output lines. In the particular SRAM under discussion, 7 address bits go to the row decoder and 6 address bits go to the column decoder. Bit lines are pre-charged to VDD = 5 V before each read operation. A read operation is complete when the bit line has discharged by 0.5 V. A memory cell can provide 1.0 mA of pull-down current to discharge the bit line.

   a) Word line resistance is 390 Ω per memory cell. What formula was used to calculate this resistance?
   b) Word line capacitance is 22 fF per memory cell. What formula was used to calculate this capacitance?
   c) Bit line capacitance is 6 fF per memory cell. What formula was used to calculate this capacitance?
   d) Calculate the access time (row delay + column delay) for this SRAM.
   e) Describe the operation and design of the word line decoder and the bit line decoder.