



Alexandria University

Faculty of Engineering

Electrical Engineering Department

Sheet 4 Sequential MOS Logic Circuits

- 1) Consider the monostable multivibrator circuit drawn in Figure 1. Calculate the output pulse width.

$$V_{T(\text{dep})} = -2 \text{ V}$$

$$V_{T(\text{enh})} = 1 \text{ V}$$

$$k' = 20 \mu\text{A}/\text{V}^2$$

$$Y = 0$$

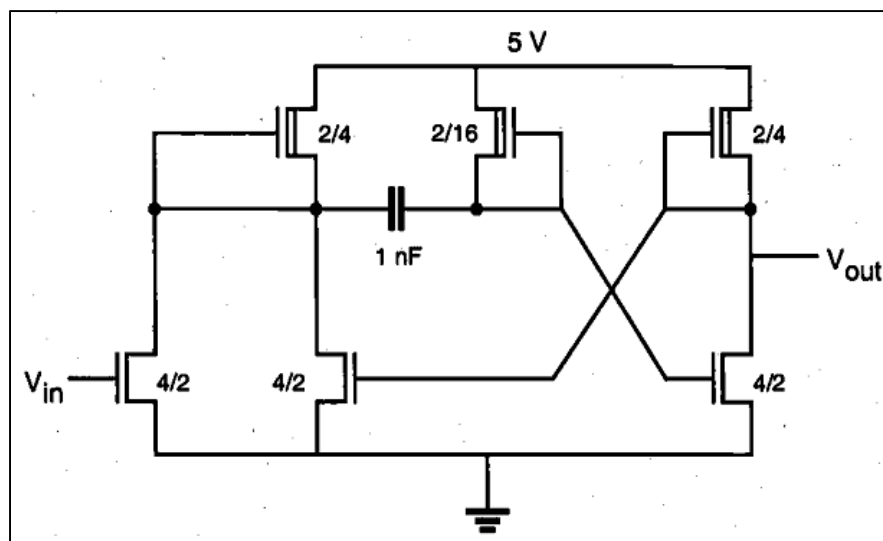


Figure 1

- 2) Shown in Figure 2 is an NMOS Schmitt trigger. Draw the voltage transfer characteristic. Include values for all important points on the graph. Use the parameters in Problem 1 and $\lambda = 0$. W/L ratios for the transistors are given below.

	M1	M2	M3	M4
W/L	1	0.5	10	1

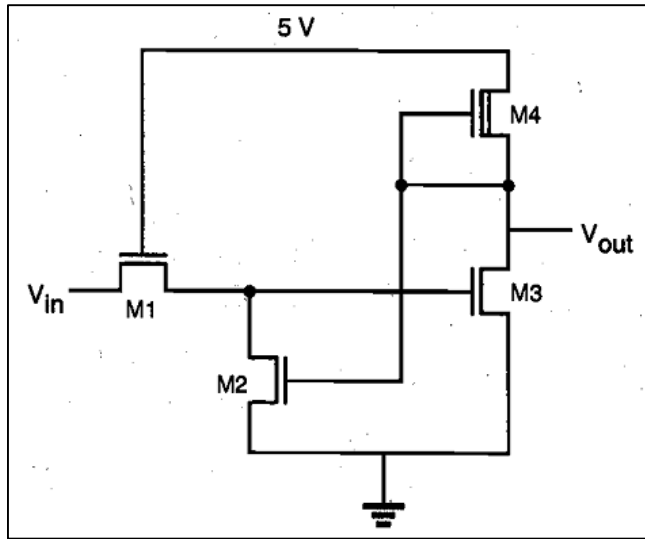


Figure 2

3) Design a circuit to implement the truth table shown in Figure 3. A gate-level design is sufficient.

S	R	Q	\bar{Q}
0	1	1	0
1	0	0	1
1	1	Q	\bar{Q}

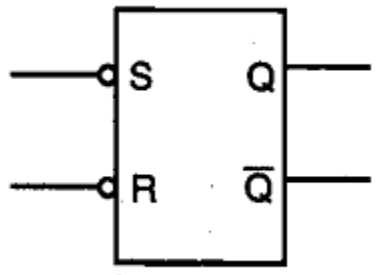


Figure 3

4) The circuit you have designed in Problem 3 is embedded in the larger circuit shown in Figure 4. Complete the timing diagram for the output.

5) The voltage waveforms shown below (in Figure 5) are applied to the NMOS JK master-slave flip-flop shown in Figure 6. With the flip-flop initially reset, show the resulting waveforms at nodes Q_m (master flip-flop output) and Q_s (slave flip-flop output).

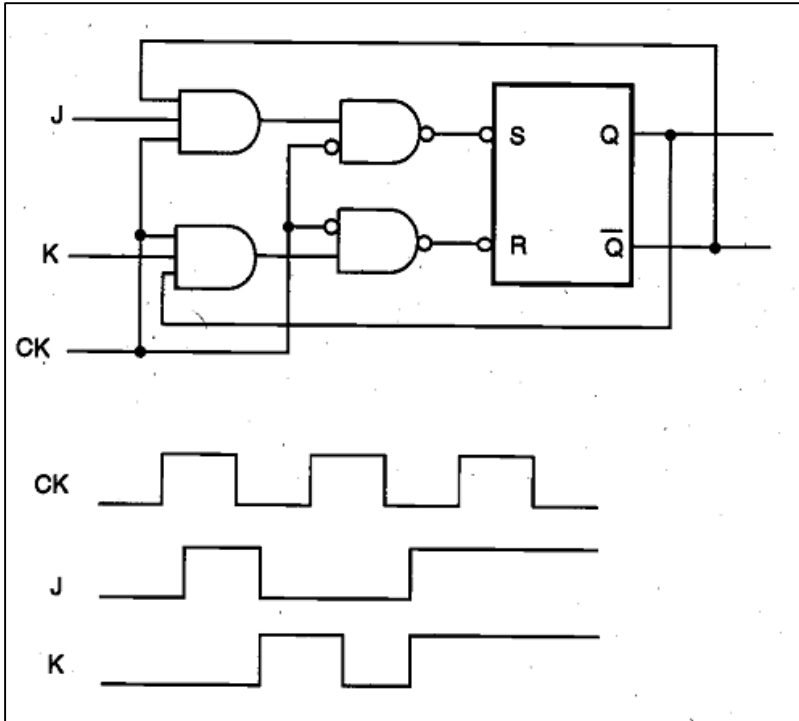


Figure 4

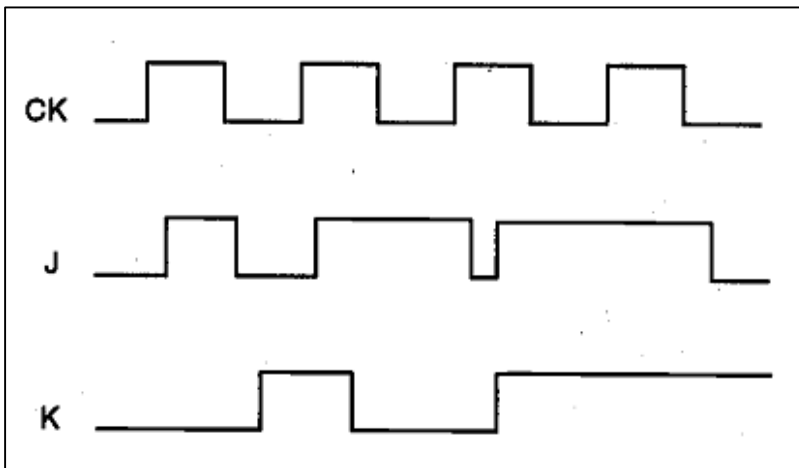


Figure 5

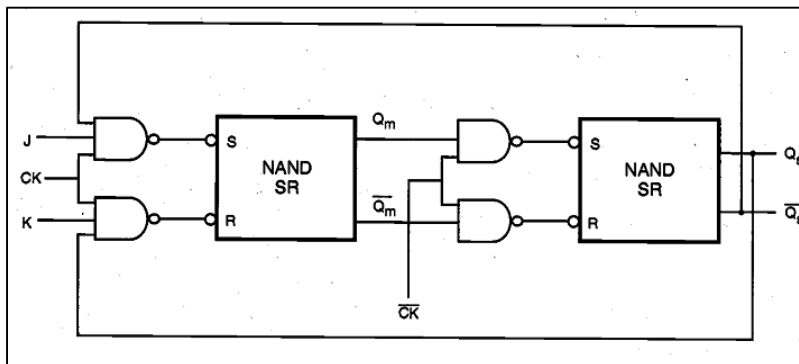


Figure 6