Alexandria University
Faculty of Engineering
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Sheet 3 Combinational MOS Logic Circuits

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1) Calculate the equivalent $\frac{W}{L}$ of the two NMOS with $\frac{W_1}{L}$ and $\frac{W_2}{L}$ connected in series. For simplicity, neglect the body effect, i.e., the threshold voltages of individual transistors are constant and do not depend on the source voltages. Although this is not true in reality, such an assumption is necessary for simple analysis with a reasonably good approximation.

2) Analytical expressions for V_{th} (logic) have been derived in Chapter 7 for the CMOS NOR2 gate. Now consider the CMOS NAND2 gate for the following cases and use $k_p = k_n = 100\ \mu A/V^2$
   - two inputs switching simultaneously
   - top NMOS switching while the bottom NMOS's gate is tied to VDD
   - top NMOS gate is tied to VDD and the gate input of the bottom NMOS is changing.

   a) Derive an analytical expression for V_{th} corresponding to the first case. Also find the V_{th} value for the first case for VDD= V when the magnitudes of the threshold voltages are 1 V with y = 0.
   b) Determine Vth for all three cases by using SPICE.
   c) For C_{load} = 0.2 pF, calculate 50% delays (low-to-high and high-to-low propagation delays) for an ideal pulse input signal for each of the three cases by assuming that C_{load} includes all of the internal parasitic capacitances. Verify the results using SPICE.

3) For the gate shown in Figure 1,

- Pull-up transistor ratio is 5/5
- Pull-down transistor ratios are 100/5
- V_{T0} = 1.0 V
- $\gamma = 0.4\ V^{\frac{1}{2}}$
- $|2\ \emptyset_F|$ = 0.6 V

a) Identify the worst-case input combination(s) for VOL.
b) Calculate the worst-case value of VOL. (Assume that all pull-down transistors have the same body bias and initially, that VOL 5% VDD.)

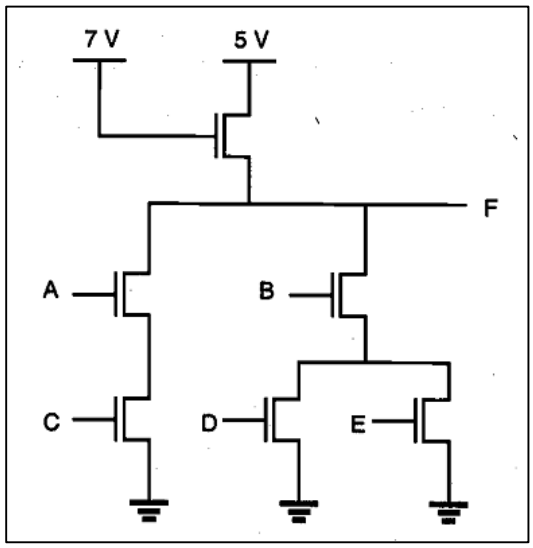

Figure 1

4) Calculate V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L, and NM_H for a two-input NOR gate fabricated with CMOS technology.

- $(W/L)_p$ =4
- $(W/L)_n$ = 1
- V_{Tn} = 0.7 V
- V_{TP} = -0.7 V
- $\mu_n C_{ox}$= 40 µA/V^2
- $\mu_p C_{ox}$ = 20 µA/V^2
- V_{DD} = 5 V

Compare your answers with SPICE simulation results.

5) Consider the circuit shown in Figure 2

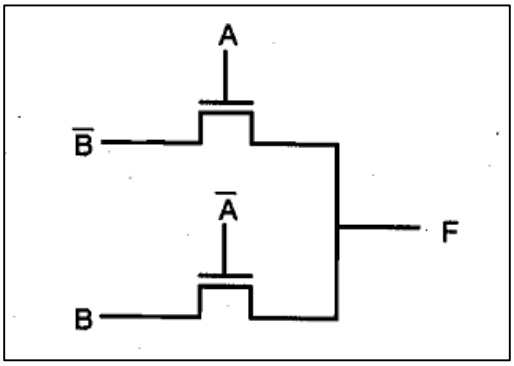

Figure 2

a) Determine the logic function F.
b) Design a circuit to implement the same logic function, but using NOR gates. Draw a transistor-level schematic and use NMOS E-D technology.
c) Design a circuit to implement the same logic function, but use an
d) AOI (AND-OR-INVERT) gate. Draw a transistor-level schematic and use, CMOS technology.

6) Consider a fully complementary CMOS transmission gate with its input terminal tied to ground (0 V) while the other non-gate terminal is tied to a 1 pF load capacitor initially charged to 5 V. At t = 0, both transistors are fully turned on by clock signals to start the discharge of the capacitor.
   - $|V_{T0}| = 1\,V$
   - $\mu_p C_{ox} = 20\ \mu A/V^2$
   - $\mu_n C_{ox} = 50\ \mu A/V^2$

   a) Plot the effective resistance of this transmission gate as a function of capacitor voltage when $(W/L)_p = 50$ and $(W/L)_n = 40$. From the plot find the average value of the resistance. Then calculate the RC delay for the capacitor voltage to change from 5 V to 2.5 V. This can be found by solving the RC-circuit differential equation.

   b) Verify your answer to part (a) by using SPICE simulation. The source/drain parasitic capacitances can be neglected.

7) Design a one-bit full adder circuit and find size of each transistor such that individual gate delay is equivalent to the delay of a reference inverter.

8) Draw the schematic and layout of the logic function *f*

$$f = \overline{(\,ab + cd + e\,)}$$

Assuming all transistors have the same aspect ratio (*W/L*):

- Draw the gate VTC and indicate all important values on it
- Find the gate propagation delay for the following cases:
  - *a=1, b=1 , c=1, d=0, e=0* → *a=0, b=1 , c=1, d=0, e=0*
  - *a=1, b=0 , c=1, d=0, e=0* → *a=1, b=0 , c=1, d=0, e=1*

  Use the same technology parameters as in problem 6 and (W/L) = 0.5µm/0.25µm.
- Find the worst gate fall and rise time

9)

a. Design a 4:1 MUX using two 2:1 MUXs using transmission gates (TGs), and draw its layout.
b. Design a 4:1 MUX directly using transmission gates (TGs), and draw its layout.

10) Find the logic function of the circuit shown in figure 3.

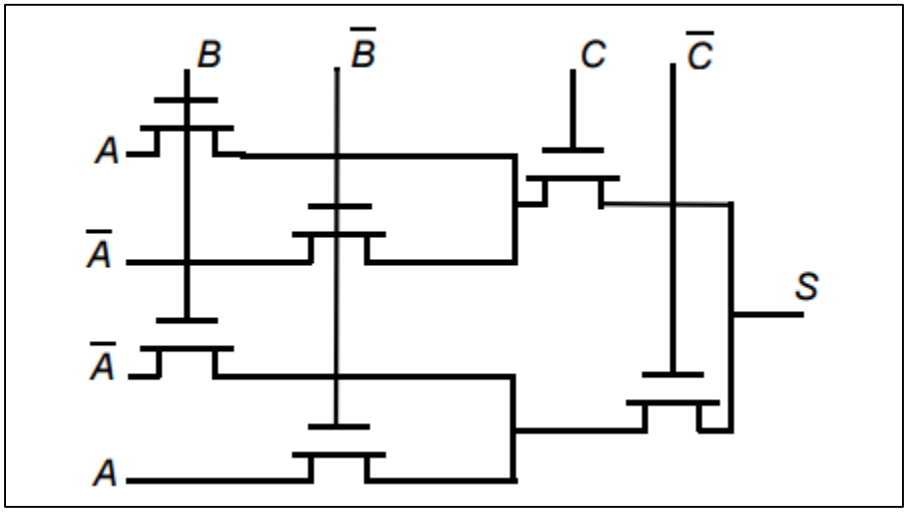

Figure 3

- If A =1, B = 0, find S for different C values.
- If C = 1, B = 0, find S for different A values.
- Calculate the gate output voltage for *A=1, B=0, C=0,* and *A=0, B=1, C=1,* and *A=0, B=0, C=0.* Modify the circuit to work properly for all inputs.
- Calculate the output propagation delay time for *A=1, B=0, C=0,* → *A=0, B=1, C=1.* Use the same technology parameters as in problem 6 and (W/L) = 0.5µm/0.25µm.