Alexandria University
Faculty of Engineering
Electrical Engineering Department

Sheet 2 MOS Dynamic Static Characteristics

---

1) Consider a CMOS ring oscillator consisting of an odd number (n) of identical inverters connected in a ring configuration as shown in figure 1. The layout of the ring oscillator is such that the interconnection (wiring) parasitics can be assumed to be zero. Therefore, the delay of each stage is the same and average delay is called intrinsic delay (τ_p) as long as identical gates are used. The ring oscillator circuit is often used to quote the circuit speed of a particular technology using ring oscillator frequency (f).
    a. Derive an expression for the intrinsic delay (τ_p) in terms of number of stages n.
    b. Show that (τ_p) is independent of the transistor sizing (it remains the same when all gates are scaled uniformly up or down).

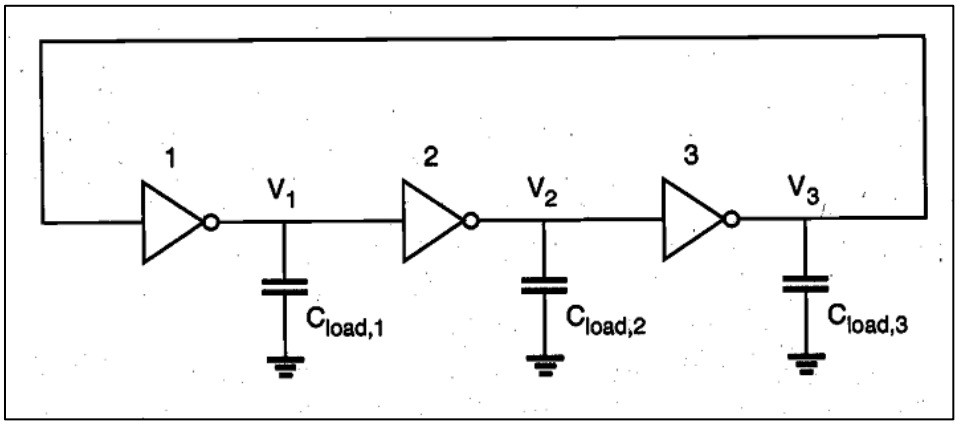

Figure 1 ring oscillator

2) The layout of CMOS inverter shown in figure 2. This inverter is driving another inverter, which is identical to the one shown below except that the transistor widths are three times larger. Calculate τ_{PLH} and τ_{PHL}. Assume that the interconnect capacitance is negligible. The parameters are given as:

V_{TP} =-1.0 V	V_{TN} = 1.0 V
k'_n = 40 µA/V^2	k'_p = 20 µA/V^2
C_{ox} = 69 nF/cm^2	C_{jsW} = 2.2 pF/cm
C_{j0} = 7 nF/cm^2	Φ_0 = 0.86 V
L_D= 1 µm	L_{mask} = 5 µm

The source and drain region length is Y = 12 µm and the channel width is W = 10 µm for both transistors.

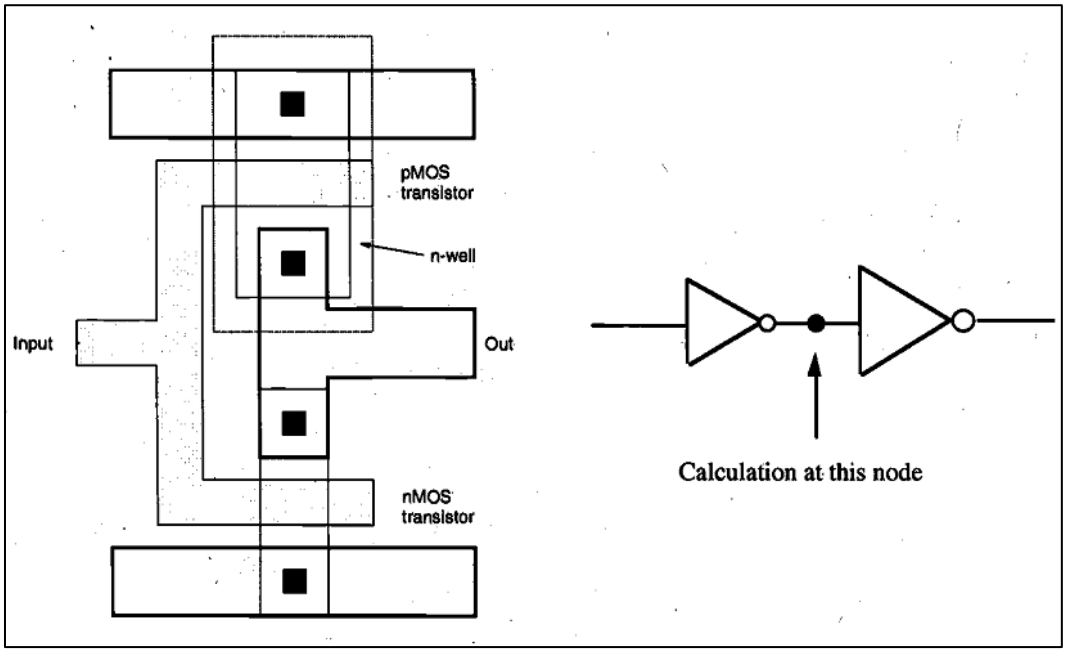

Figure 2 inverter layout

3) Consider a CMOS inverter, with the following device parameters:

NMOS	$V_{T0,n} = 0.8$ V	$\mu_n C_{ox} = 50\ \mu A/V^2$
PMOS	$V_{T0,p} = -1.0$ V	$\mu_p C_{ox} = 20\ \mu A/V^2$

The power supply voltage is $V_{DD} = 5$ V. Both transistors have a channel length of $L_n = L_p = 1$ µm. The total output load capacitance of this circuit is $C_{out} = 2$ pF, which is independent of transistor dimensions.

a. Determine the channel width of the NMOS and the PMOS transistors such that the switching threshold voltage is equal to 2.2 V and the output rise time is $\tau_{rise} = 5$ ns.
b. Calculate the average propagation delay time τ_p for the circuit designed in (a).
c. How do the switching threshold V_{th} and the delay times change if the power supply voltage is dropped from 5 V to 3.3 V. Provide an interpretation of the results.

4) Consider a CMOS inverter with the same process parameters as in Problem 3. The switching threshold is designed to be equal to 2.4 V.

A simplified expression of the total output load capacitance is given as:

$$C_{out} = 500\ fF + C_{db,n} + C_{db,p}$$

Furthermore, we know that the drain-to-substrate parasitic capacitances of the NMOS and the PMOS transistors are functions of the channel width. A set of simplified capacitance expressions are given below.

$$C_{db,n} = 100\ fF + 9\ W_n$$
$$C_{db,P} = 80\ fF + 7\ W_p$$

Where W_n and W_p are expressed in µm.

a. Determine the channel width of both transistors such that the propagation delay τ_{pHL} is smaller than 0.825 ns.

b. Assume now that the CMOS inverter has been designed with $(W/L)_n = 6$ and $(W/L)_p = 15$, and that the total output load capacitance is 250 fF. Calculate the output rise time and fall time using the average current method.

5) Consider a CMOS inverter with the following parameters:

NMOS	$V_{T0,n} = 1.0$ V	$\mu_n C_{ox} = 45\ \mu A/V^2$	$(W/L)_n = 10$
PMOS	$V_{T0,p} = -1.2$ V	$\mu_p C_{ox} = 25\ \mu A/V^2$	$(W/L)_p = 20$

The power supply voltage is 5 V, and the output load capacitance is 1.5 pF.

a. Calculate the rise time and the fall time of the output signal using
   i. exact method (differential equations)
   ii. average current method
b. Determine the maximum frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0 V to 5 V in each cycle.
c. Calculate the dynamic power dissipation at this frequency.
d. Assume that the output load capacitance is mainly dominated by fixed fanout components (which are independent of W_n and W_p). We want to re-design the inverter so that the propagation delay times are reduced by 25%.
   Determine the required channel dimensions of the NMOS and the PMOS transistors. How does this re-design influence the switching (inversion) threshold?