Alexandria University
Faculty of Engineering
Electrical Engineering Department

Sheet 1 MOS Inverter Static Characteristics

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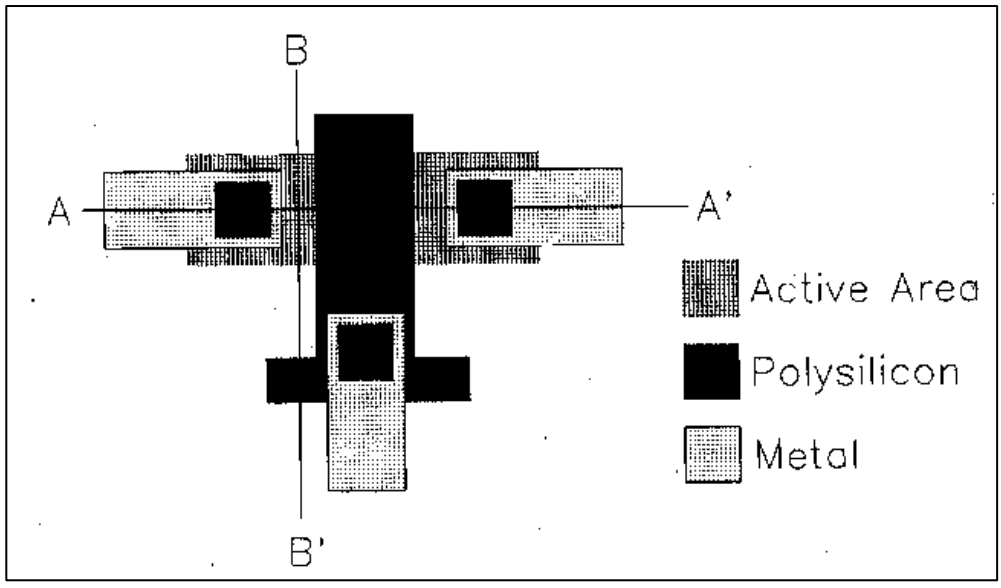
1) Draw cross-sections of the following device along the lines A - A' and B – B'.



2) Consider CMOS inverter with the following parameters:

NMOS	$V_{T0,n} = 0.6$ V	$\mu_n C_{ox} = 60\ \mu A/V^2$	$(W/L)_n = 8$
PMOS	$V_{T0,p} = 0.7$ V	$\mu_p C_{ox} = 25\ \mu A/V^2$	$(W/L)_p = 12$

Calculate the noise margins and the switching threshold (V_{th}) of this circuit. The power supply is $V_{DD} = 3.3$ V.

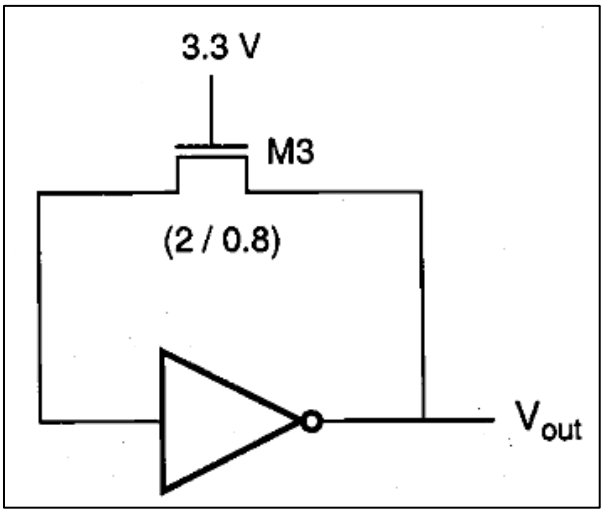
3) Design of a CMOS inverter circuit:

Use the same device parameters as in problem 2.
The power supply V_{DD} = 3.3 V. The channel length of both transistors is $L_n = L_p$ = 0.8 μm.

a) Determine the (W_n /W_p) ratio so that the switching (inversion) threshold voltage of the circuit is V_{th} = 1.4 V.

b) The CMOS fabrication process used to manufacture this inverter allows a variation of the $V_{T0,n}$ value by ±15% around its normal value, and a variation of the $V_{T0,p}$ value by ±20% around its normal value. Assuming that all other parameters (such as μ_n, μ_p, C_{ox}, W_n ,W_p) always retain their nominal values, find the upper and lower limits of the switching threshold voltage (V_{th}) of this circuit.

4) Consider the CMOS inverter designed in problem 3, with the following circuit configuration



a) Calculate the output voltage level V_{out}.

b) Determine if the process-related variation of $V_{T0,n}$ of M3 has any influence upon the voltage V_{out}.

c) Calculate the total current being drawn from the power supply source, and determine its variation due to process-related threshold voltage variations.

5) Consider a CMOS inverter, with the following device parameters:

NMOS	$V_{T0,n} = 0.6$ V	$\mu_n C_{ox} = 60\ \mu A/V^2$
PMOS	$V_{T0,p} = -0.8$ V	$\mu_p C_{ox} = 20\ \mu A/V^2$

Also: $V_{DD} = 3$ $\lambda = 0$

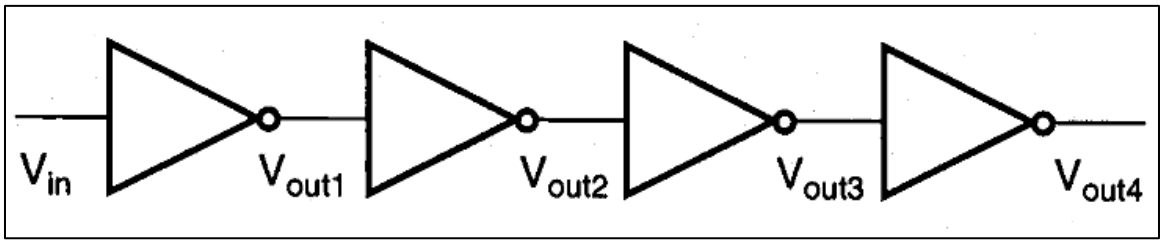
a) Determine the (W/L) ratios of the NMOS and the PMOS transistor such that the switching threshold is $V_{th} = 1.5$ V.

b) Plot the VTC of the CMOS inverter using SPICE.

c) Determine the VTC of the inverter for $\lambda = 0.05$ and $\lambda = 0.1\ V^{-1}$.

d) Discuss how the noise margins are influenced by non-zero λ value. Note that transistors with very short channel lengths tend to have larger λ values than long-channel transistors.

6) Consider the CMOS inverter designed in problem 5 above, with $\lambda = 0.1\ V^{-1}$. Now consider a cascade connection of four identical inverters, as shown.



a) If the input voltage is $V_{in} = 1.55$ V, find V_{out1}, V_{out2}, V_{out3} and V_{out4}.

(note that this requires solving KCL equations for each subsequent stage, using the non-zero λ value).

b) How many stages are necessary to restore a true logic output level?

c) Verify your result with SPICE simulation.