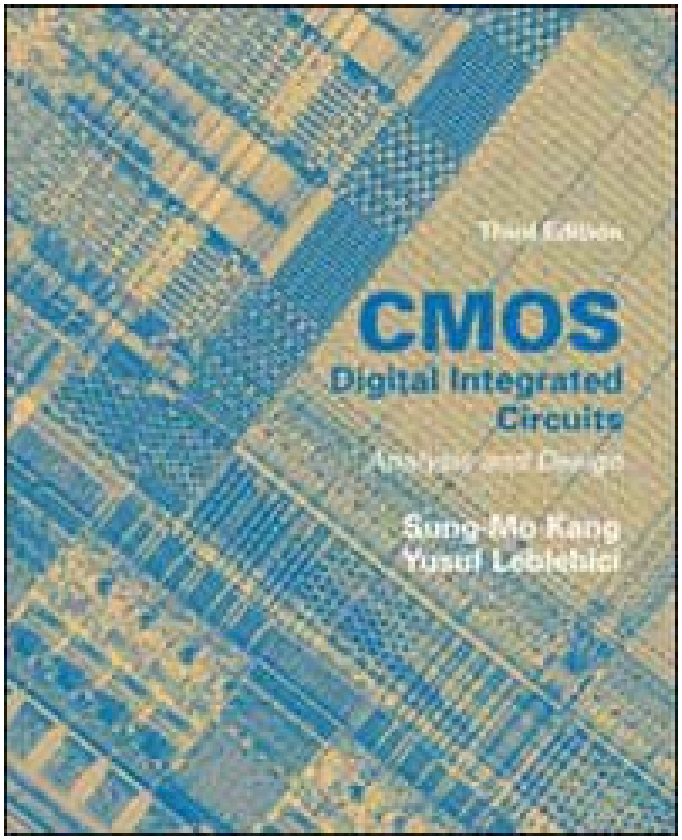
Digital IC Design and Architecture



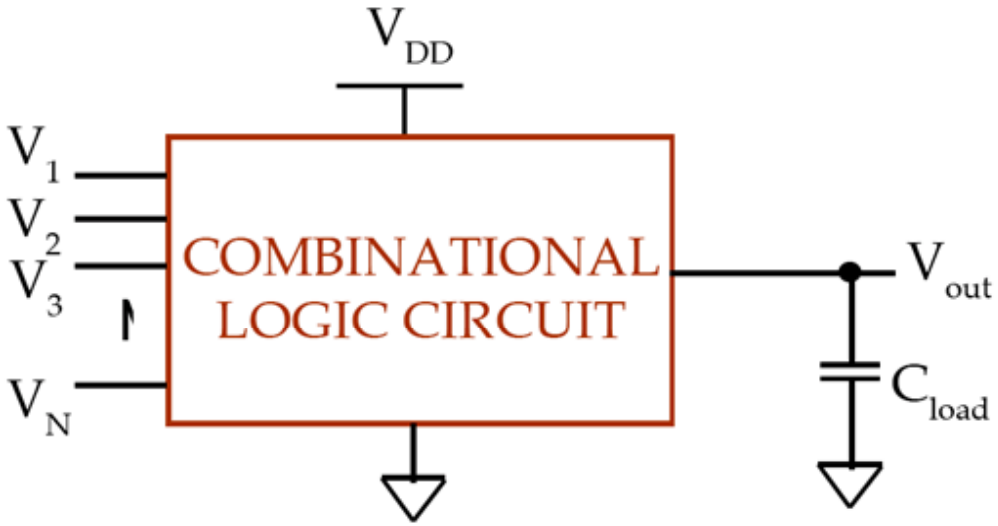
Combinational Logic and Circuits

Static CMOS Circuit

At every point in time (except during the switching transients) each gate output is connected to either V_{DD} or V_{ss} via a low-resistive path.

The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

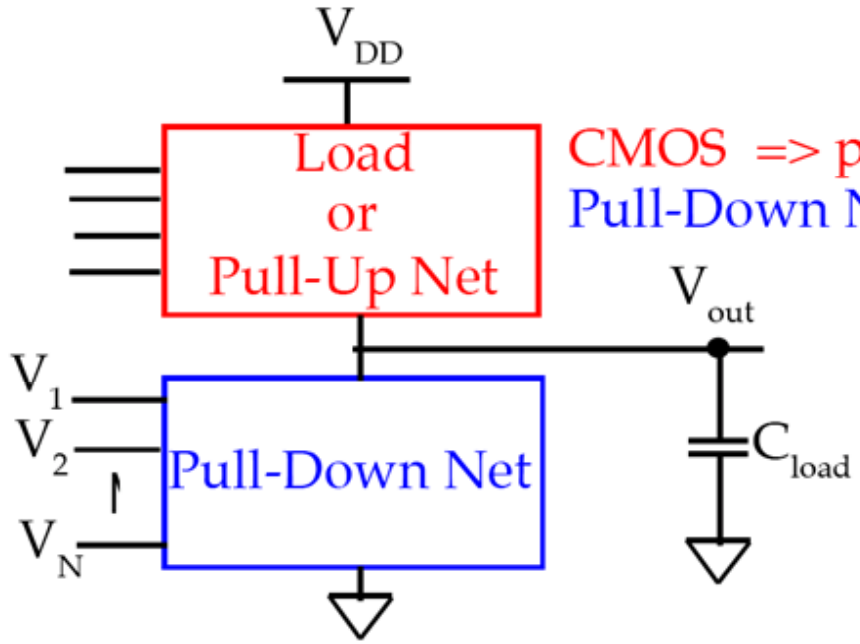
This is in contrast to the dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.



V_{out} is Boolean function of inputs , V_1, V_2, V_3, ..., V_N.

"1" => V_{DD}

"0" => 0

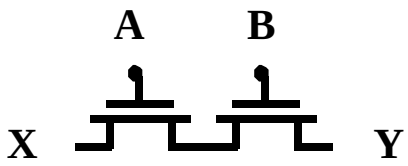


CMOS => pMOS Net complement of Pull-Down Net

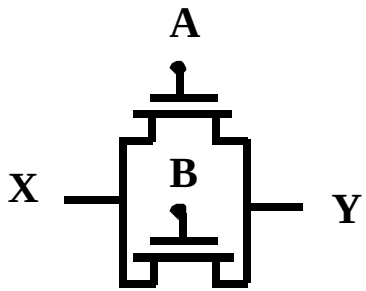
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

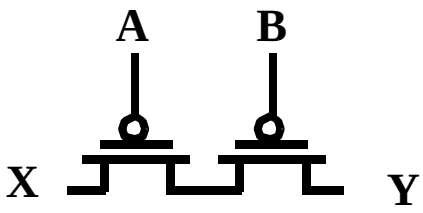


Y = X if A OR B

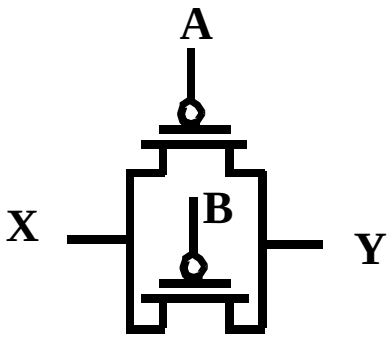
NMOS Transistors pass a "strong" 0 but a "weak" 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



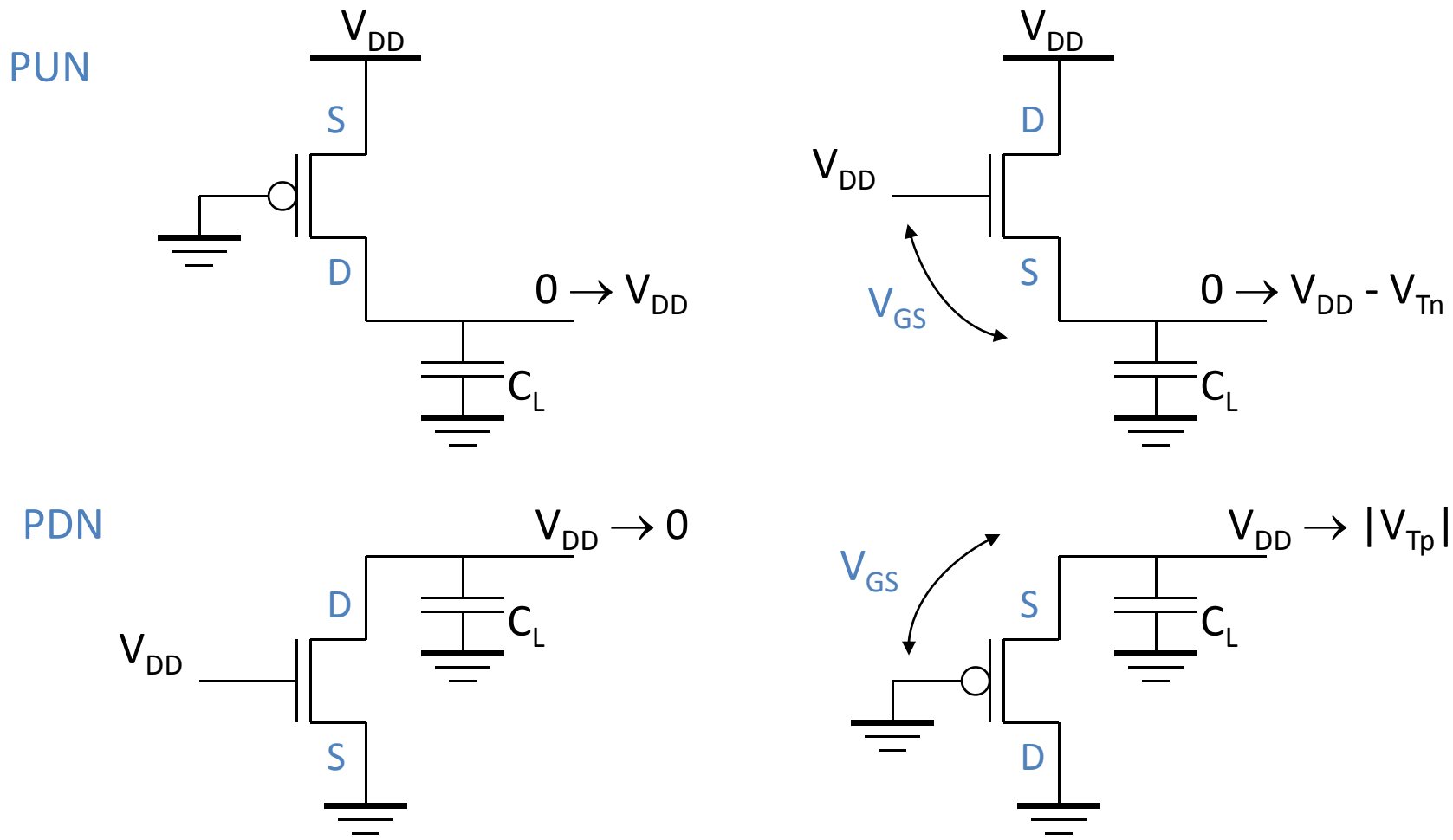
Y = X if $\overline{A}$ AND $\overline{B}$ = $\overline{A + B}$



Y = X if $\overline{A}$ OR $\overline{B}$ = $\overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

Threshold Drops



Complementary CMOS Logic Style

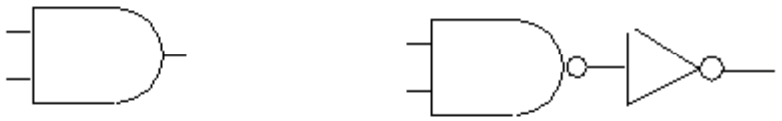
- **PUP is the DUAL of PDN**

  (can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

- **The complementary gate is inverting**

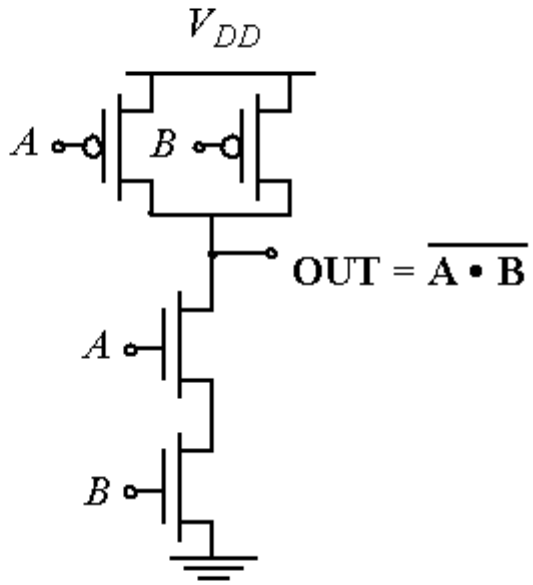


AND = NAND + INV

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: G = A B $\Rightarrow$ Conduction to GND

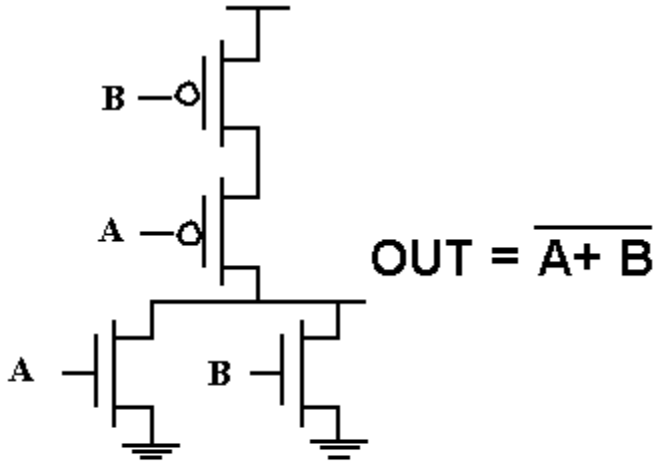
PUN: F= $\overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

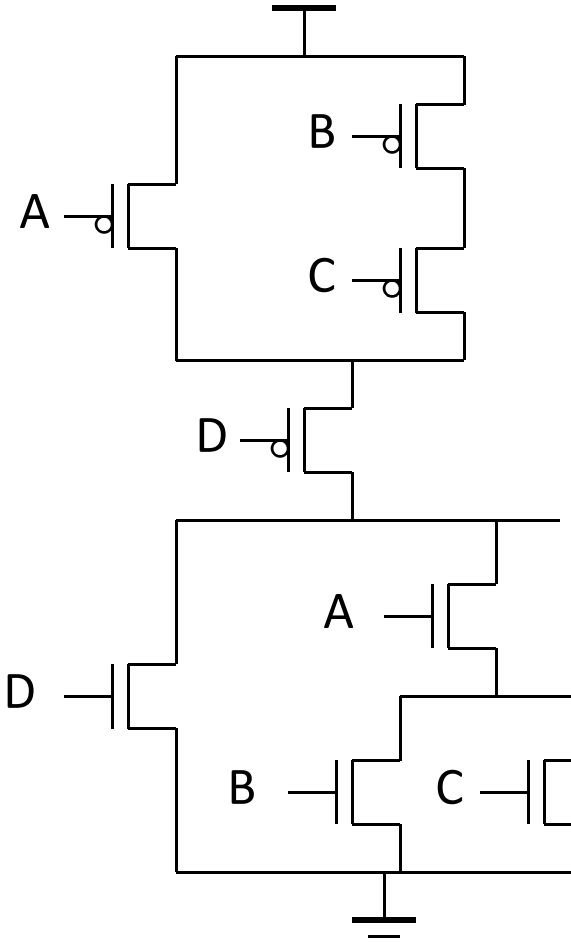
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



Complex CMOS Gate



$$\overline{OUT = D + A \bullet (B + C)}$$

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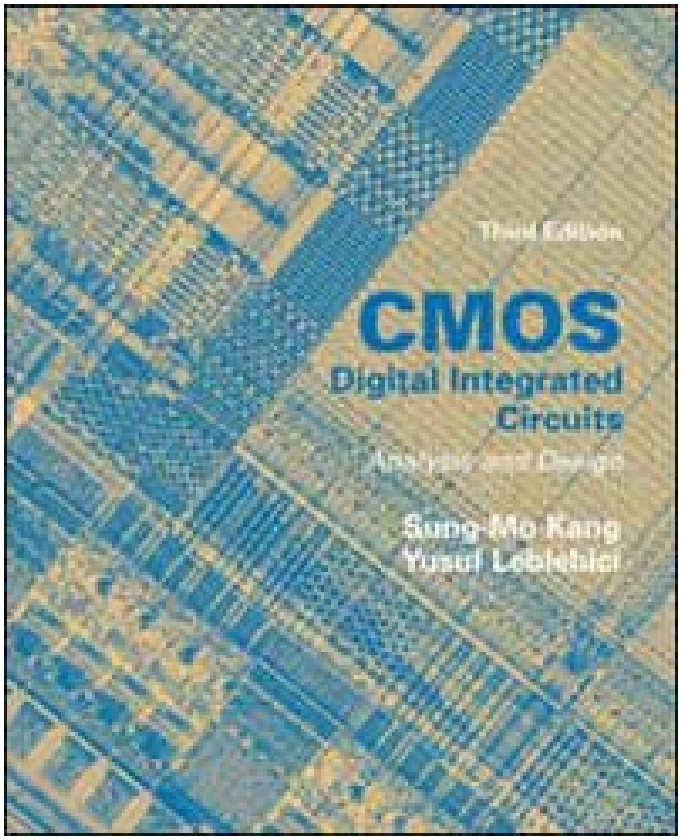
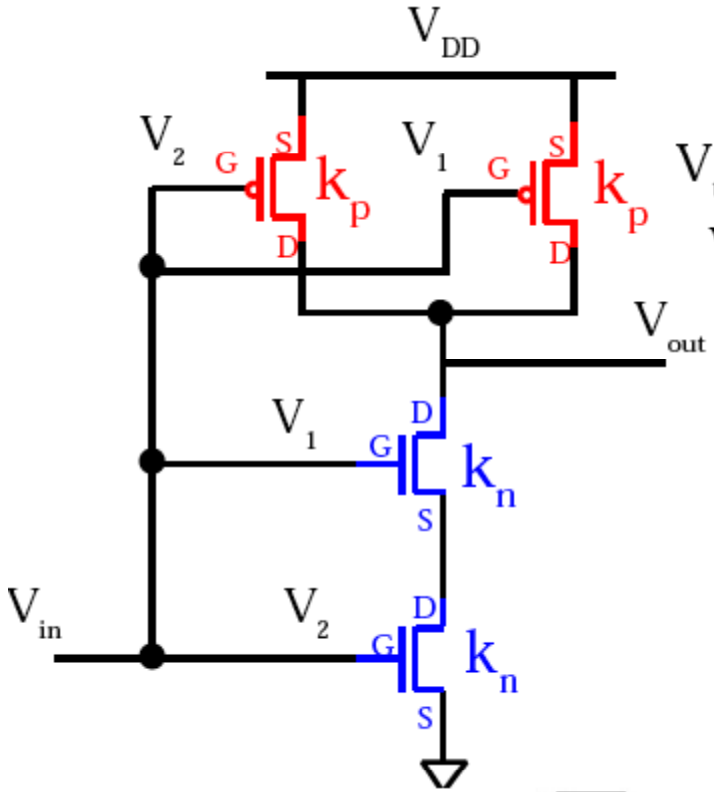


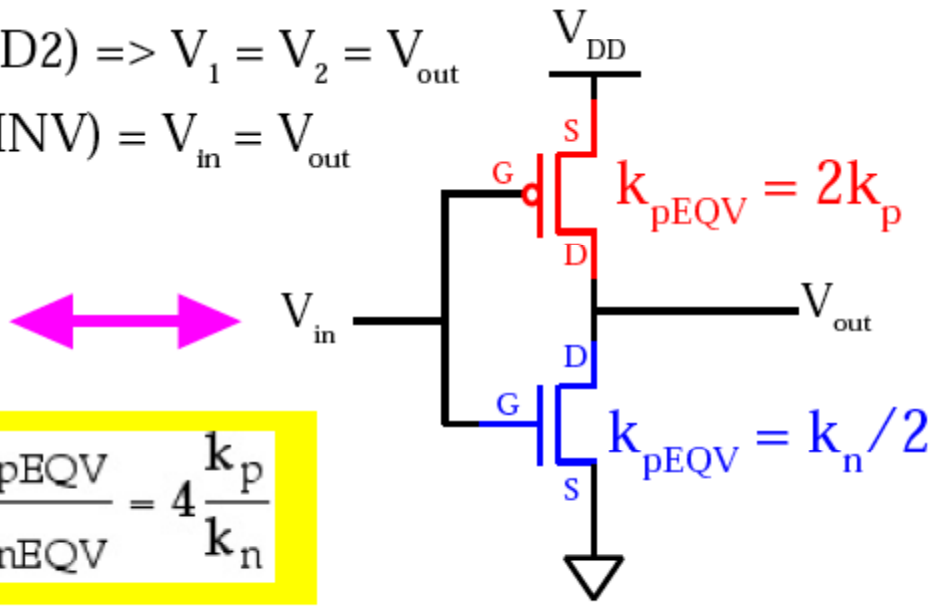
Combinational Logic: CMOS Implementation

CMOS ND2



$V_{th}(ND2) => V_1 = V_2 = V_{out}$

$V_{th}(INV) = V_{in} = V_{out}$



$$\frac{k_{pEQV}}{k_{nEQV}} = 4\frac{k_p}{k_n}$$

$$V_{th}(NAND2) = \frac{V_{Tn} + 2\sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + 2\sqrt{\frac{k_p}{k_n}}}$$

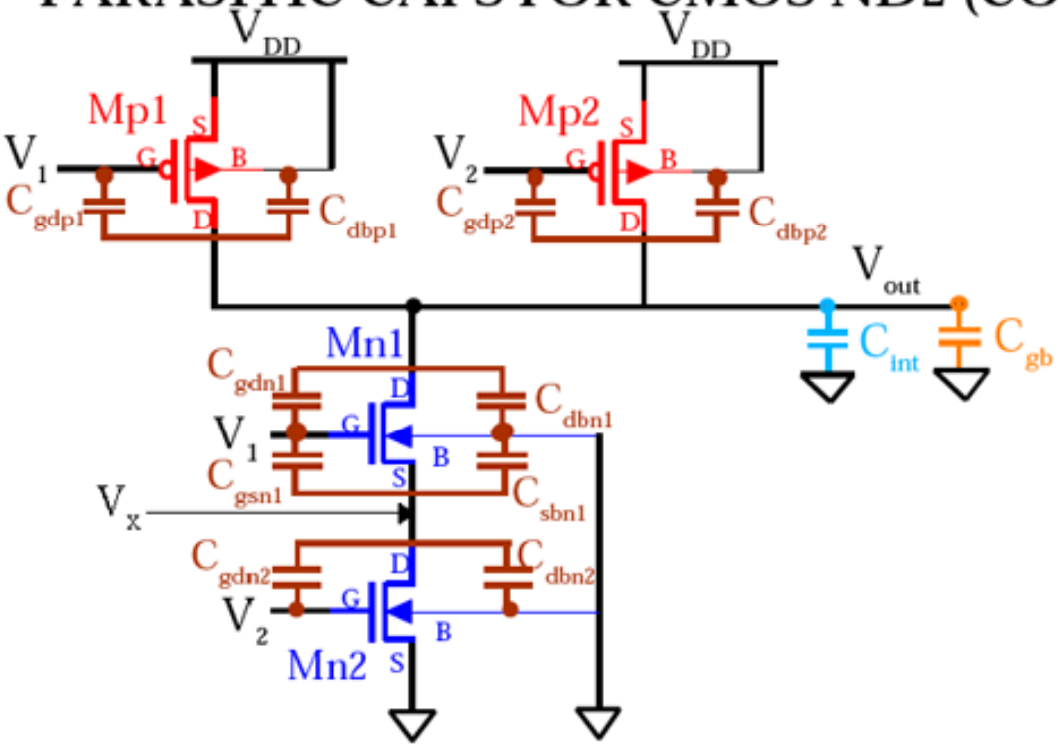
$$V_{th}(INV) = \frac{V_{Tn} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$

Symmetrical EQUIV INV

$k_{pEQV} = k_{nEQV}$ and $V_{Tn} = |V_{Tp}| => V_{th}(INV) = V_{DD}/2$

$V_{th}(ND2) = V_{DD}/2 => k_n = 4k_p$

PARASITIC CAPS FOR CMOS ND2 (CONSERVATIVE)



$C_{gdn1} = C_{gdn2} = C_{gdn}$
$C_{dbn1} = C_{dbn2} = C_{dbn}$
$C_{gdp1} = C_{gdp2} = C_{gdp}$
$C_{dbp1} = C_{dbp2} = C_{dbp}$
$C_{gsp1} = C_{gsp2} = C_{gsp}$
$C_{sbp1} = C_{sbp2} = C_{sbp}$

WORST CASE for PULL-UP => $V_1 = V_{DD}$, $V_2 = V_{DD}$ -> 0 & V_x = low -> high

$C_{load\text{-}ND2} \approx 2C_{dbn} + C_{sbn} + 2C_{dbp} + C_{int} + C_{gb} = 3C_{dbn} + 2C_{dbp} + C_{int} + C_{gb}$

WORST CASE for PULL-DOWN => $V_1 = V_{DD}$, $V_2 = 0$ -> V_{DD} & V_x = high -> low

$C_{load\text{-}ND2} \approx 2C_{dbn} + C_{sbn} + 2C_{dbp} + C_{int} + C_{gb} = 3C_{dbn} + 2C_{dbp} + C_{int} + C_{gb}$

NDn: $C_{load\text{-}ND2} \approx (2n-1)C_{dbn} + nC_{dbp} + C_{int} + C_{gb}$

CMOS ND DESIGN STRATEGIES

ND2:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

$$V_{th}(ND2) = V_{DD}/2 \Rightarrow k_n = 4k_p$$

2. Propogation delay τ_{PHL} or τ_{PLH}:

$$\tau_{PHL-ND2} \approx \frac{C_{load-ND2}}{k_n/2}\left[\frac{2V_{T0n}}{V_{DD}-V_{T0n}} + \ln\left(\frac{4(V_{DD}-V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH-ND2} \approx \frac{C_{load-ND2}}{2k_p}\left[\frac{2|V_{T0p}|}{V_{DD}-|V_{T0p}|} + \ln\left(\frac{4(V_{DD}-|V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

NDn:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

$$V_{th}(NDn) = V_{DD}/2 \Rightarrow k_n = n^2 k_p$$

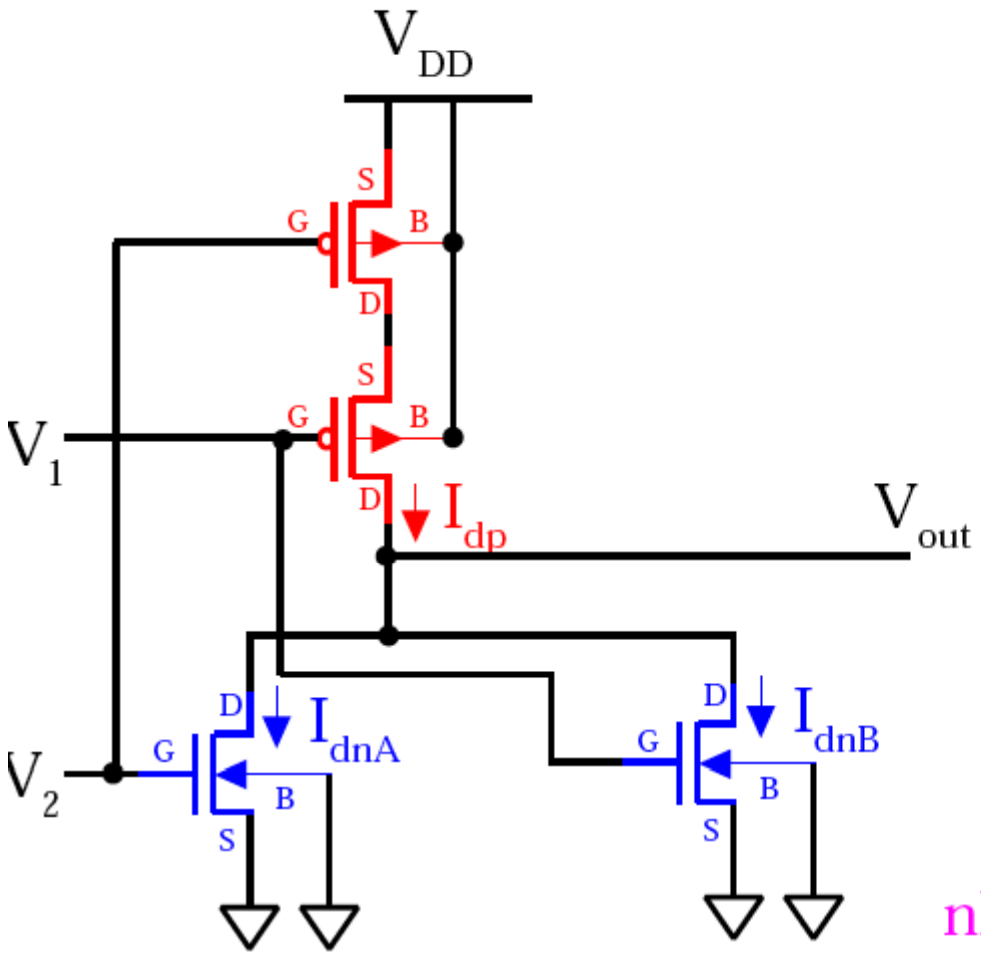
2. Propogation delay τ_{PHL} or τ_{PLH}:

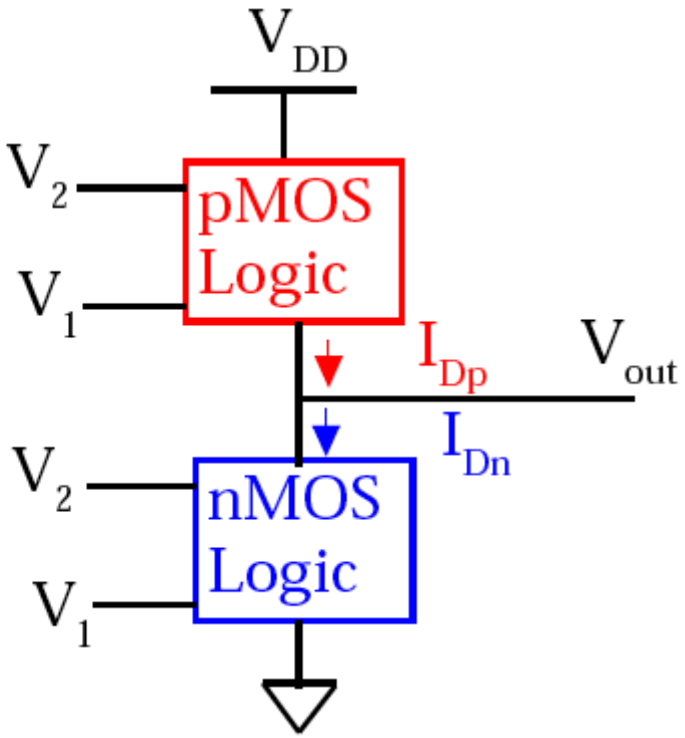
$$\tau_{PHL-NDn} \approx \frac{C_{load-NDn}}{k_n/n}\left[\frac{2V_{T0n}}{V_{DD}-V_{T0n}} + \ln\left(\frac{4(V_{DD}-V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH-NDn} \approx \frac{C_{load-NDn}}{nk_p}\left[\frac{2|V_{T0p}|}{V_{DD}-|V_{T0p}|} + \ln\left(\frac{4(V_{DD}-|V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

CMOS LOGIC GATES

2-INPUT NOR (NR2)



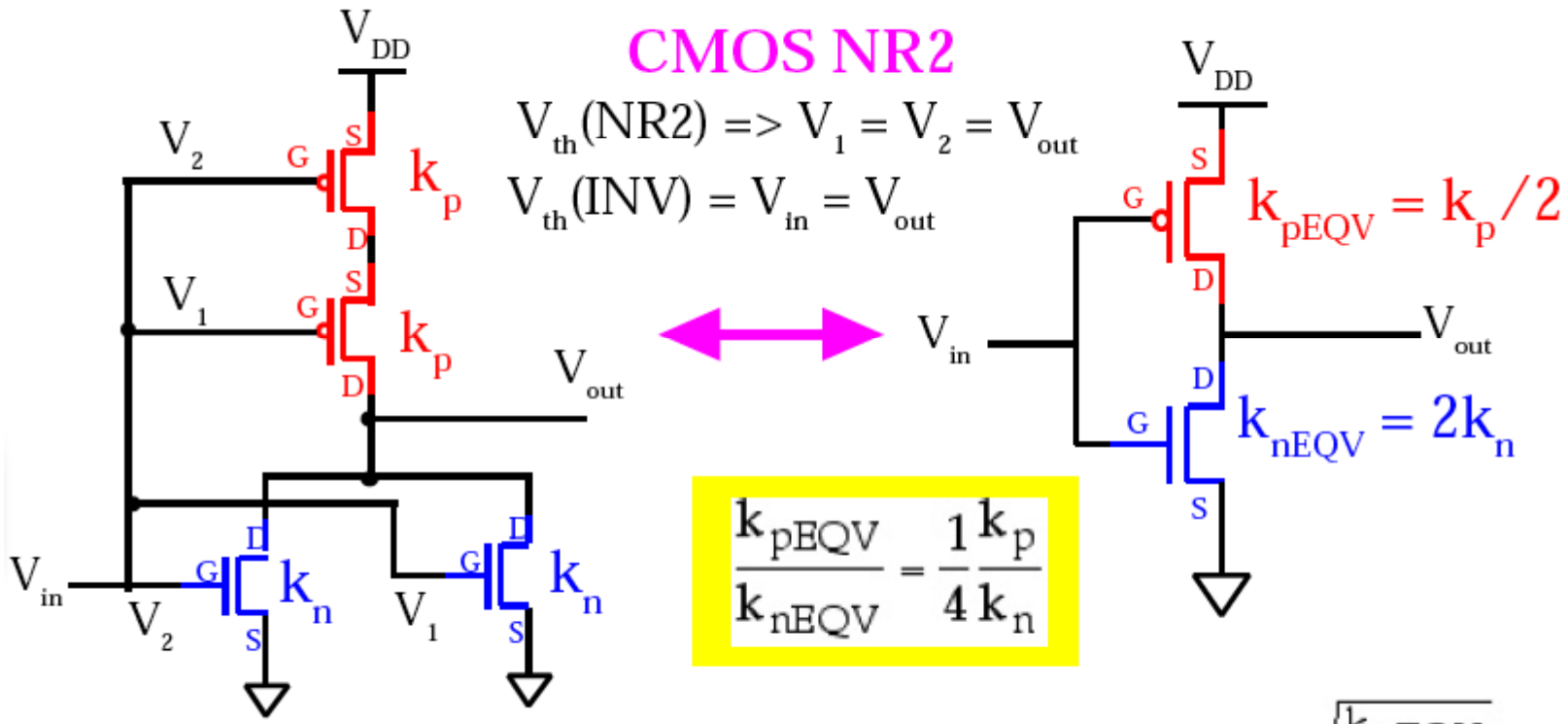


nMOS Net ON, pMOS Net OFF
or
nMOS Net OFF, pMOS Net ON

CMOS NR2

$V_{th}(NR2) => V_1 = V_2 = V_{out}$

$V_{th}(INV) = V_{in} = V_{out}$



$$\frac{k_{pEQV}}{k_{nEQV}} = \frac{1}{4}\frac{k_p}{k_n}$$

$$V_{th}(NOR2) = \frac{V_{Tn} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}}$$

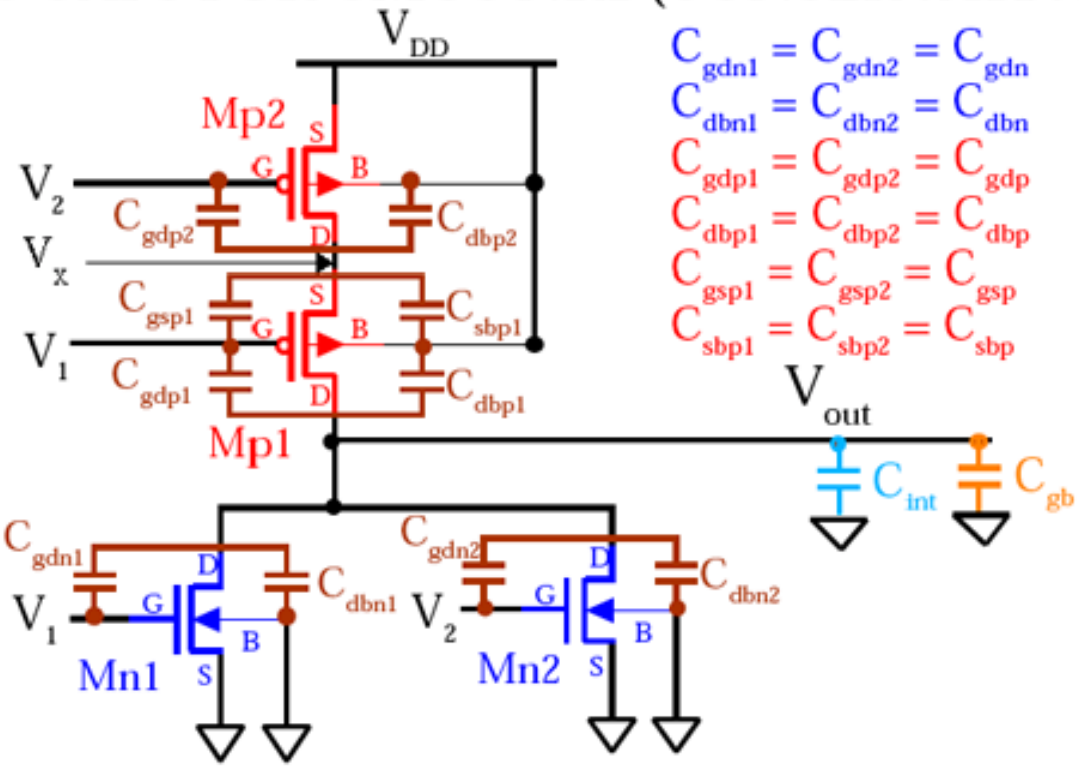
$$V_{th}(INV) = \frac{V_{Tn} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$

Symmetrical EQUIV INV

$k_{pEQV} = k_{nEQV}$ or $k_{pEQV}/k_{nEQV} = 1$ and $V_{Tn} = |V_{Tp}| => V_{th}(INV) = V_{DD}/2$

$V_{th}(NR2) = V_{DD}/2 => k_p = 4k_n$

PARASITIC CAPS FOR CMOS NR2 (CONSERVATIVE)



$C_{gdn1} = C_{gdn2} = C_{gdn}$
$C_{dbn1} = C_{dbn2} = C_{dbn}$
$C_{gdp1} = C_{gdp2} = C_{gdp}$
$C_{dbp1} = C_{dbp2} = C_{dbp}$
$C_{gsp1} = C_{gsp2} = C_{gsp}$
$C_{sbp1} = C_{sbp2} = C_{sbp}$

WORST CASE for PULL-UP => $V_1 = 0$, $V_2 = V_{DD}$ -> 0 & V_x = low -> high

$C_{load\text{-}NR2} \approx 2C_{dbn} + 2C_{dbp} + C_{sbp} + C_{int} + C_{gb} = 2C_{dbn} + 3C_{dbp} + C_{int} + C_{gb}$

WORST CASE for PULL-DOWN => $V_1 = 0$, $V_2 = 0$ -> V_{DD} & V_x = high -> low

$C_{load\text{-}NR2} \approx 2C_{dbn} + 2C_{dbp} + C_{sbp} + C_{int} + C_{gb} = 2C_{dbn} + 3C_{dbp} + C_{int} + C_{gb}$

NRn: $C_{load\text{-}NR2} \approx nC_{dbn} + (2n-1)C_{dbp} + C_{int} + C_{gb}$

CMOS NR DESIGN STRATEGIES

NR2:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

$$V_{th}(NR2) = V_{DD}/2 \Rightarrow k_p = 4k_n$$

2. Propogation delay τ_{PHL} or τ_{PLH}:

$$\tau_{PHL-NR2} \approx \frac{C_{load-NR2}}{2k_n}\left[\frac{2V_{T0n}}{V_{DD}-V_{T0n}} + \ln\left(\frac{4(V_{DD}-V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH-NR2} \approx \frac{C_{load-NR2}}{k_p/2}\left[\frac{2|V_{T0p}|}{V_{DD}-|V_{T0p}|} + \ln\left(\frac{4(V_{DD}-|V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

NRn:

1. Symmetric Inverter $V_{th} = V_{DD}/2$:

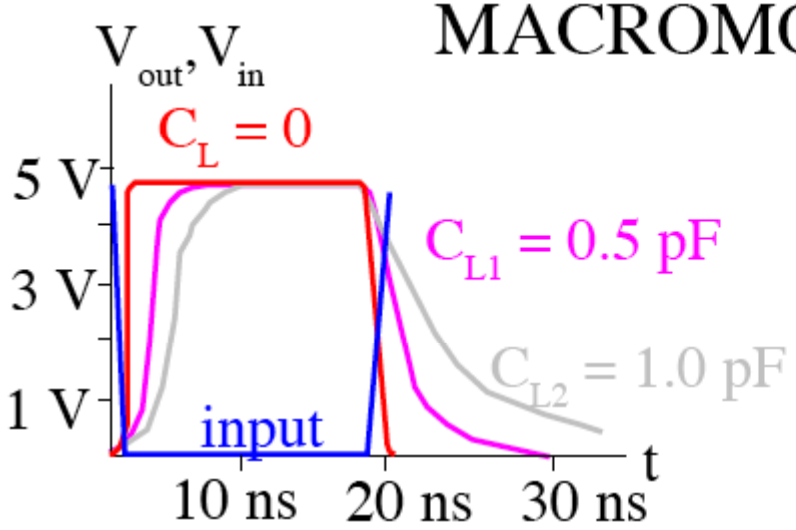
$$V_{th}(NRn) = V_{DD}/2 \Rightarrow k_p = n^2 k_n$$

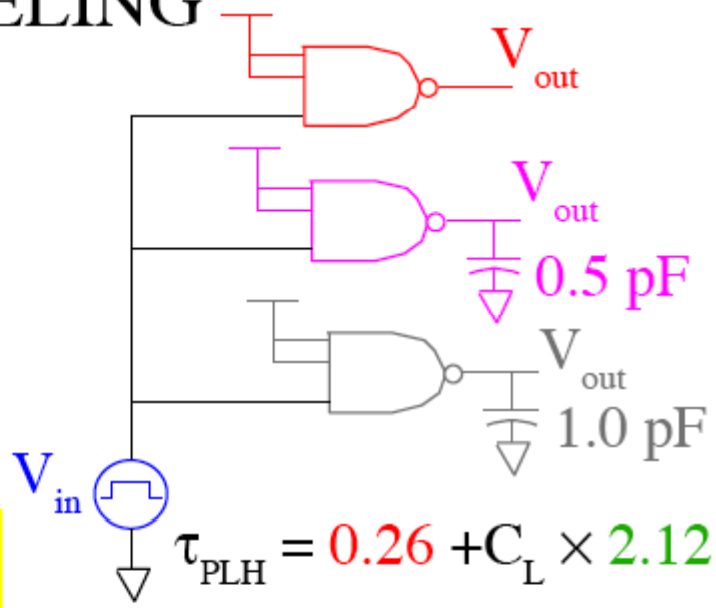
2. Propogation delay τ_{PHL} or τ_{PLH}:

$$\tau_{PHL-NRn} \approx \frac{C_{load-NRn}}{nk_n}\left[\frac{2V_{T0n}}{V_{DD}-V_{T0n}} + \ln\left(\frac{4(V_{DD}-V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH-NRn} \approx \frac{C_{load-NRn}}{k_p/n}\left[\frac{2|V_{T0p}|}{V_{DD}-|V_{T0p}|} + \ln\left(\frac{4(V_{DD}-|V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

MACROMODELING



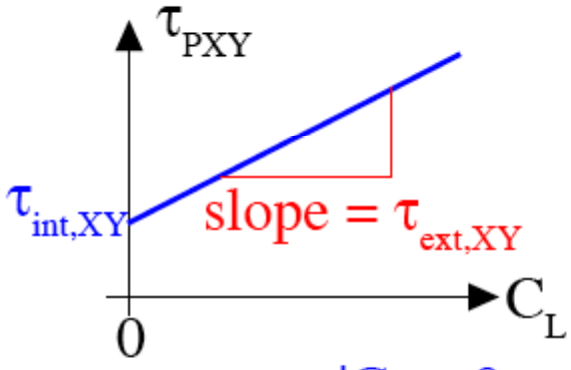


$$\tau_{PLH} = \tau_{int,LH} + [(C_{L2} - C_{L1})/C_{L2}] \times \tau_{ext,LH}$$

$$\tau_{PHL} = \tau_{int,HL} + [(C_{L2} - C_{L1})/C_{L2}] \times \tau_{ext,HL}$$

$$\tau_{PLH} = 0.26 + C_L \times 2.12 \text{ ns}$$

$$\tau_{PHL} = 0.42 + C_L \times 3.88 \text{ ns}$$



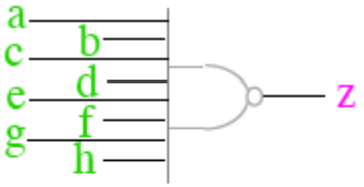
$$\tau_{int,XY} = \tau_{PXY} | C_L = 0$$

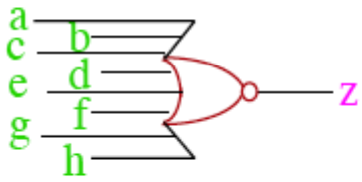
	Load Conditions		
Time	$C_L = 0$	$C_L = 0.5$ pF	$C_L = 1.0$ pF
τ_{PLH} (ns)	0.26	1.32	2.38
τ_{PHL} (ns)	0.42	2.36	4.30
$\tau_{ext,LH}$ (ns/pF)	0	2.12	2.12
$\tau_{ext,HL}$ (ns/pF)	0	3.88	3.88

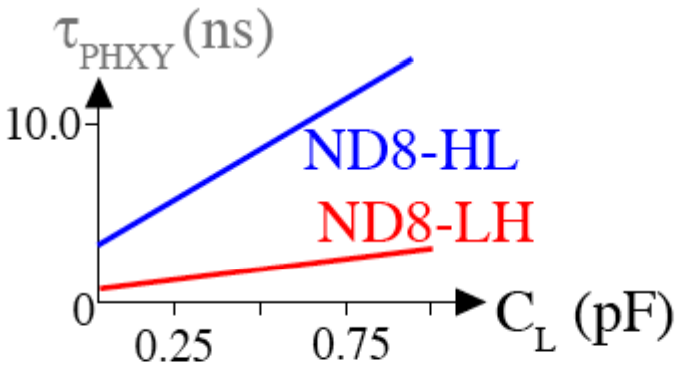
TYPICAL CMOS NAND AND NOR DELAYS

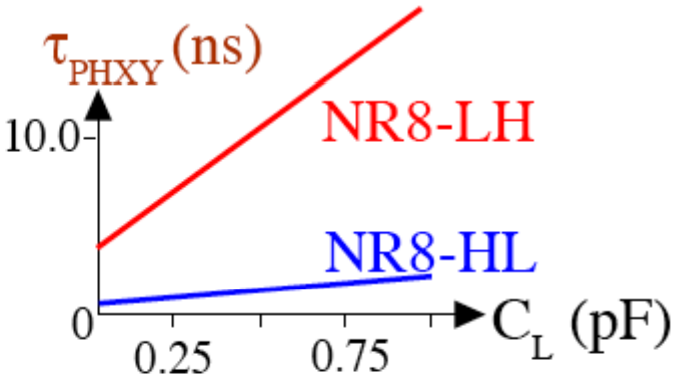
Delays for a Family of NAND & NOR gates

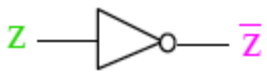
1. $W_n = 6.4\ \mu m$, $L_n = 1\ \mu m$, and $W_p = 12.8\ \mu m$, $L_p = 1\ \mu m$.
2. $t_{input\text{-}rise/fall} = 0.1$ ns and $C_{load} = 0 \rightarrow 1$ pF.

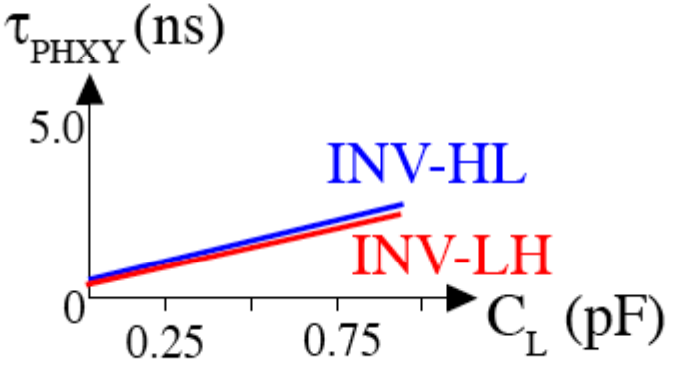


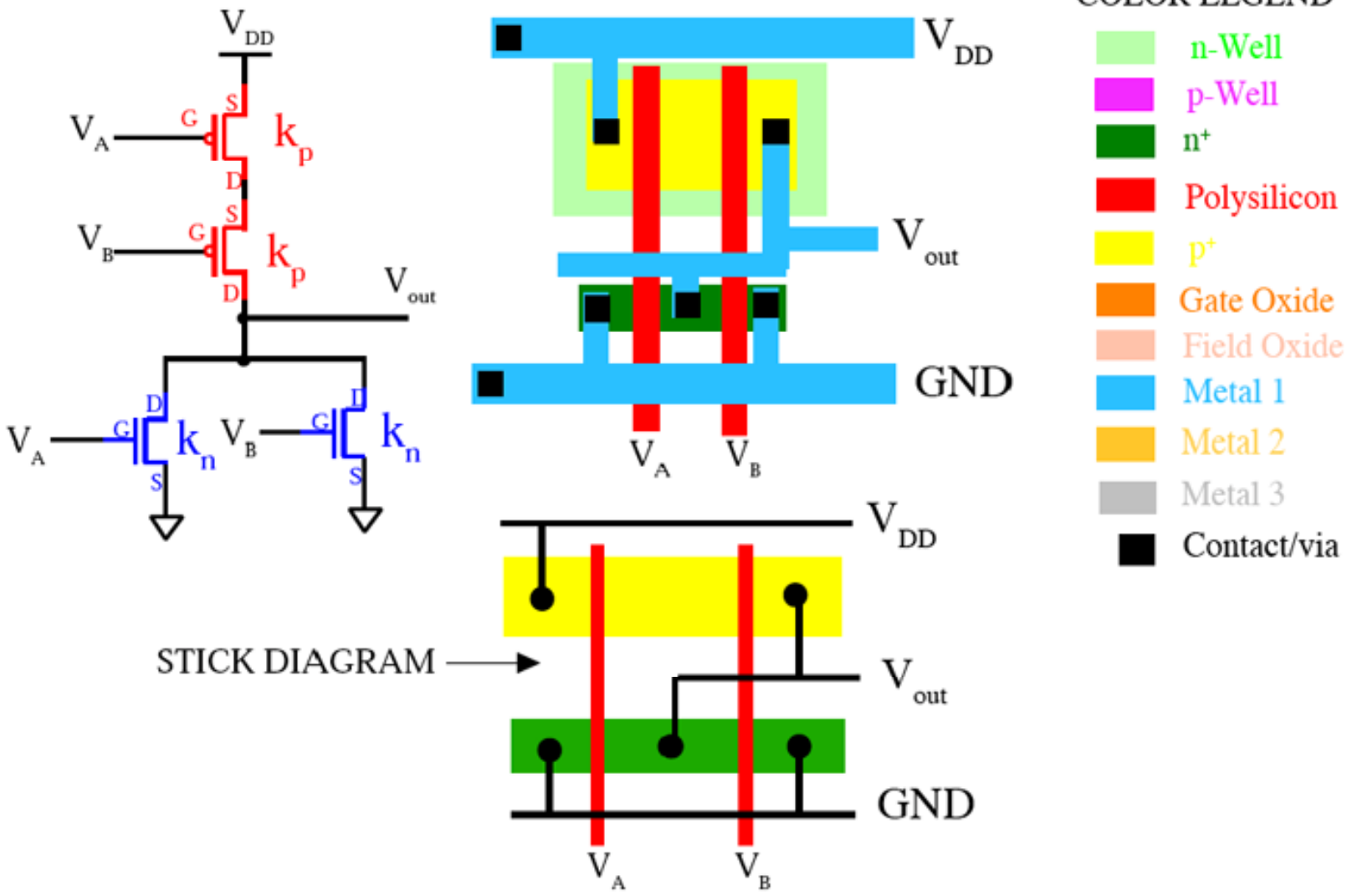


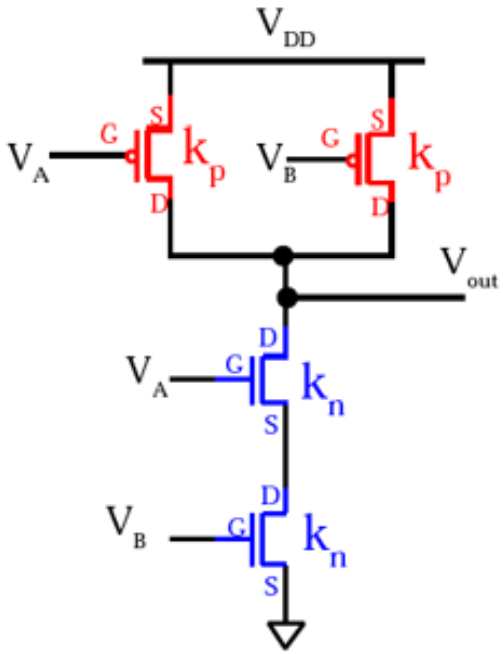


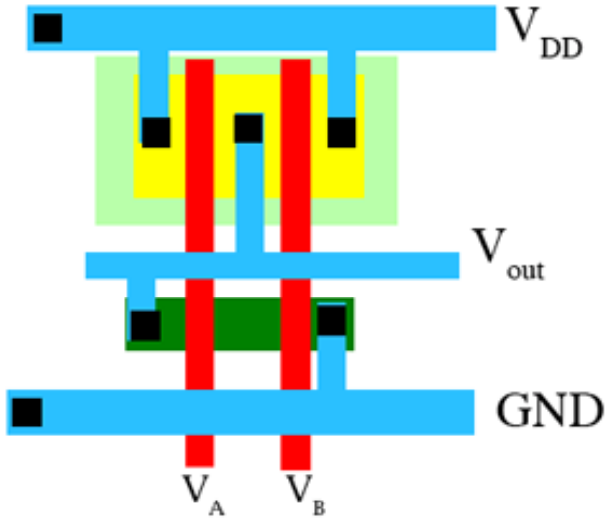







V_DD
V_A
G
S
k_p
D
V_B
G
S
k_p
D
V_out
D
V_A
G
k_n
V_B
G
k_n
S
S
V_DD
V_out
GND
V_A
V_B
STICK DIAGRAM
V_DD
V_out
GND
V_A
V_B
COLOR LEGEND
n-Well
p-Well
n+
Polysilicon
p+
Gate Oxide
Field Oxide
Metal 1
Metal 2
Metal 3
Contact/via





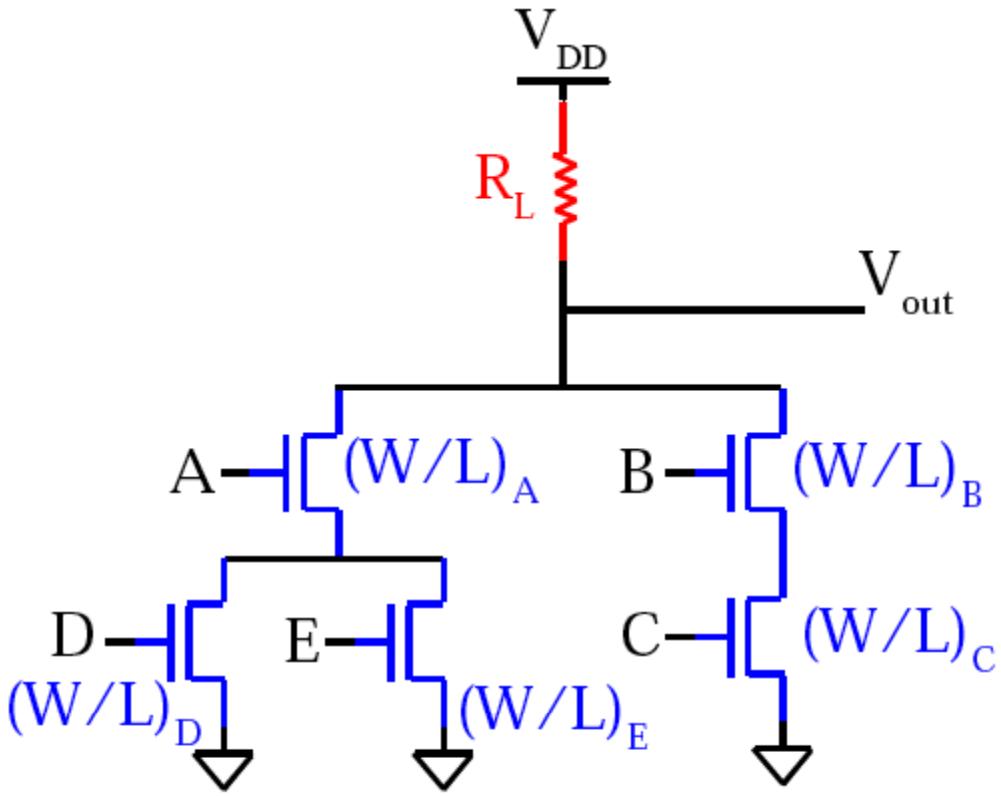
COLOR LEGEND 30

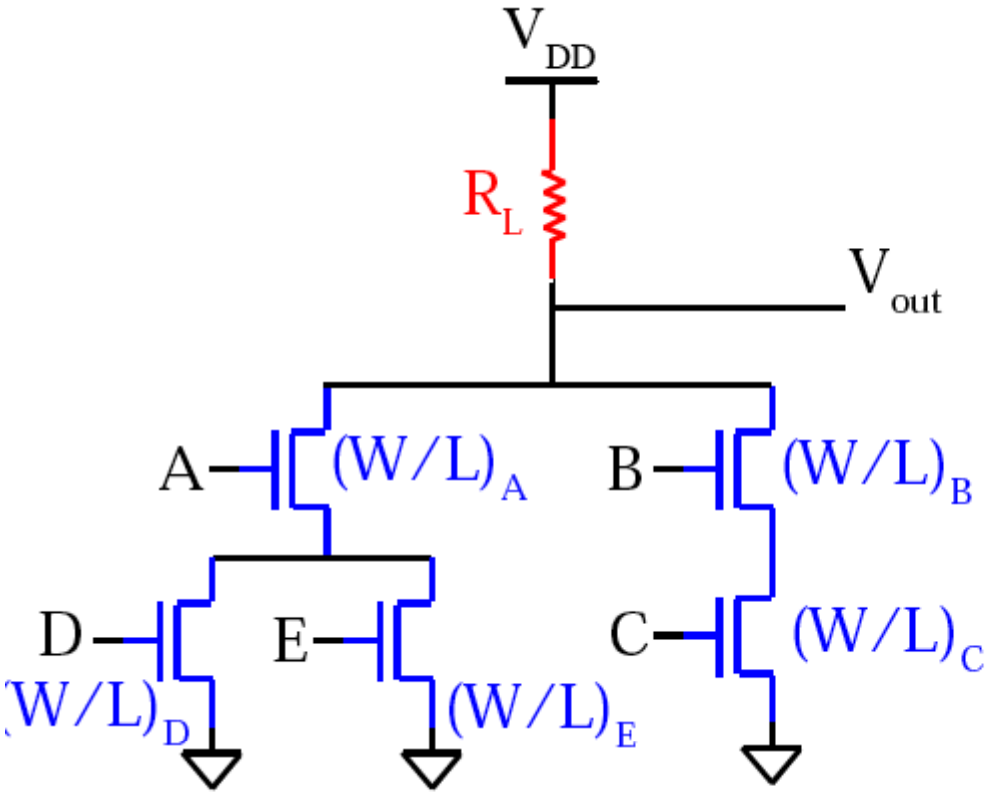
- n-Well
- p-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

COMPLEX LOGIC GATES

$$Z = \overline{A(D + E) + BC}$$

"OR" OPS PERFORMED BY PARALLEL CONECTED DRIVERS.
"AND" OPS PERFORMED BY SERIES CONNECTED DRIVERS.
"INVERSION" IS PROVIDED BY NATURE OF MOS CIRCUIT OP.





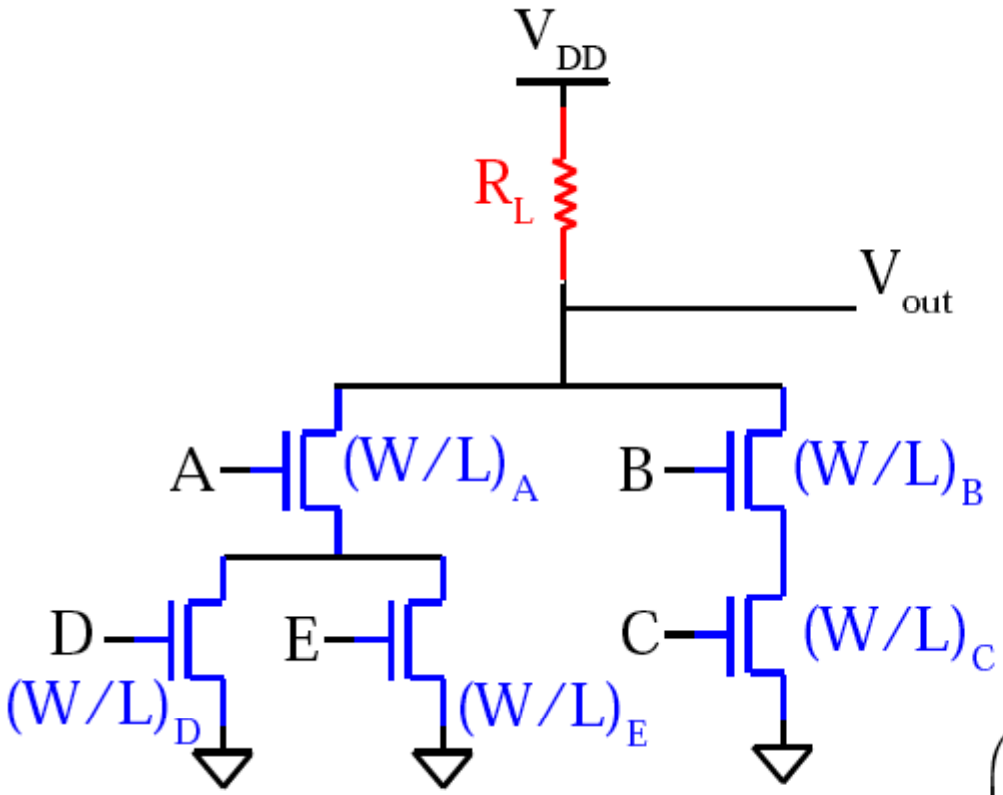
ON Drivers	Out-GND Path
A-D	Class 1
A-E	Class 1
B-C	Class 1
A-D-E	Class 2
A-D-B-C	Class 3
A-E-B-C	Class 3
A-D-E-B-C	Class 4

G1 < G2 < G3 < G4

$V_{OL1} > V_{OL2} > V_{OL3} > V_{OL4}$

EQV INVERTER (for case G4 where A = B = C = D = E = 1)

$$\left(\frac{W}{L}\right)_{EQV} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E}}$$



$$\left(\frac{W}{L}\right)_{EQV-ND2} = \frac{1}{2}\left(\frac{W}{L}\right)$$

DESIGN STRATEGY:

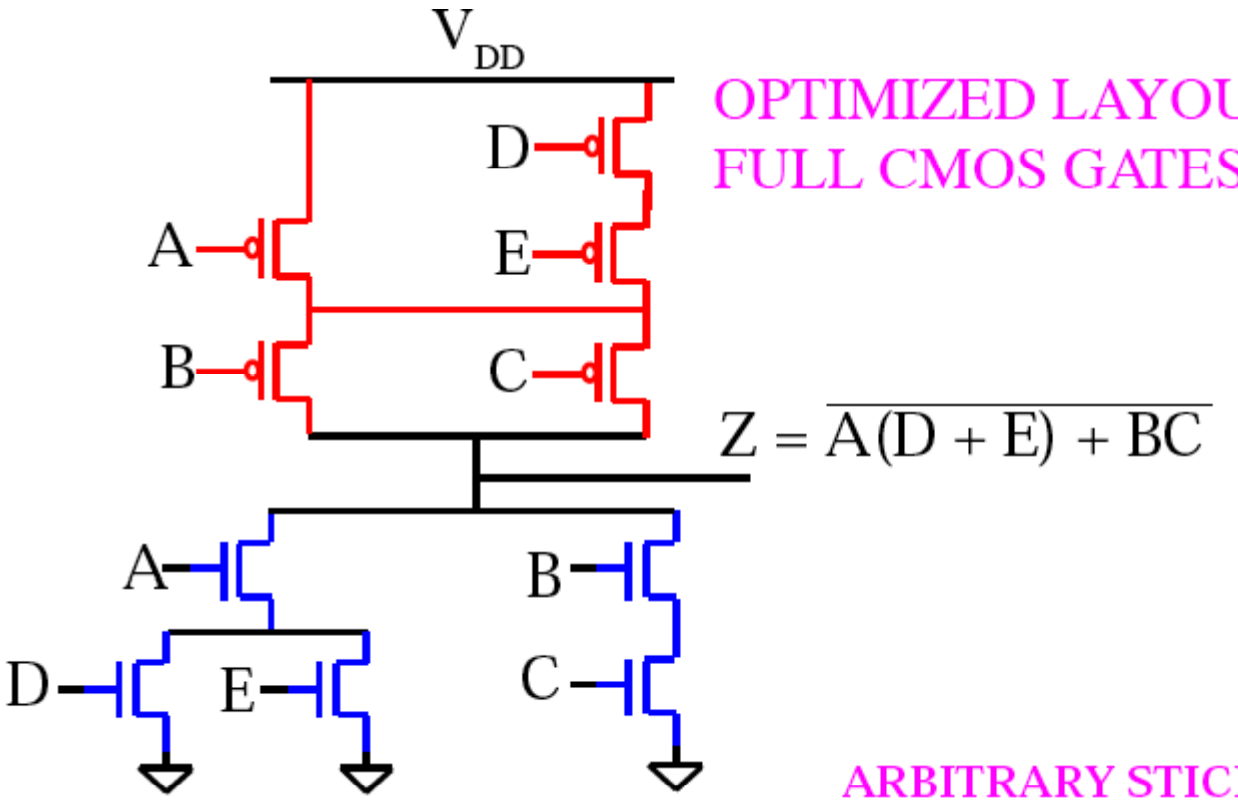
1. Identify all WORST CASE Paths (e.g. Class 1).
2. Determine nMOS transistor sizes such that each Class 1 path has $(W/L)_{EQV}$.

$$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_D = 2\left(\frac{W}{L}\right)_{EQV}$$

$$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_E = 2\left(\frac{W}{L}\right)_{EQV}$$

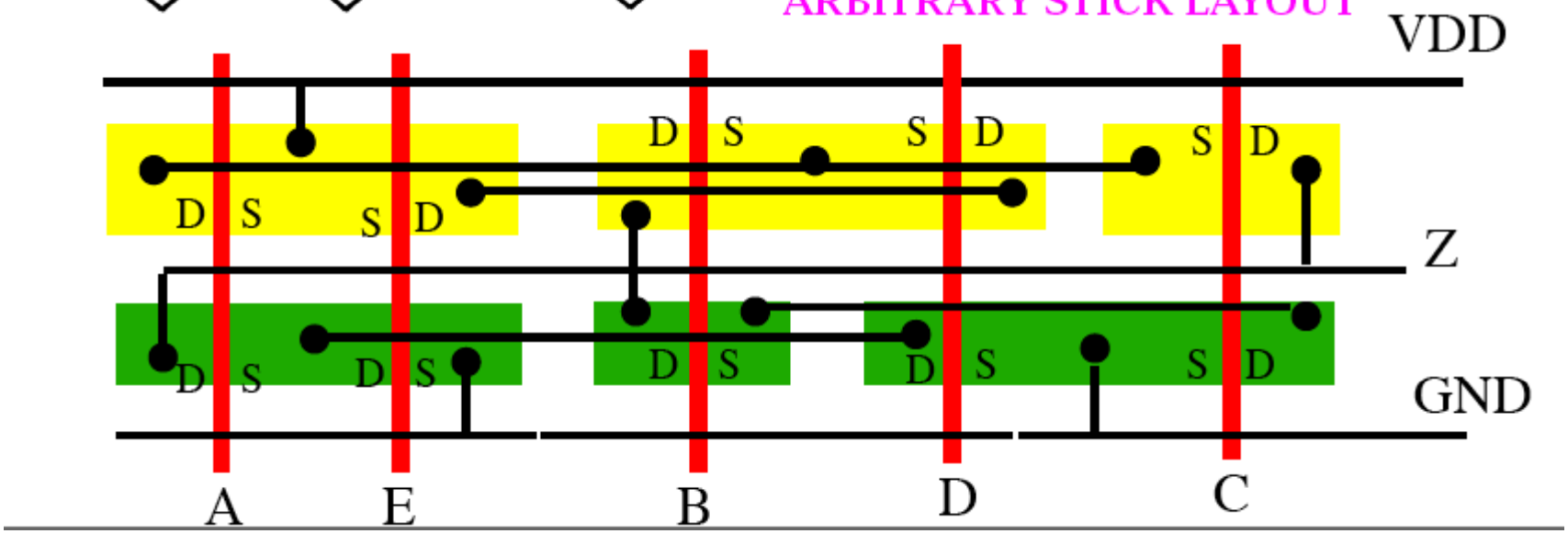
$$\left(\frac{W}{L}\right)_B = \left(\frac{W}{L}\right)_C = 2\left(\frac{W}{L}\right)_{EQV}$$

OPTIMIZED LAYOUT OF COMPLEX FULL CMOS GATES

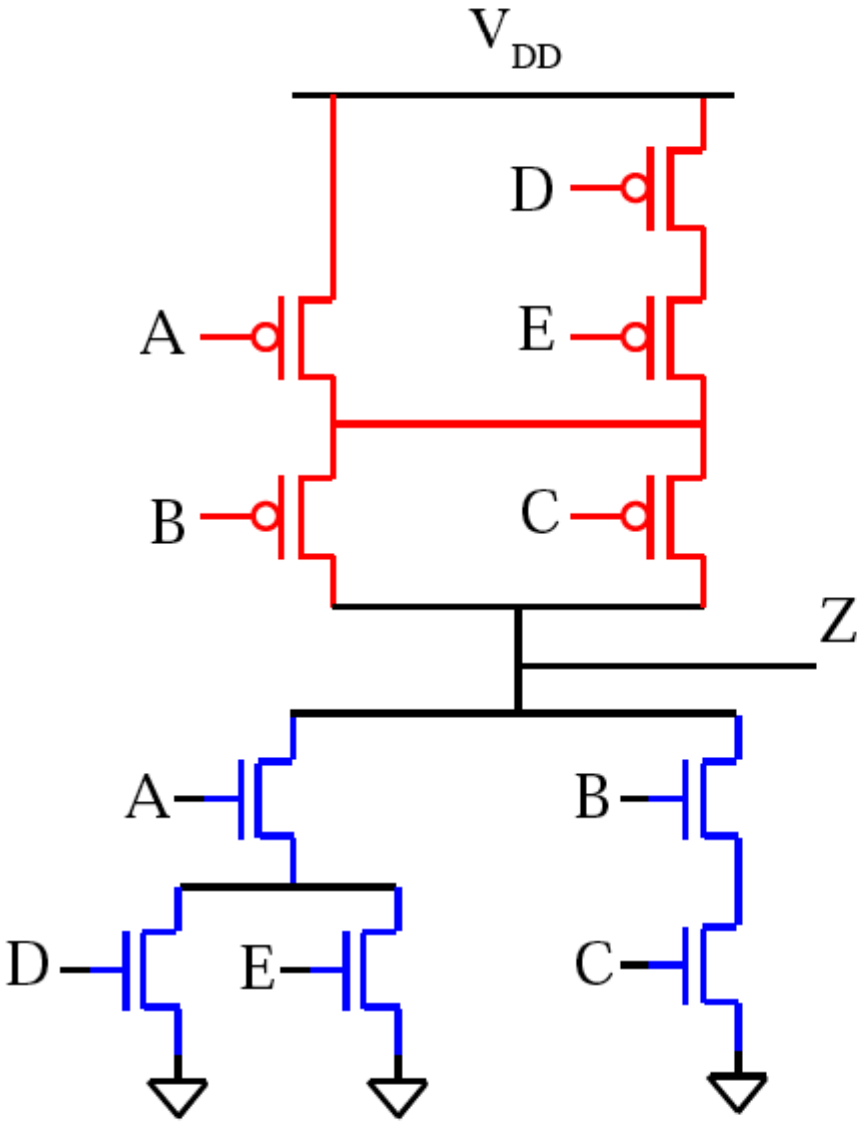


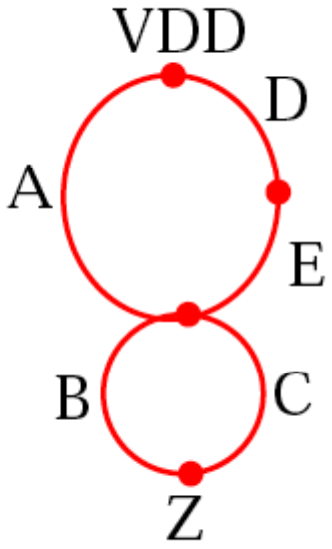
$$Z = \overline{A(D + E) + BC}$$

ARBITRARY STICK LAYOUT

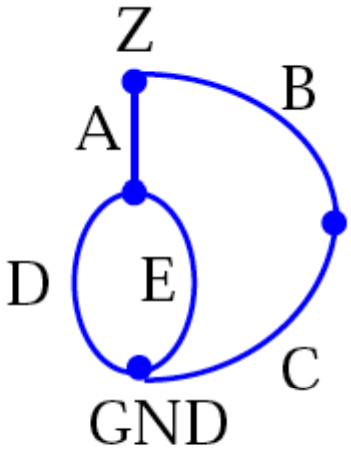


OTIMIZED LAYOUT OF COMPLEX FULL CMOS GATES



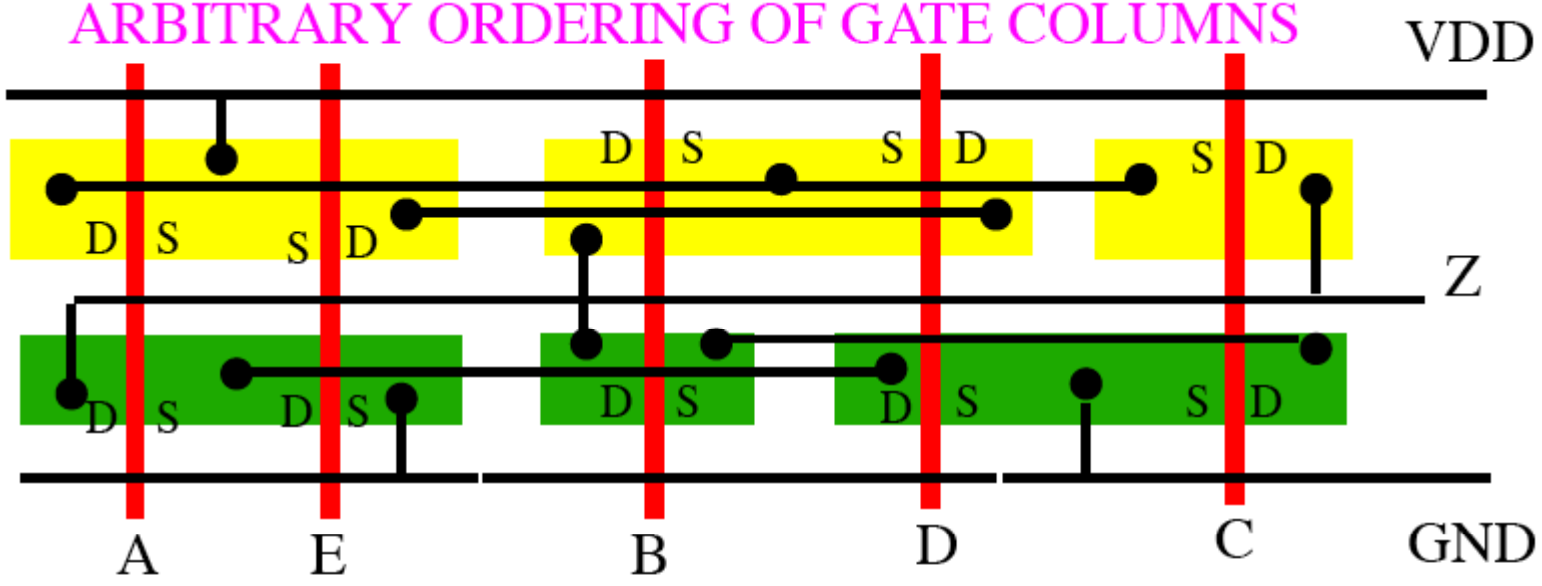


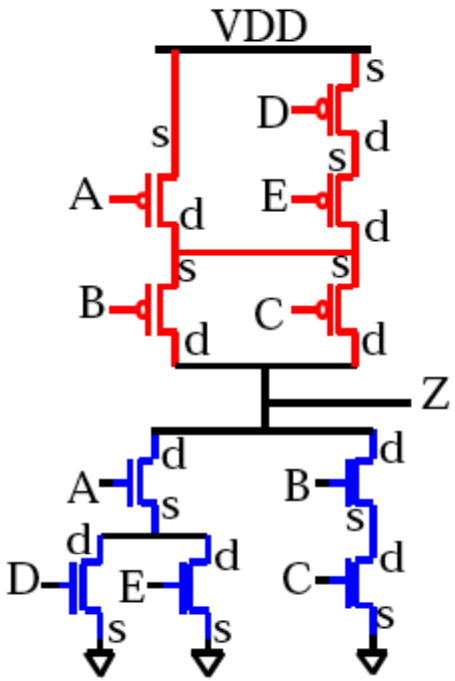
pMOS NET GRAPH

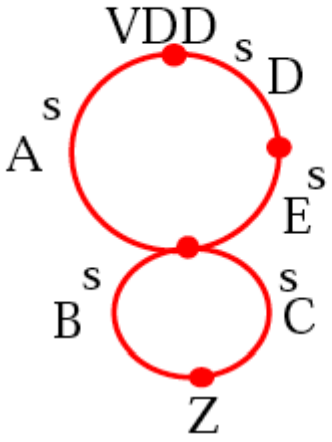


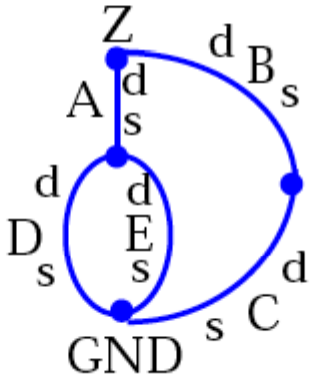
nMOS NET GRAPH

ARBITRARY ORDERING OF GATE COLUMNS





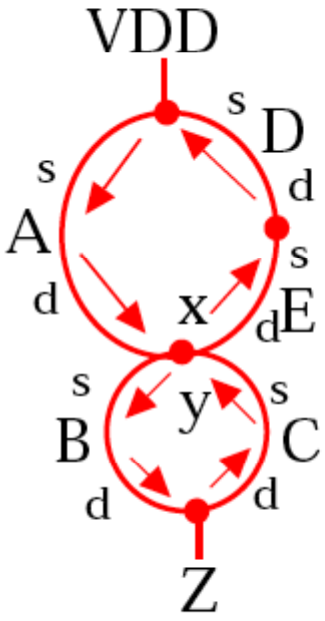




Euler path - connected sequence of edges

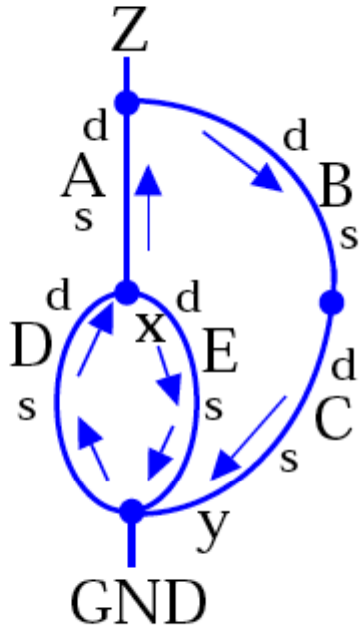
n, p diffusions for common Euler paths have layouts with no diffusion breaks.

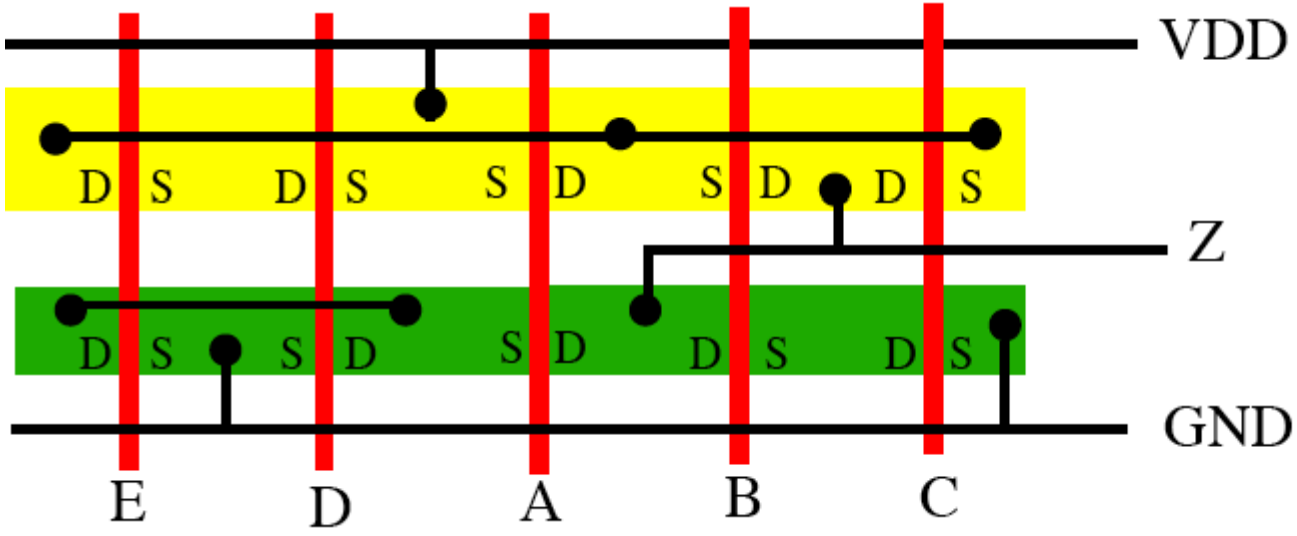
MINIMIZE NUMBER OF DIFFUSION BREAKS

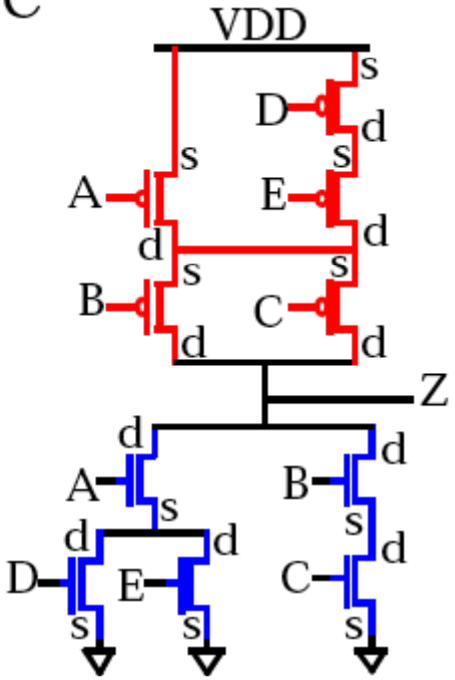


COMMON EULER PATH:
E-D-A-B-C

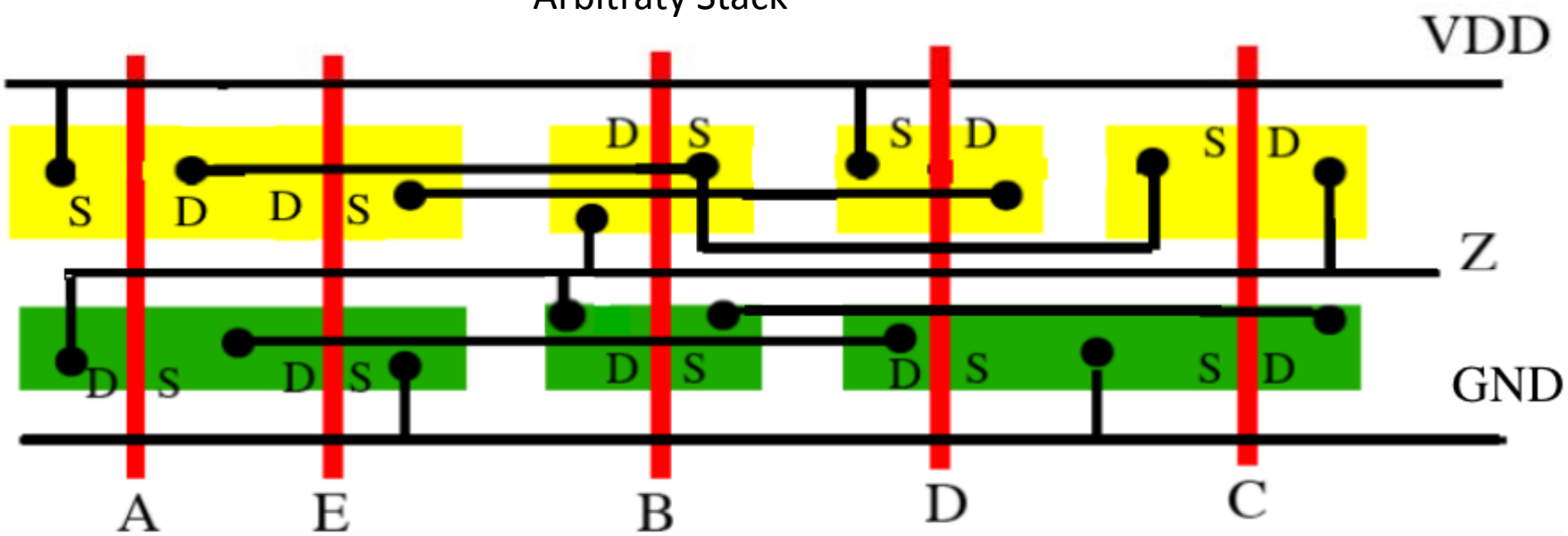
Is A-D-E-C-B a common Euler path?



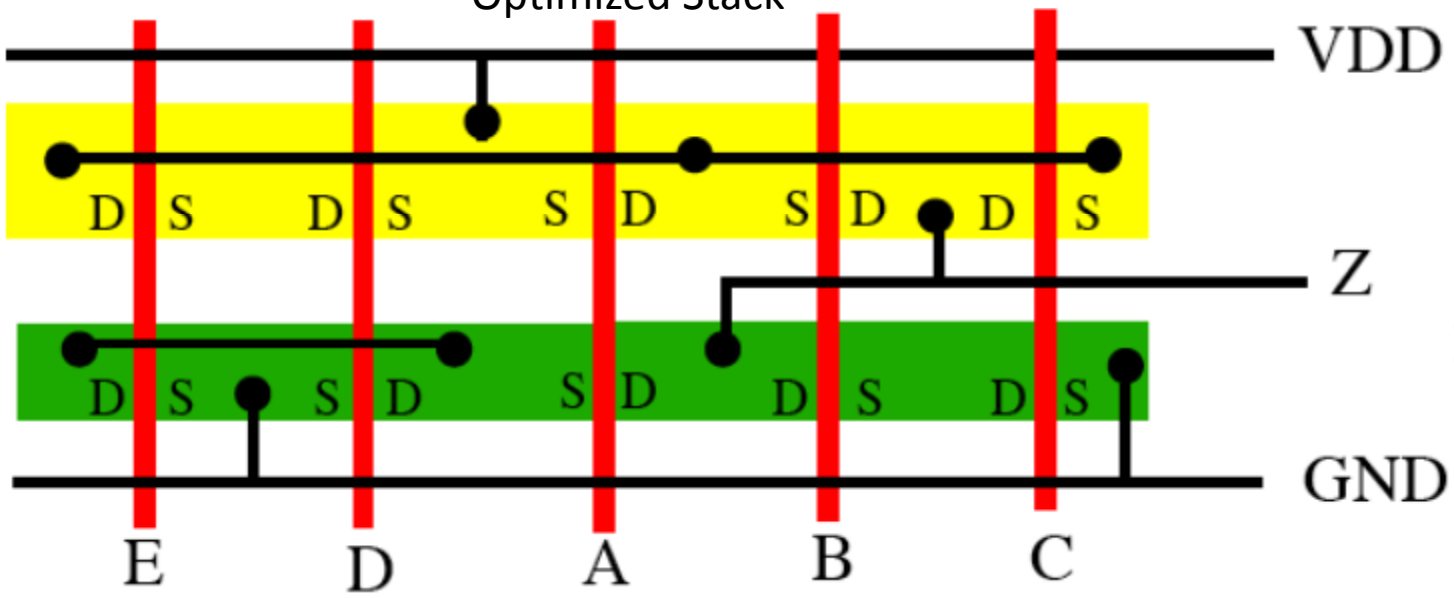




Arbitraty Stack



Optimized Stack



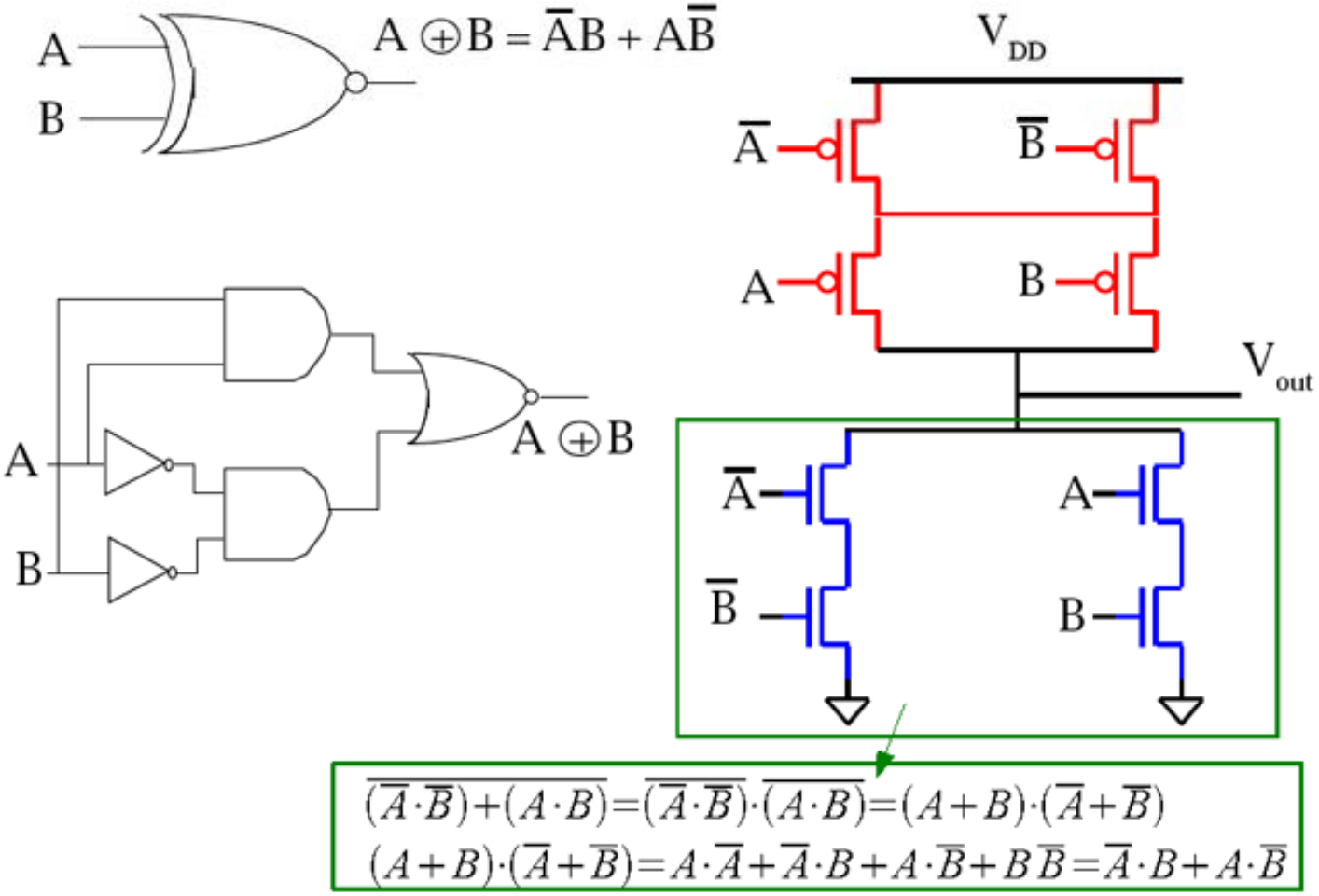
ALGORYTHYM FOR LINE OF GATES LAYOUT STYLE

1. Find all Euler paths that cover the graph.

2. Find common n- and p- Euler paths.

3. If no Euler paths are found in step 2, break the gate in the minimum number of places that to achieve step 2 with separate common Euler paths.

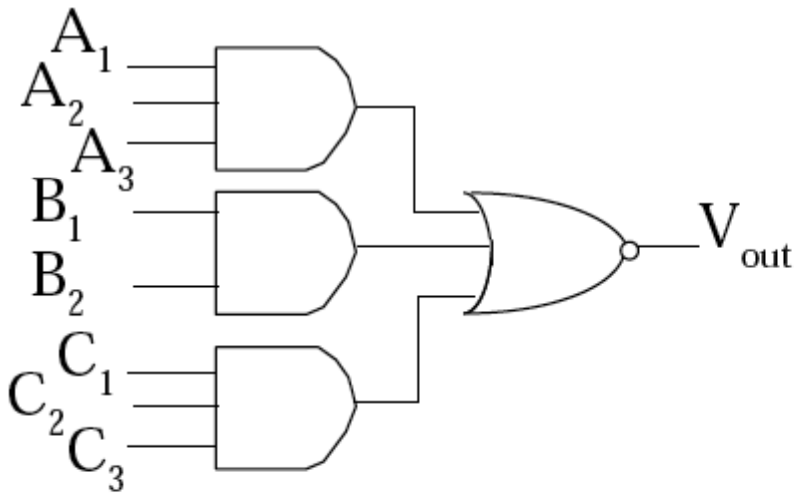
FULL CMOS XOR GATE



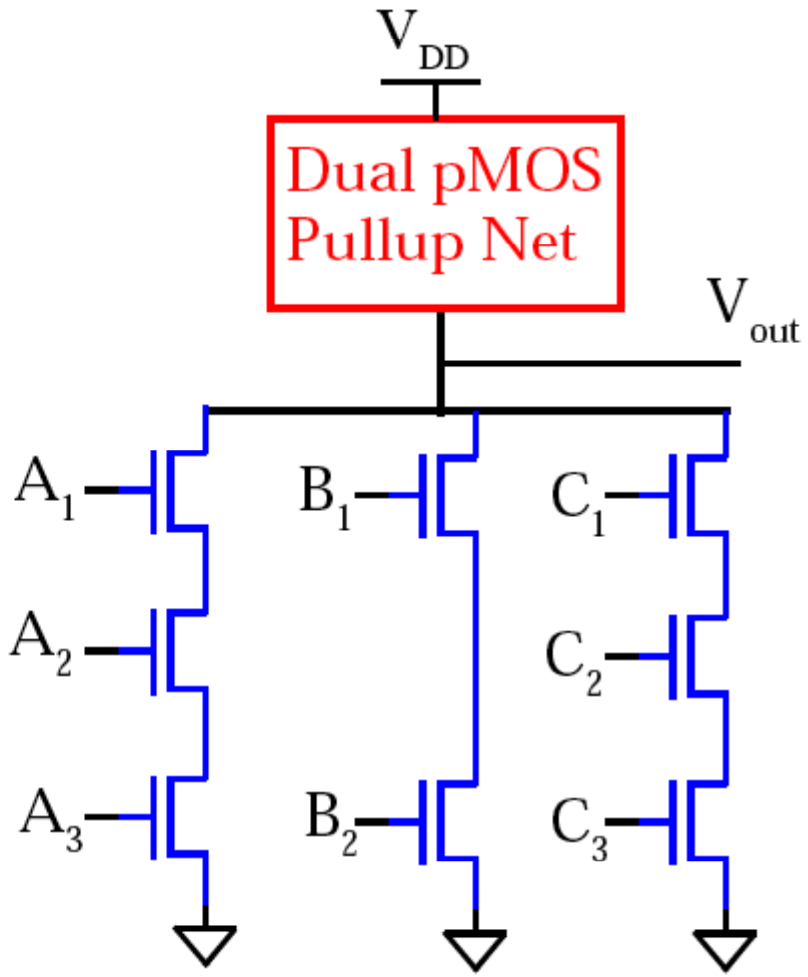
AOI & OAI GATES

AOI -> AND-OR-INVERT (for SUM - of - PRODUCTS Realization)

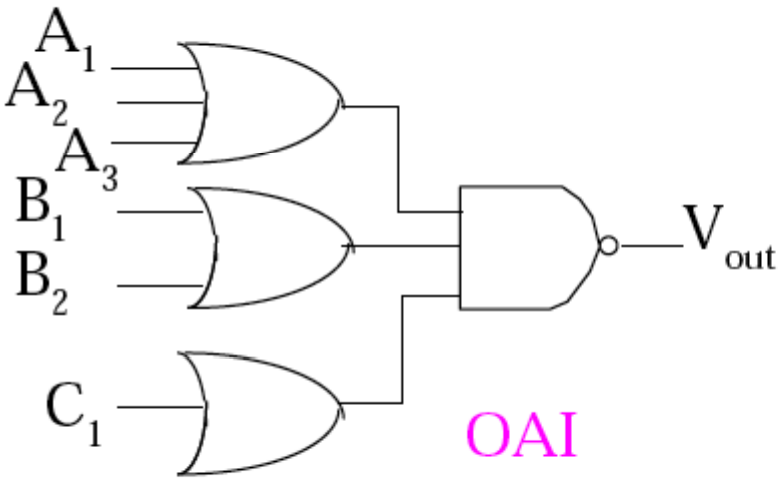
OAI -> OR-AND-INVERT (for PRODUCT - of - SUMS Realization)

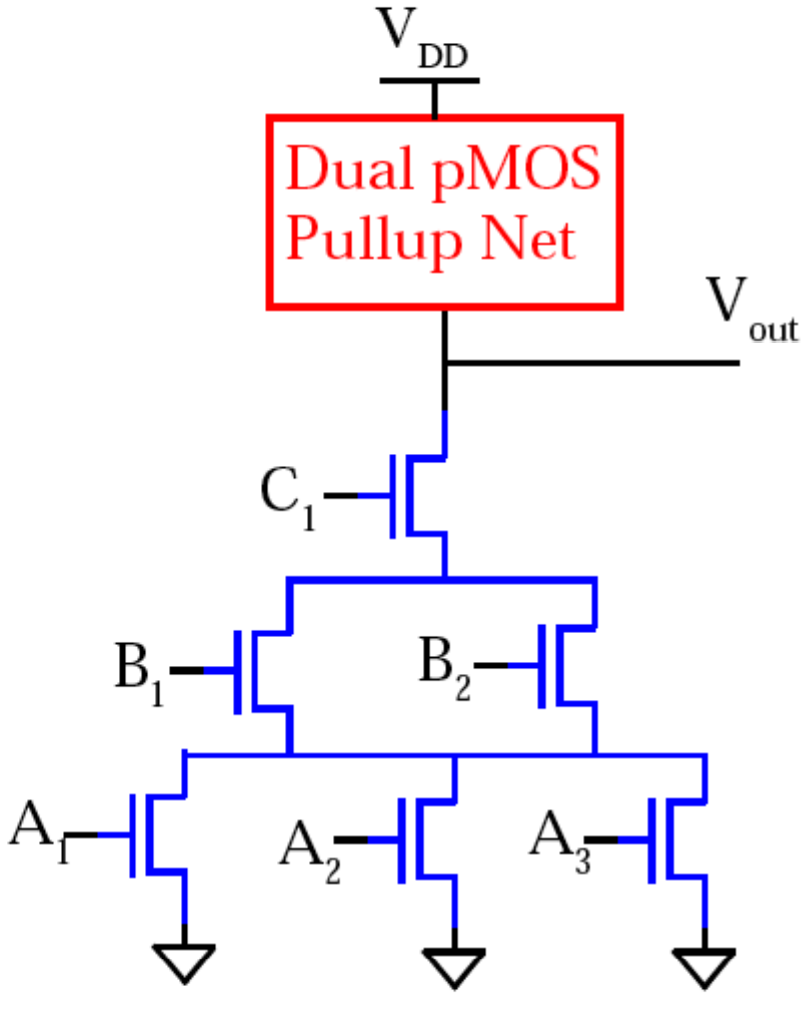


AOI

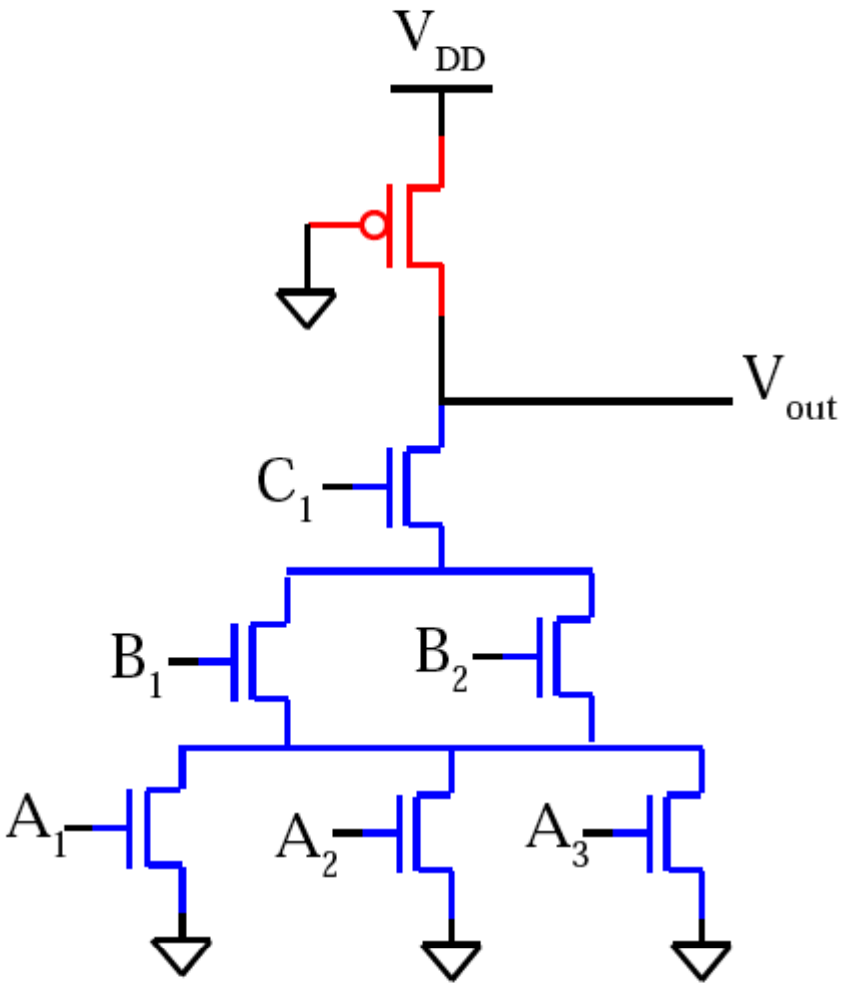


OAI -> OR-AND-INVERT (for PRODUCT - of - SUMS Realization)



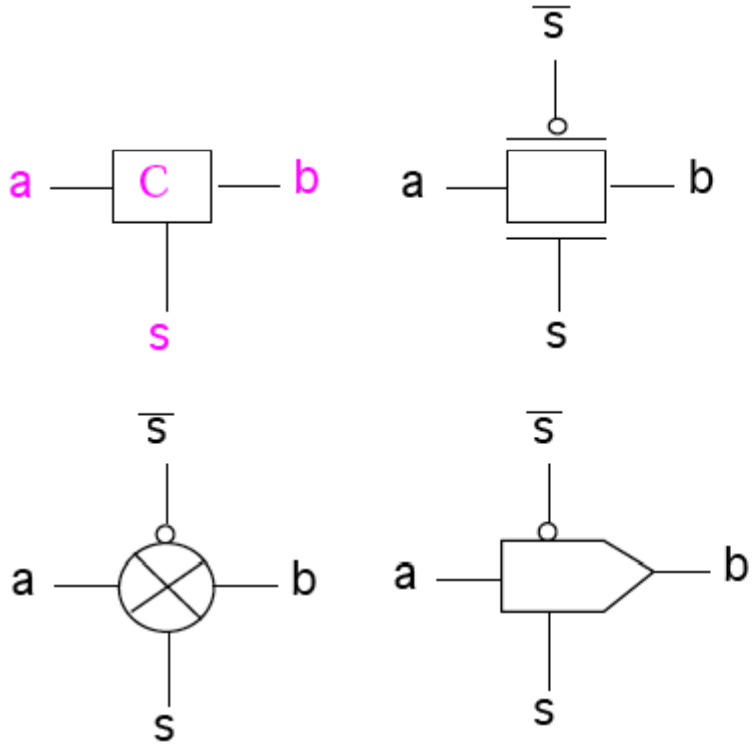


Pseudo-nMOS OAI Realization



CMOS Transmission Gates (TGs) & TG Logic

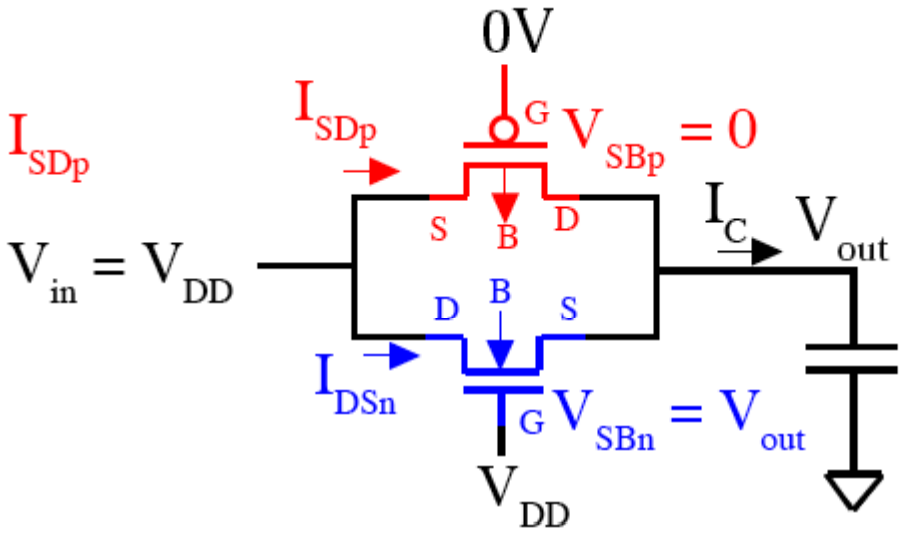
SYMBOLS



SWITCH CHARACTERISTICS

Input		Output
0	a — b	Srong 0
1	a — b	Strong 1

$I_C = I_{DSn} + I_{SDp}$



$V_{DSn} = V_{DD} - V_{out}$

$V_{GSn} = V_{DD} - V_{out}$

$V_{DSp} = V_{out} - V_{DD}$

$V_{GSp} = - V_{DD}$

REGION 1
nMOS: SAT
pMOS: SAT
$V_{DSn} > V_{GSn} - V_{Tn}$
$V_{DSp} < V_{GSp} - V_{Tp}$

REGION 2
nMOS: SAT
pMOS: LIN
$V_{DSn} > V_{GSn} - V_{Tn}$
$V_{DSp} > V_{GSp} - V_{Tp}$

REGION 3
nMOS: OFF
pMOS: LIN
$V_{GSn} < V_{Tn}$
$V_{DSp} > V_{GSp} - V_{Tp}$

V_{out}

0V $\quad |V_{Tp}| \quad (V_{DD} - V_{Tn}) \quad V_{DD}$

$$R_{eqn} = \frac{V_{DD} - V_{out}}{I_{DSn}} \qquad R_{eqp} = \frac{V_{DD} - V_{out}}{I_{SDp}} \qquad R_{eqTOT} = R_{eqn} \| R_{eqp}$$

REGION 1:
nMOS: SAT
pMOS: SAT

$$R_{eqn} = \frac{2(V_{DD} - V_{out})}{k_n (V_{DD} - V_{out} - V_{Tn})^2}$$

$$R_{eqp} = \frac{2(V_{DD} - V_{out})}{k_p (V_{DD} - |V_{Tp}|)^2}$$

REGION 2
nMOS: SAT
pMOS: LIN

$$R_{eqn} = \frac{2(V_{DD} - V_{out})}{k_n (V_{DD} - V_{out} - V_{Tn})^2}$$

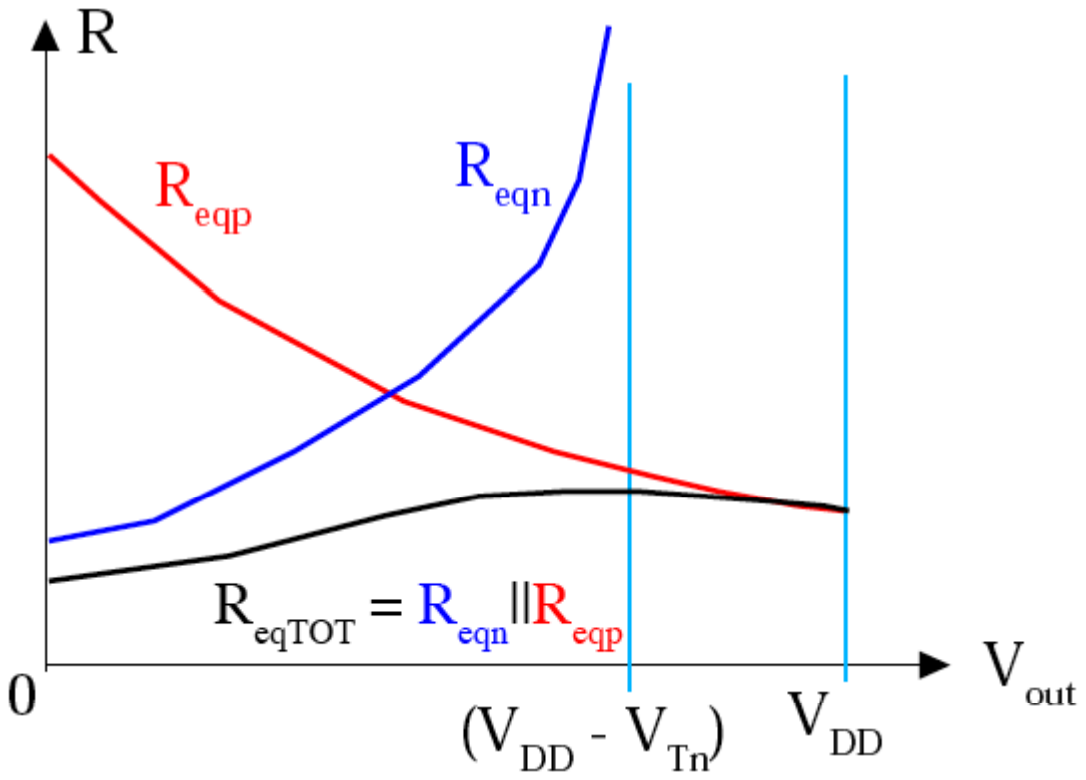
$$R_{eqp} = \frac{2(V_{DD} - V_{out})}{k_p \left[2(V_{DD} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]}$$

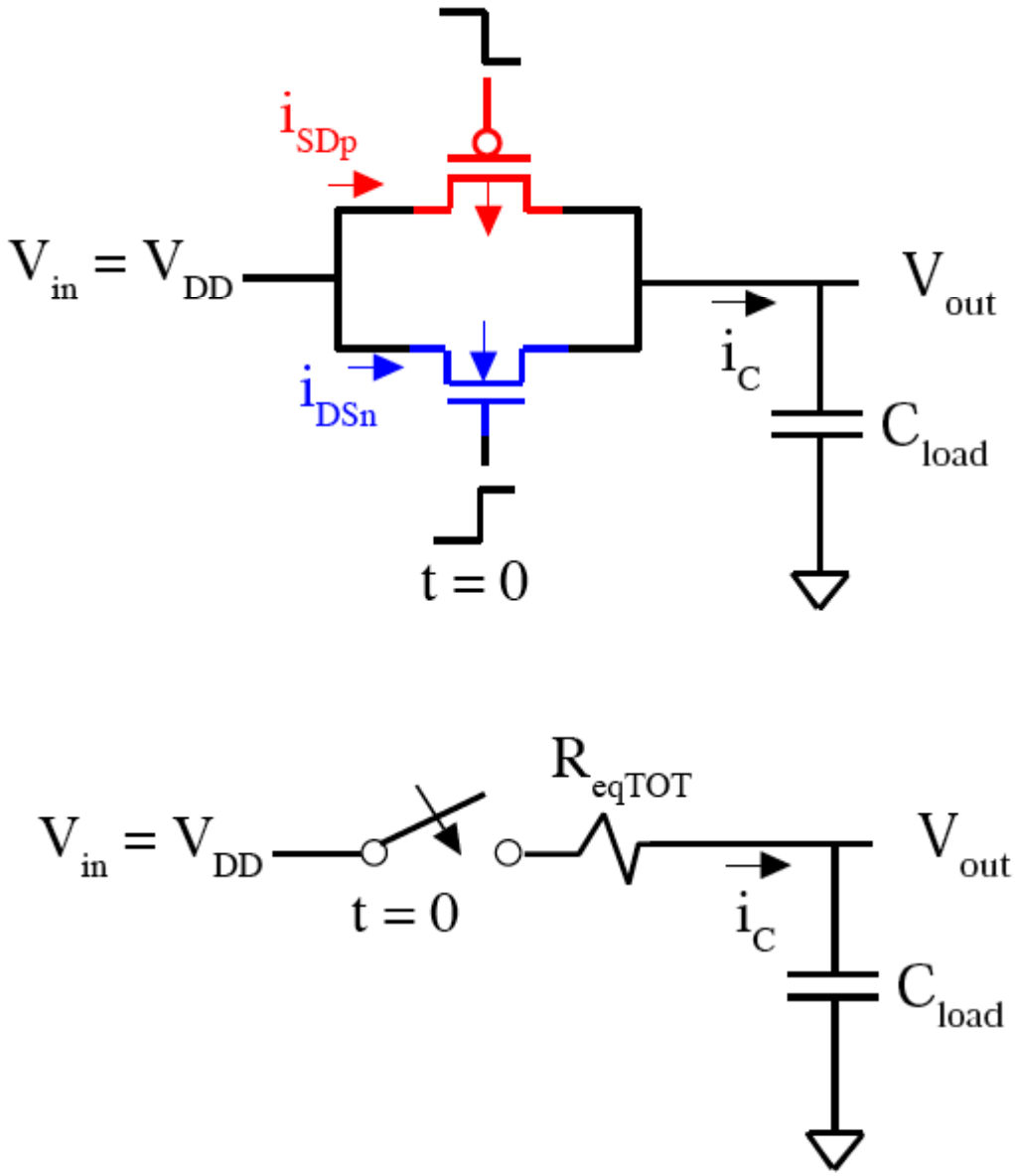
$$= \frac{2}{k_p \left[2(V_{DD} - |V_{Tp}|) - (V_{DD} - V_{out}) \right]}$$

REGION 3
nMOS: OFF
pMOS: LIN

$$R_{eqn} = \infty$$

$$R_{eqp} = \frac{2}{k_p \left[2(V_{DD} - |V_{Tp}|) - (V_{DD} - V_{out}) \right]}$$


R
R_{eqp}
R_{eqn}
$R_{eqTOT} = R_{eqn} || R_{eqp}$
0
V_{out}
$(V_{DD} - V_{Tn})$
V_{DD}


i_{SDp}
$V_{in} = V_{DD}$
V_{out}
i_C
i_{DSn}
C_{load}
t = 0
R_{eqTOT}
$V_{in} = V_{DD}$
t = 0
V_{out}
i_C
C_{load}

TRANSMISSION GATE LAYOUTS

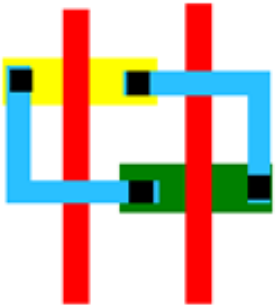
Simple and small, but no metal lines can pass horizontally

poly used to achieve horizontal metal1 transparency

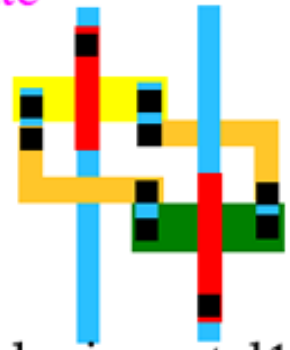
metal2 used to achieve horizontal metal1 transparency

Routing Gate Signals to Transmission Gate

horizontal, via metal1



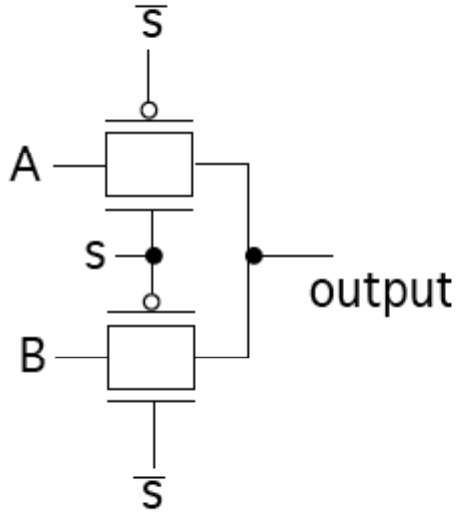
vertical, via poly



vertical, via metal1 straps

metal2 used to achieve vertical metal1 transparency

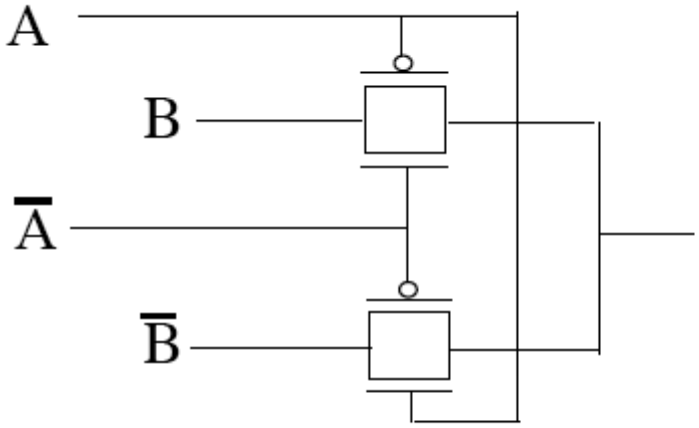
2-INPUT MULTIPLEXER



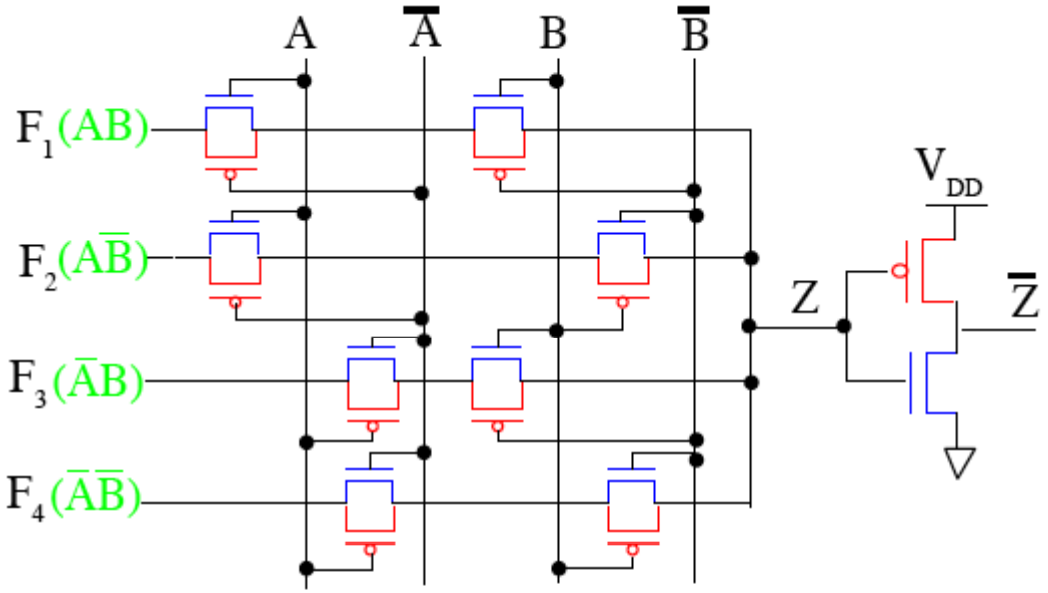
$$output = A.s + B \quad .\overline{s}$$

A	B	s	$\overline{s}$	output
x	0	0	1	0 (B)
x	1	0	1	1 (B)
0	x	1	0	0 (A)
1	x	1	0	1 (A)

XOR (COMPLEMENTARY PASS-TRANSISTOR LOGIC OR CPL)



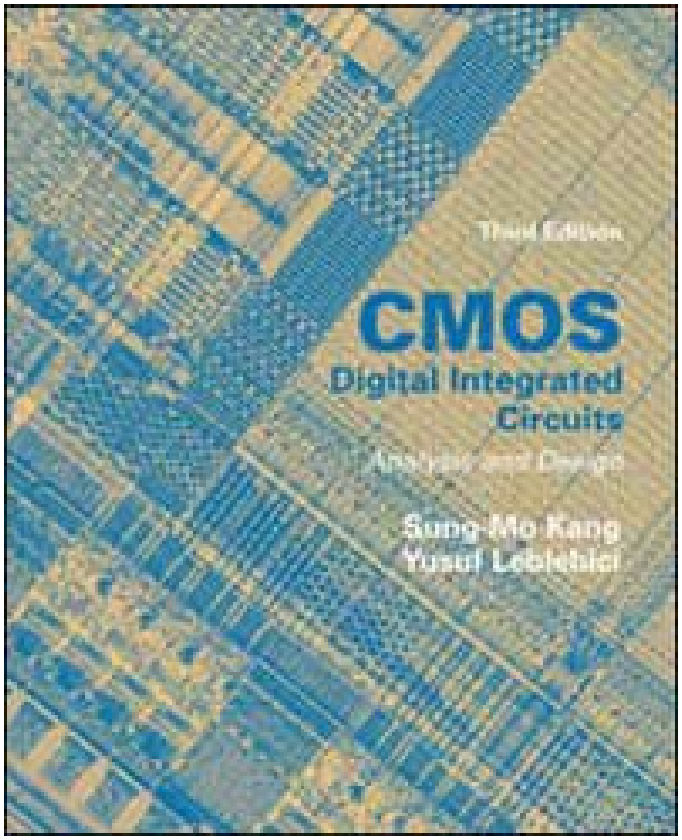
$$F = A\overline{B} + \overline{A}B$$



SOME OF THE FUNCTIONS REALIZED BY THE BOOLEAN FUNCTION UNIT (CPL)

OPERATION (Z)	F_1	F_2	F_3	F_4
NOR(A,B)	0	0	0	1
XOR(A,B)	0	1	1	0
NAND(A,B)	0	1	1	1
AND(A,B)	1	0	0	0
OR(A,B)	1	1	1	0

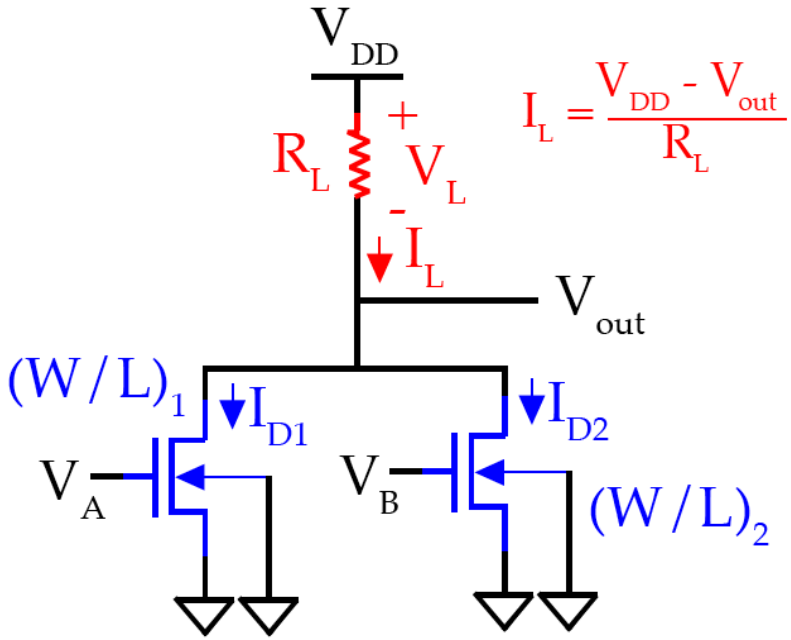
Digital IC Design and Architecture



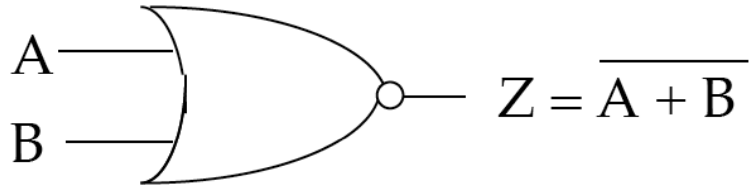
Combinational Logic with Resistive Load

MOS LOGIC CIRCUITS WITH RESISTOR LOADS

2-INPUT NOR GATE (NR2)

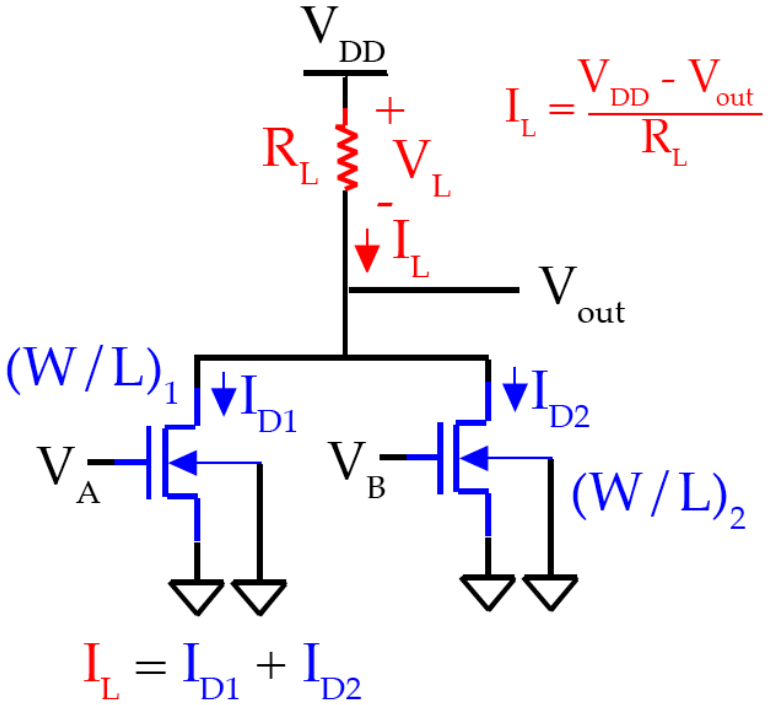


$$I_L = \frac{V_{DD} - V_{out}}{R_L}$$

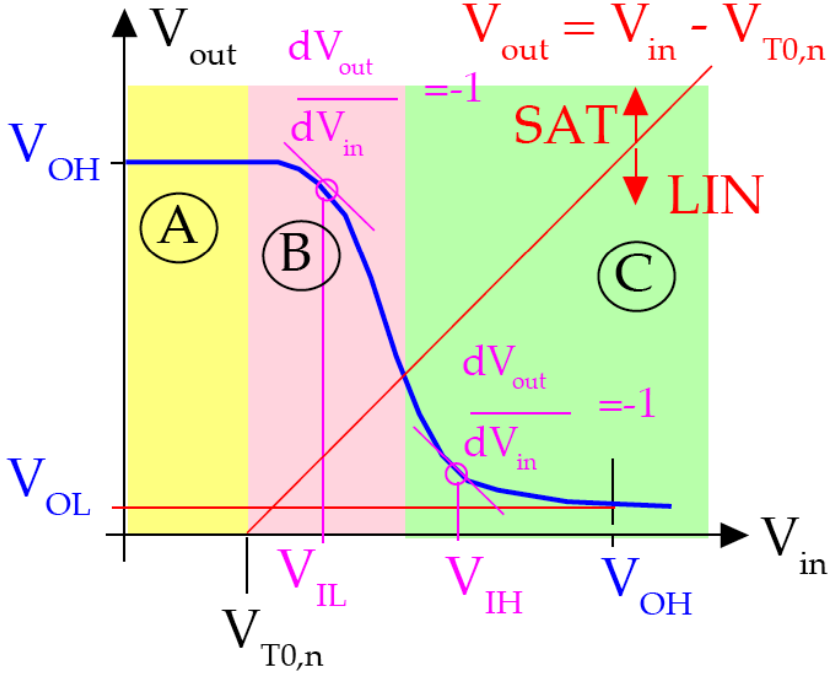


V_A	V_B	V_{out}
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOWER

$$I_L = \begin{cases} 0 & \text{CUTOFF} \\ \sum_{m(ON)} \frac{k'_{n,d}}{2}\left(\frac{W}{L}\right)_m \left[2(V_{GS,m} - V_{T0,n})V_{out} - (V_{out})^2\right] & \text{LIN} \\ \sum_{m(ON)} \frac{k'_{n,d}}{2}\left(\frac{W}{L}\right)_m \left[(V_{GS,m} - V_{T0,n})^2\right] & \text{SAT} \end{cases}$$



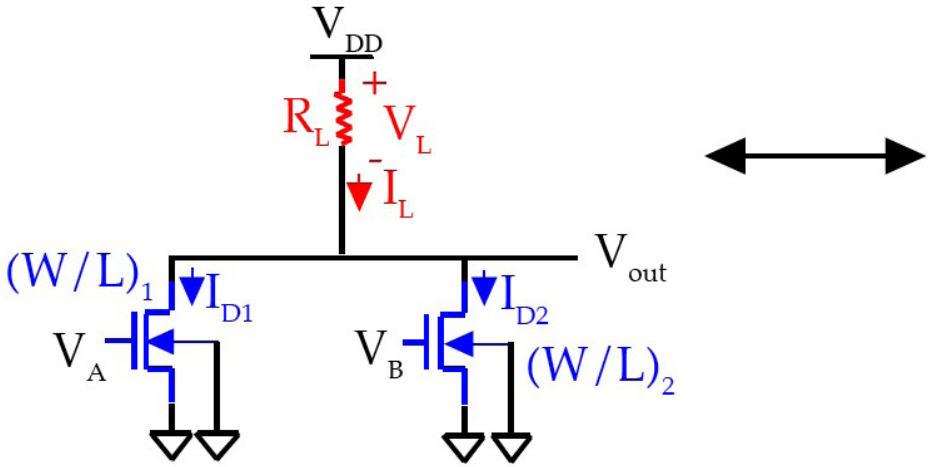
$$I_L = \frac{V_{DD} - V_{out}}{R_L}$$

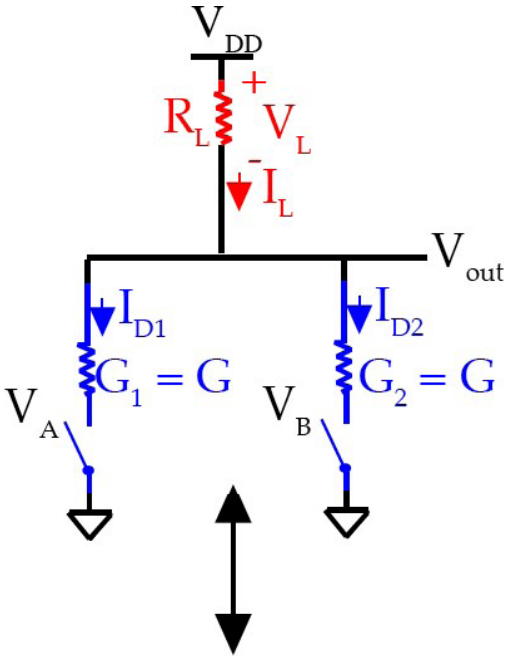


$V_{OH} = V_{DD}$: $V_A = V_B = 0 \Rightarrow I_{D1} = I_{D2} = 0 \Rightarrow I_L = 0$

V_{OL}:

V_A	V_B	V_{out}
LOW	V_{DD}	LOW
V_{DD}	LOW	LOW
V_{DD}	V_{DD}	LOWER

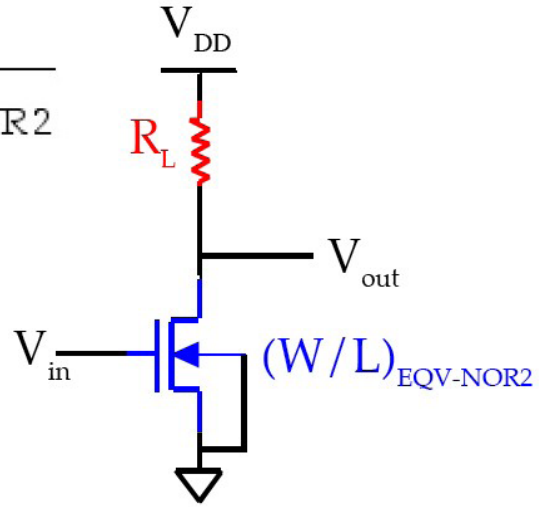




$$G_i = \frac{I_{Di}}{V_{DS}} = \frac{I_D}{V_{DS}} \propto KP_i\left(\frac{W}{L}\right)_i = KP\left(\frac{W}{L}\right)$$

$$k_{nEQV-NR2}R_L = \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL-NR2} + V_{OL-NR2}^2}$$

CASE	V_A	V_B	$G_{EQV-NR2}$	$(W/L)_{EQV-NR2}$
1	V_{DD}	V_{OL}	G	(W/L)
2	V_{OL}	V_{DD}	G	(W/L)
3	V_{DD}	V_{DD}	2G	2(W/L)



TRANSIENT ANALYSIS OF 2-INPUT NOR

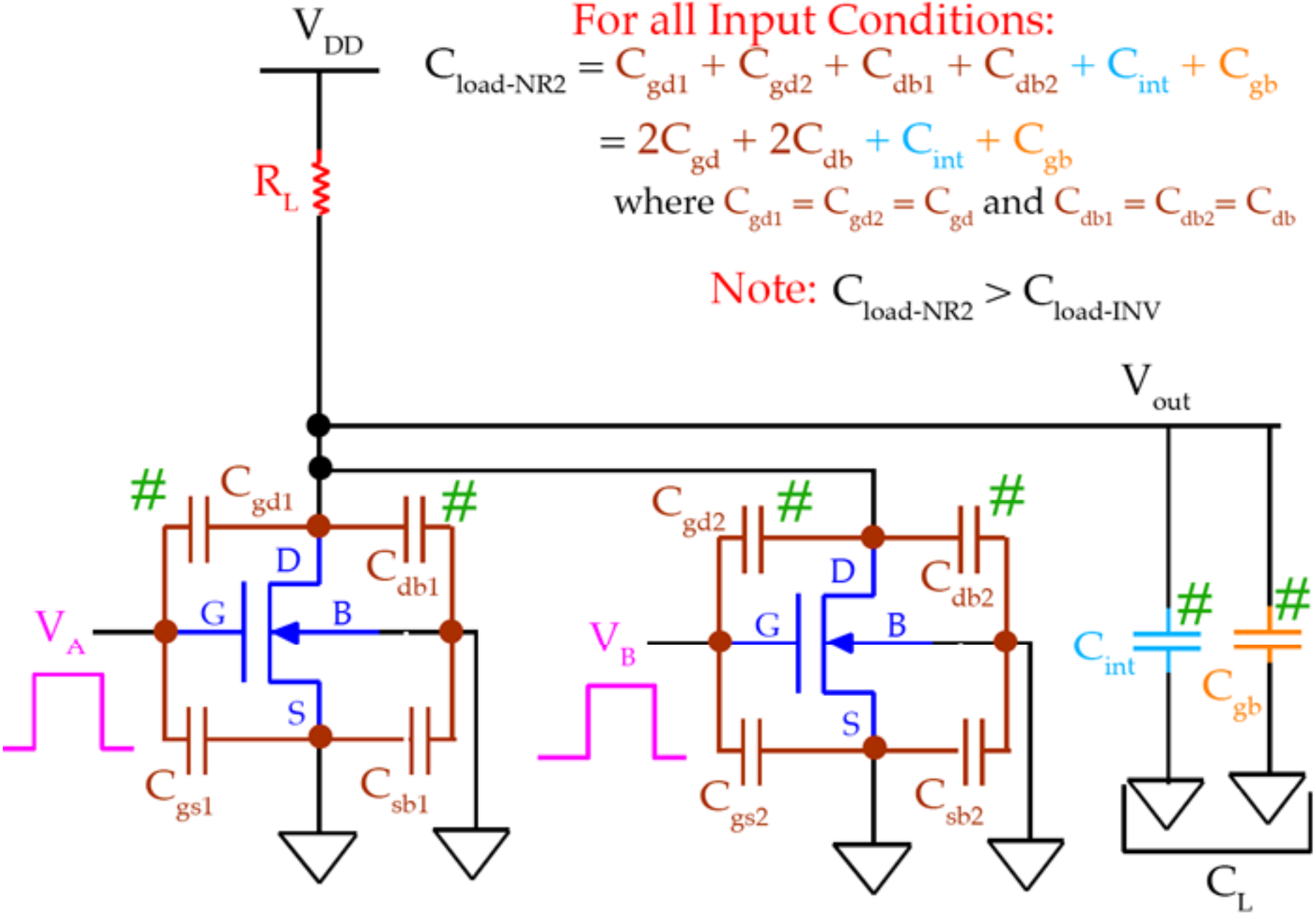
For all Input Conditions:

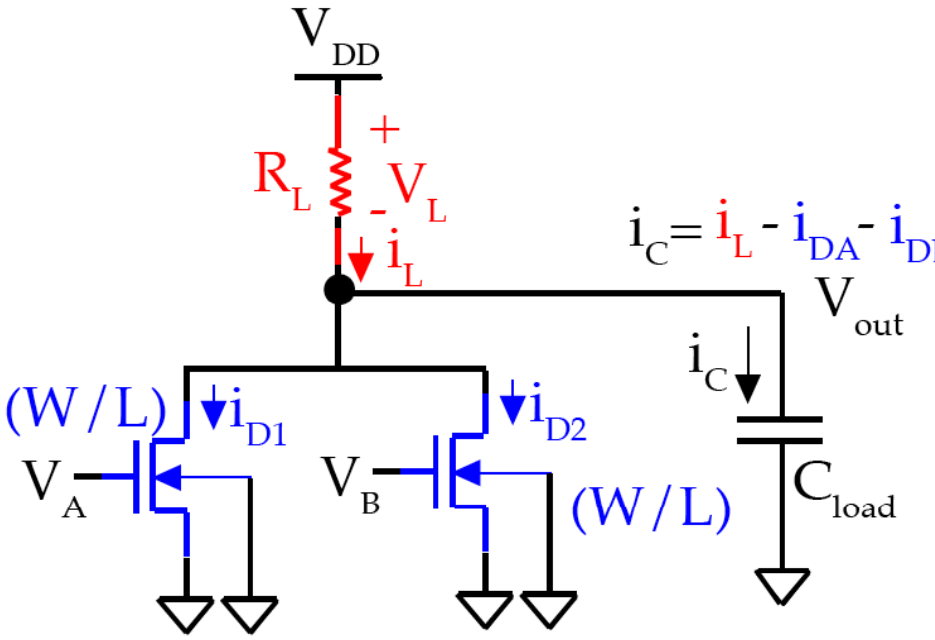
$$C_{load\text{-}NR2} = C_{gd1} + C_{gd2} + C_{db1} + C_{db2} + C_{int} + C_{gb}$$

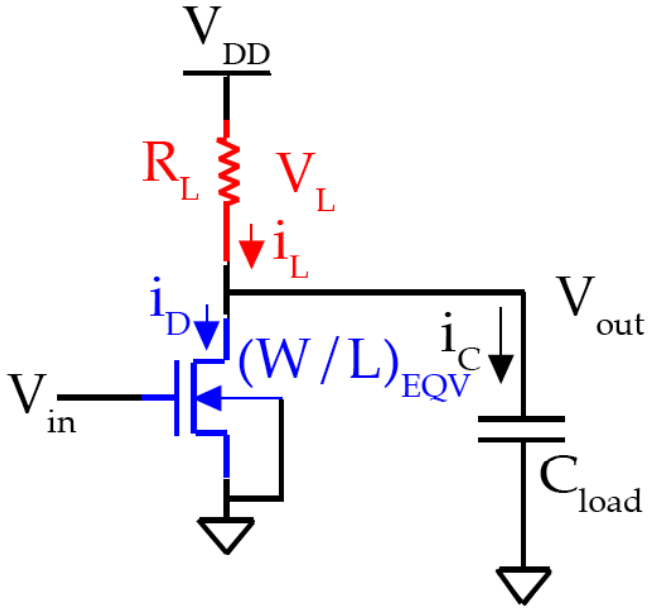
$$= 2C_{gd} + 2C_{db} + C_{int} + C_{gb}$$

where $C_{gd1} = C_{gd2} = C_{gd}$ and $C_{db1} = C_{db2} = C_{db}$

Note: $C_{load\text{-}NR2} > C_{load\text{-}INV}$







Recall for the INV:

$$\tau_{PHL-INV} = \frac{C_{load-INV}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL-INV}} - 1\right)\right]$$

For the NR2:

$C_{load\text{-}INV}$ -> $C_{load\text{-}NR2}$ (input pattern independent)

k_{EQV} -> mk_n where m = 1 or 2.

$V_{OL\text{-}INV}$ -> $V_{OL\text{-}NR2}$ (input pattern dependent)

$\tau_{PHL\text{-}INV}$ -> $\tau_{PHL\text{-}NR2}$ (input pattern dependent)

NR2 DESIGN STRATEGY

1. Design V_{OL} for worst case: CASE 1 or CASE 2 - V_A or $V_B = V_{DD}$.

Set $(W/L)_1 = (W/L)_2 = (W/L) = (W/L)_{EQV\text{-}NR2}$.

WHERE for EQV INV

$$k_{nEQV-NR2}R_L = \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL-NR2} + V_{OL-NR2}^2}$$

2. Design for delay for worst case: CASE 1 or CASE 2 i.e. one input switching L->H and other input set at V_{OL}.

$$\tau_{PHL-INV} = \frac{C_{load-INV}}{k_{nINV}(V_{DD} - V_{T0n})}\left[\frac{V_{T0n}}{(V_{OH} - V_{T0n})} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL-INV}} - 1\right)\right]$$

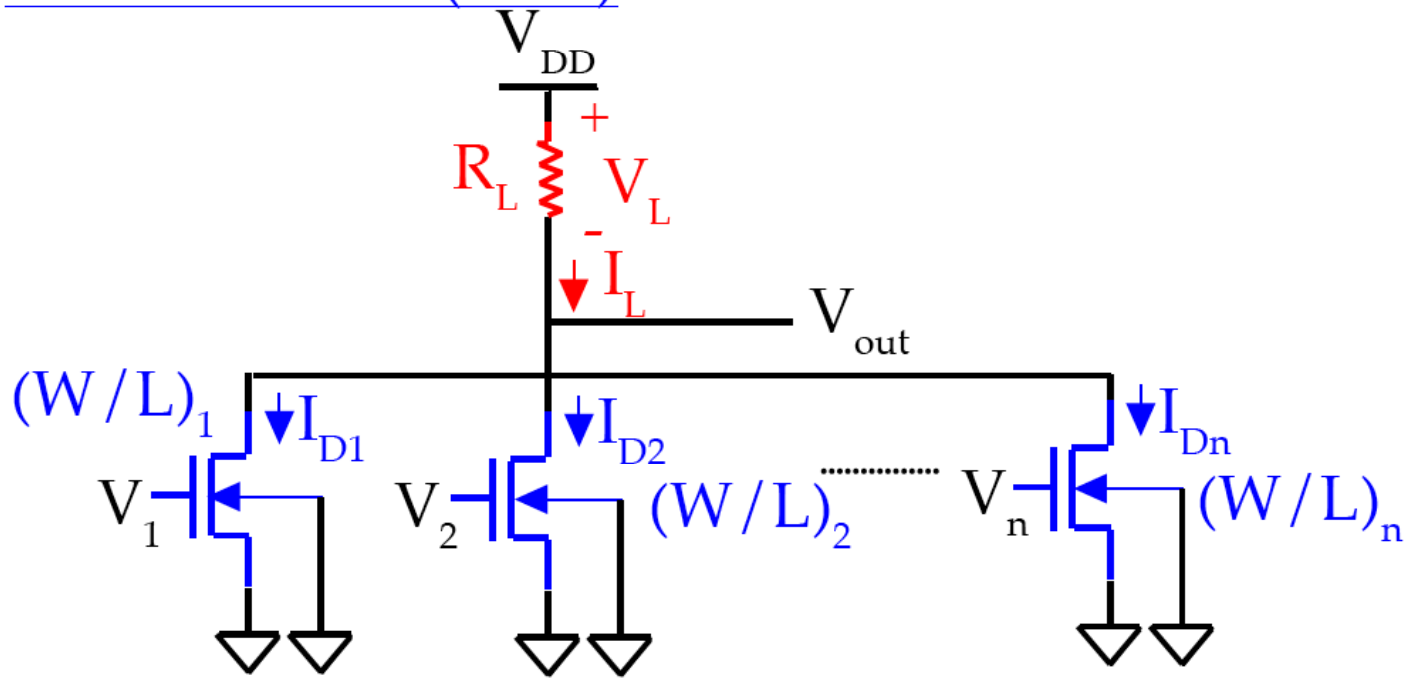
$$C_{load\text{-}NR2} = 2(C_{gd} + C_{db}) + C_{int} + C_{gb}$$

For the NR2:

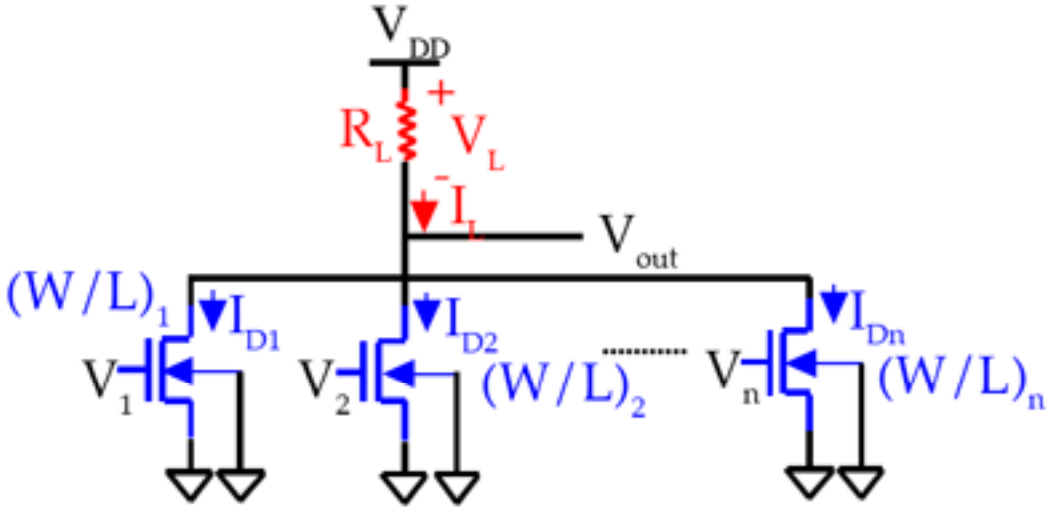
$\tau_{PHL\text{-}INV}$ -> $\tau_{PHL\text{-}NR2}$ ➔

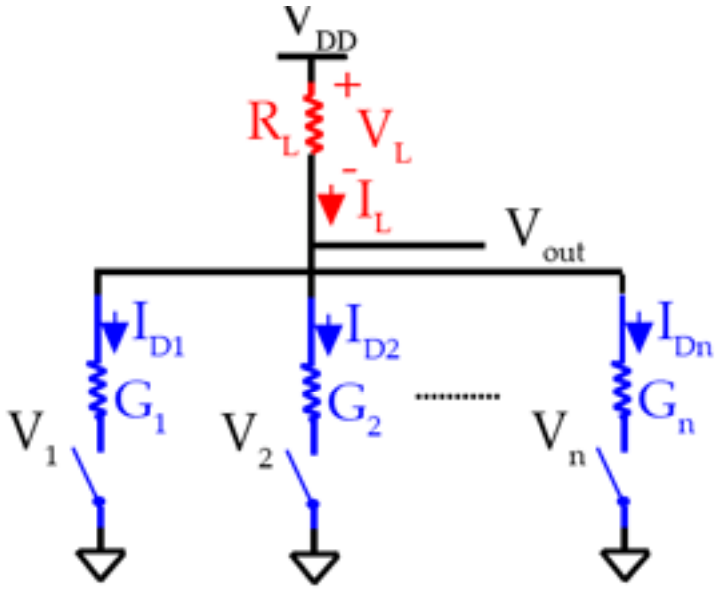
- $C_{load\text{-}INV}$ -> $C_{load\text{-}NR2}$ (Case 1 or Case 2)
- $V_{OL\text{-}INV}$ -> $V_{OL\text{-}NR2}$ (Case 1 or Case 2)
- k_{nINV} -> $k_{nEQV\text{-}NR2}$ (Case 1 or Case 2)

n INPUT NOR (NRn)



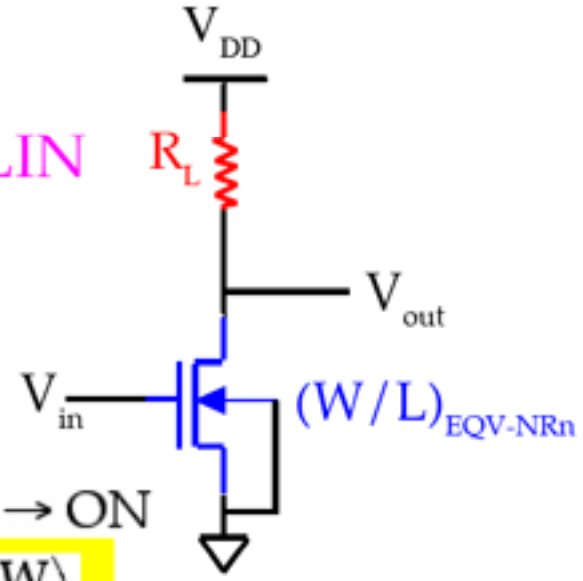
$$I_L = \begin{cases} \sum_{m(ON)} \frac{k'_{n,d}}{2}\left(\frac{W}{L}\right)_m \left[2(V_{GS,m} - V_{T0,n})\,V_{out} - (V_{out})^2\right] & \text{LIN} \\ \sum_{m(ON)} \frac{k'_{n,d}}{2}\left(\frac{W}{L}\right)_m \left[(V_{GS,m} - V_{T0,n})^2\right] & \text{SAT} \end{cases}$$





ASSUMING ALL nMOS DRIVERS HAVE IDENTICAL, (W/L) & $V_{GSi} = V_{GS}$ $= V_{DD}$ for all i = 1, 2, ..., m ≤ n; otherwise $V_{GS} = V_{OL}$

$$I_{DL} = \begin{cases} \frac{k'_{n,d}}{2}\left(\sum_{m(ON)}\left(\frac{W}{L}\right)_m\right)\left[2(V_{GS}-V_{T0,n})V_{out}-(V_{out})^2\right] & \text{LIN} \\ \frac{k'_{n,d}}{2}\left(\sum_{m(ON)}\left(\frac{W}{L}\right)_m\right)(V_{GS}-V_{T0,n})^2 & \text{SAT} \end{cases}$$



$$G_{EQV} = \sum_{i=1}^{m} G_i = mG \quad \text{where } m \le n = \text{number of nMOS} \rightarrow \text{ON}$$

$$\left(\frac{W}{L}\right)_{EGV-NRn} = \sum_{m(ON)}\left(\frac{W}{L}\right)_m = m\left(\frac{W}{L}\right)$$

← pattern dependent

NRn DESIGN STRATEGY

$$\left(\frac{W}{L}\right)_{EQV} = \sum_{m(ON)} \left(\frac{W}{L}\right)_m = m\left(\frac{W}{L}\right)$$

1. Design V_{OL} for worst case: $V_k = V_{DD}$, $V_i = V_{OL}$ for all $i \neq k$.

Set $(W/L)_1 = (W/L)_2 = \text{--} = (W/L)_n = (W/L) = (W/L)_{EQV\text{-}NRn}$.

WHERE for EQV INV

$$k_{nEQV-NRn} R_L = \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL-NRn} + V_{OL-NRn}^2}$$

2. Design for delay for worst case: $V_k = V_{DD}$, $V_i = V_{OL}$ for all $i \neq k$ i.e. one input switching L->H and all other inputs set at V_{OL}.

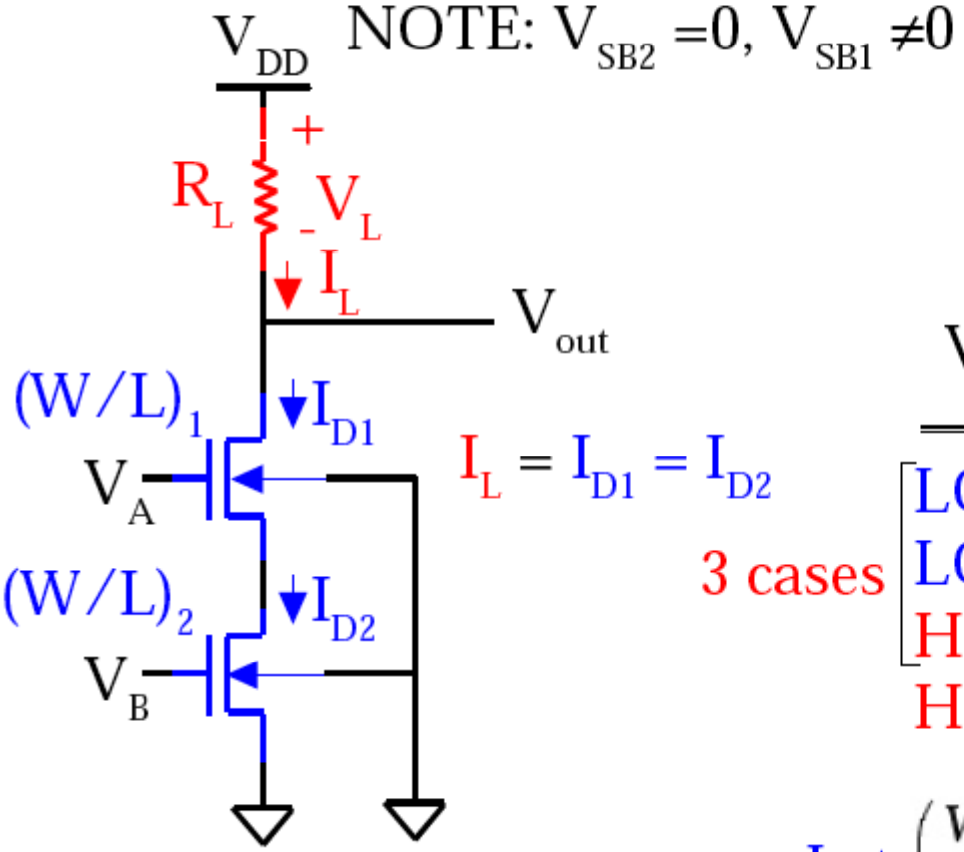
$$\tau_{PHL-INV} = \frac{C_{load-INV}}{k_{nINV}(V_{DD} - V_{T0n})}\left[\frac{V_{T0n}}{(V_{OH} - V_{T0n})} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL-INV}} - 1\right)\right]$$

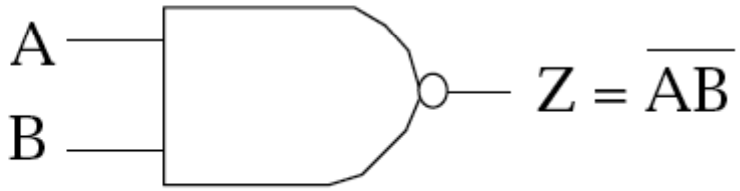
$$C_{load\text{-}INV} \Rightarrow C_{load\text{-}NRn} = n(C_{gd} + C_{db}) + C_{int} + C_{gb}$$

For the NRn:

$$\tau_{PHL\text{-}INV} \rightarrow \tau_{PHL\text{-}NORn} \rightarrow \begin{cases} C_{load\text{-}INV} \rightarrow C_{load\text{-}NRn} \\ V_{OL\text{-}INV} \rightarrow V_{OL\text{-}NRn} \\ k_{nINV} \rightarrow k_{nEQV\text{-}NRn} \end{cases}$$

2-INPUT NAND GATE (ND2)





$I_L = I_{D1} = I_{D2}$

3 cases

V_A	V_B	V_{out}
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

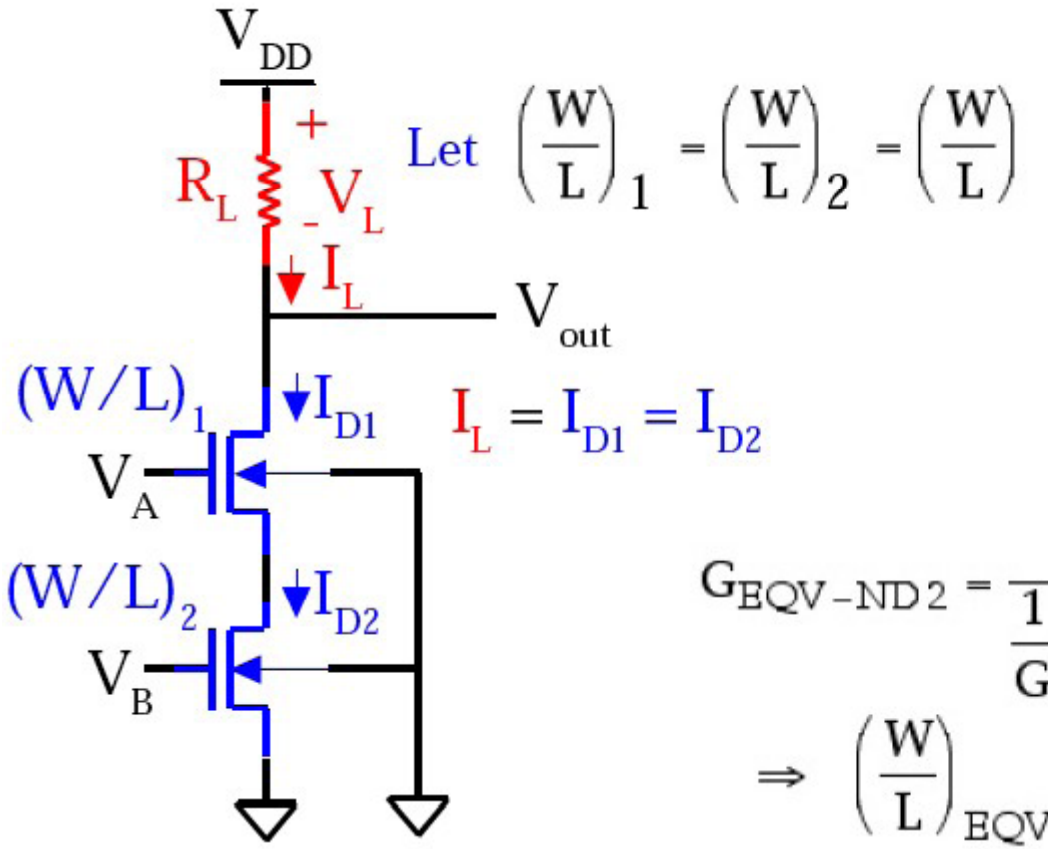
Let $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)$

CALCULATION OF V_{OH}

WHEN $V_A = 0$ and/or $V_B = 0 \Rightarrow I_L = I_{D1} = I_{D2} = 0$

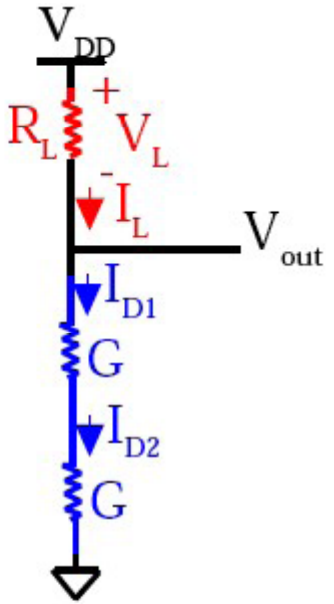
$V_{OH} = V_{DD}$ FOR ALL 3 INPUT CASES

$\underline{V_{OL}}$: $V_A = V_{DD}$, $V_B = V_{DD}$



Let $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)$

$I_L = I_{D1} = I_{D2}$



$$G_{EQV-ND2} = \frac{1}{\frac{1}{G}+\frac{1}{G}} = \frac{1}{2}G \Rightarrow k_{EQV-ND2} = \frac{1}{2}k_n$$

$$\Rightarrow \left(\frac{W}{L}\right)_{EQV-ND2} = \frac{1}{2}\left(\frac{W}{L}\right) = (W/L)_1 = (W/L)_2$$

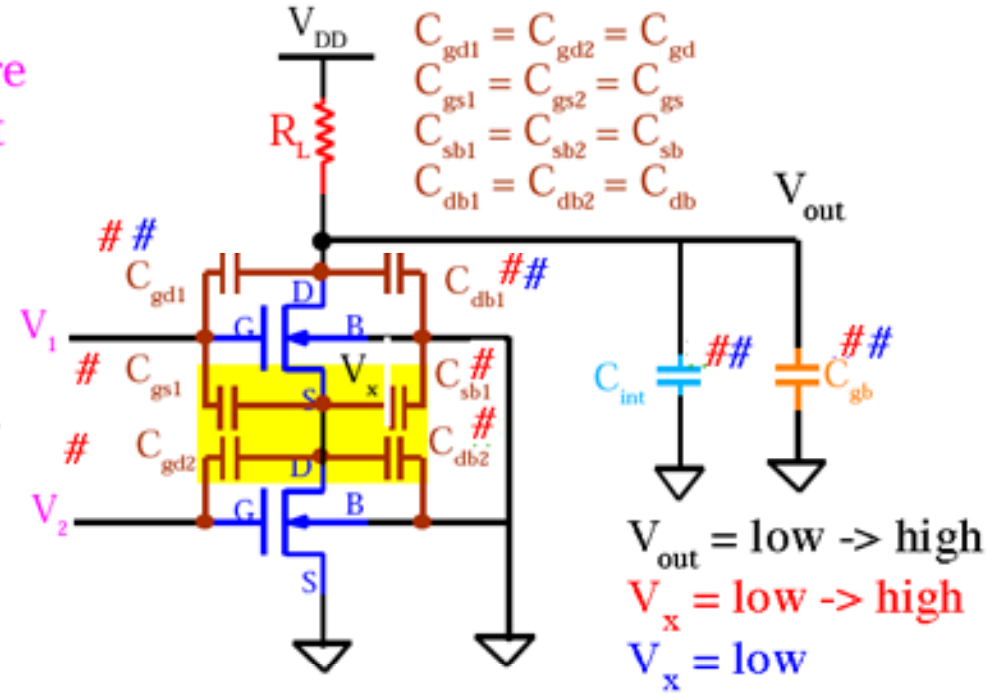
ND2 GATE WITH TWO nMOS (W/L):

$$k_{nEQV-ND2}R_L = \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL-ND2} + V_{OL-ND2}^2}$$

In Pull-Up C_{load} & τ_{PLH} are input pattern dependent

CASE1: $V_1 = V_{OH}$, $V_2 = V_{OH} \rightarrow V_{OL}$

CASE2: $V_1 = V_{OH} \rightarrow V_{OL}$, $V_2 = V_{OH}$



CASE1:

$$C_{load} = C_{gd1} + C_{gs1} + C_{db1} + C_{sb1} + C_{db2} + C_{gd2} + C_{int} + C_{gb} \text{ (worst case)}$$

$$\approx \boxed{C_{db1} + C_{sb1} + C_{db2}} + C_{int} + C_{gb} \text{ (worst case)}$$

$$= 3C_{db}$$

CASE2:

$$C_{load} = C_{gd1} + C_{db1} + C_{int} + C_{gb}$$

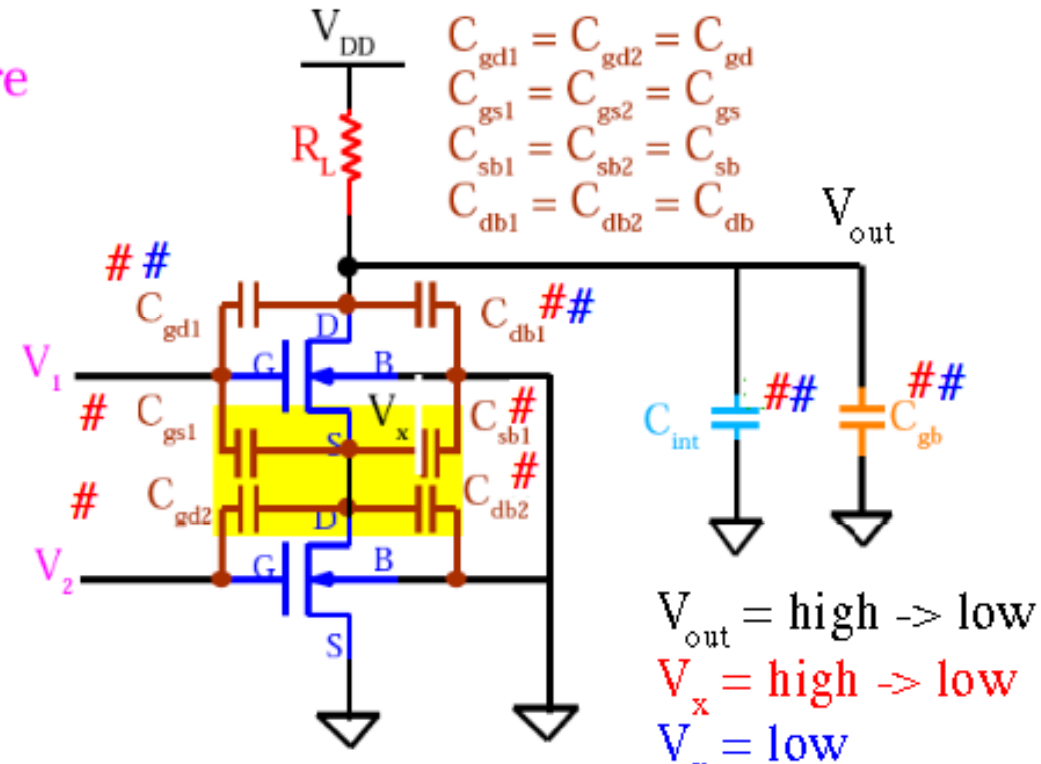
$$\approx C_{db1} + C_{int} + C_{gb}$$

$$\tau_{PLH1} > \tau_{PLH2}$$

In Pull-Down C_{load} & τ_{PHL} are input pattern dependent

CASE1: $V_1 = V_{OH}$, $V_2 = V_{OL} \rightarrow V_{OH}$

CASE2: $V_1 = V_{OL} \rightarrow V_{OH}$, $V_2 = V_{OH}$



CASE1:

$$C_{load} = C_{gd1} + C_{gs1} + C_{db1} + C_{sb1} + C_{db2} + C_{gd2} + C_{int} + C_{gb} \text{ (worst case)}$$

$$\approx C_{db1} + C_{sb1} + C_{db2} + C_{int} + C_{gb} \text{ (worst case)}$$

$$= 3C_{db}$$

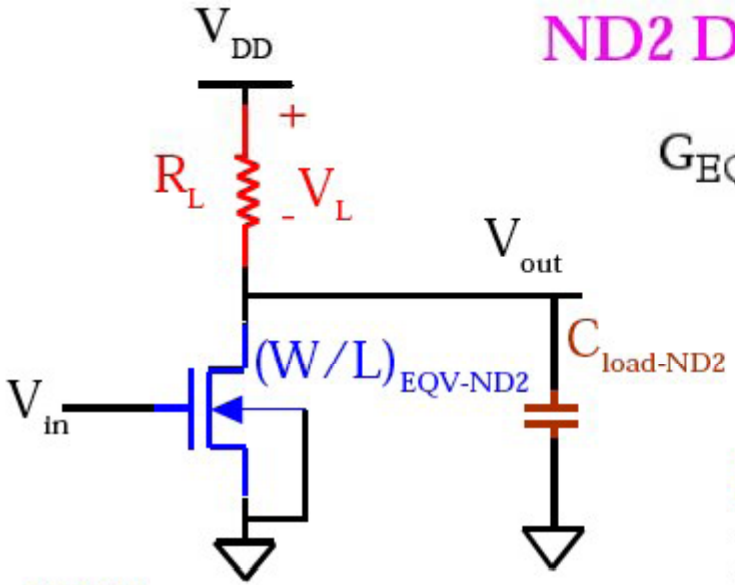
CASE2:

$$C_{load} = C_{gd1} + C_{db1} + C_{int} + C_{gb}$$

$$\approx C_{db1} + C_{int} + C_{gb}$$

$\tau_{PHL1} > \tau_{PHL2}$

ND2 DESIGN STRATEGY



$$G_{EQV-ND2} = \frac{1}{\frac{1}{G}+\frac{1}{G}} = \frac{1}{2}G \Rightarrow k_{EQV-ND2} = \frac{1}{2}k_n$$

$$\Rightarrow \left(\frac{W}{L}\right)_{EQV-ND2} = \frac{1}{2}\left(\frac{W}{L}\right)$$

FOR DESIGN:

1. Determine R_L and $(W/L)_{EQV-ND2}$
2. Set $(W/L)_1 = (W/L)_2 = (W/L) = 2(W/L)_{EQV-ND2}$

INV:

$$k_n R_L = \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL} + V_{OL}^2}$$

where $k_n = k_n'\left(\frac{W}{L}\right)$

ND2 GATE WITH TWO nMOS (W/L):

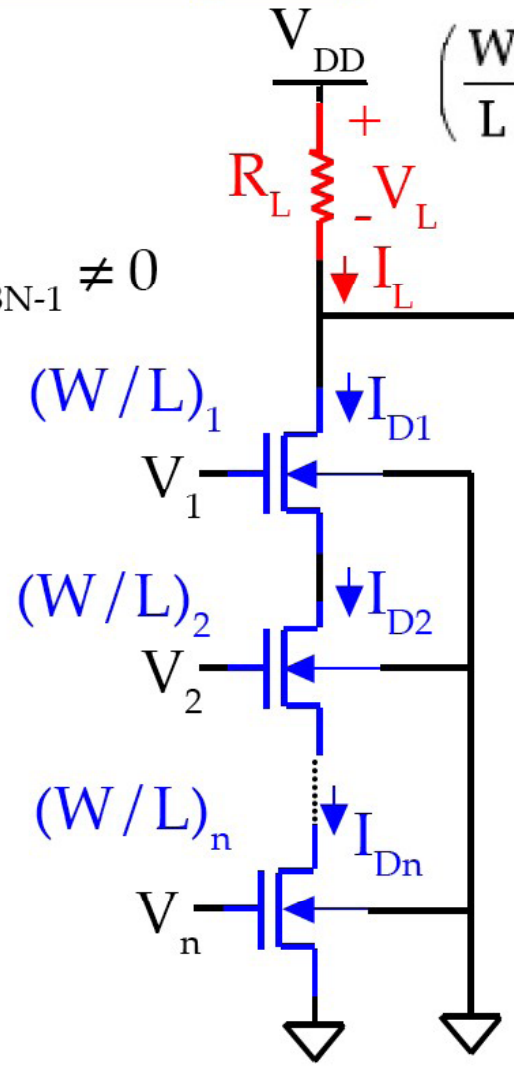
$$k_{nEQV-ND2} R_L = \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL-ND2} + V_{OL-ND2}^2}$$

where $k_n = 2k_{EQV-ND2}$

$$\tau_{PHL-ND2} = \frac{C_{load-ND2}}{k_{nEQV-ND2}(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL-ND2}} - 1\right)\right]$$

$C_{load-ND2} = 2C_{gd} + 2C_{db} + C_{gs} + C_{sb} + C_{int} + C_{gb}$ (worst case)

n INPUT NAND GATE (NDn)



$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \ldots\ldots = \left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)$$

NOTE: $V_{SB1}, .., V_{SBN-1} \neq 0$

If $V_1 = V_2 = \ldots = V_N = V_{in}$ &
$V_{T01} \approx V_{T02} \approx \ldots \approx V_{T0N} \approx V_{T0n}$

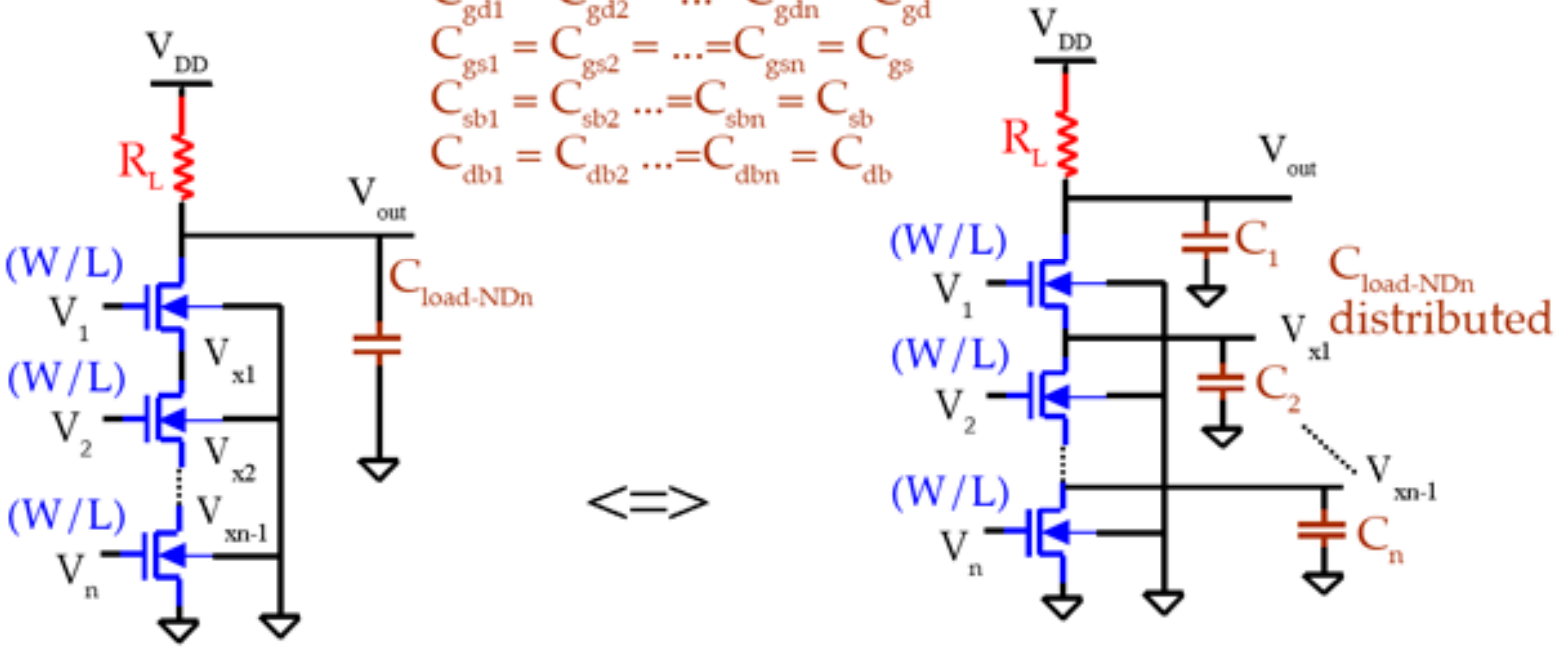
$$G_{EQV} = \frac{1}{\sum_{I=1}^{n} \frac{1}{G_i}} = \frac{1}{n} G$$

for all i=1, n (ON)

$$\left(\frac{W}{L}\right)_{EQV-NDn} = \frac{1}{n}\left(\frac{W}{L}\right)$$

$$= (W/L)_1$$
$$\vdots$$
$$= (W/L)_n$$

$C_{gd1} = C_{gd2} = \ldots = C_{gdn} = C_{gd}$
$C_{gs1} = C_{gs2} = \ldots = C_{gsn} = C_{gs}$
$C_{sb1} = C_{sb2} \ldots = C_{sbn} = C_{sb}$
$C_{db1} = C_{db2} \ldots = C_{dbn} = C_{db}$



Worst-case H-L: $V_1 = V_2 \ldots = V_{n-1} = V_{OH}$ and $V_n = V_{OL}$ -> V_{OH} => $V_{out} = V_{OH}$ -> V_{OL}

and V_{x1} = high -> low; V_{x2} = high -> low; ... ; V_{xn-1} = high -> low

Worst-case L-H: $V_1 = V_2 \ldots = V_{n-1} = V_{OH}$ and $V_n = V_{OH}$ -> V_{OL} => $V_{out} = V_{OL}$ -> V_{OH}

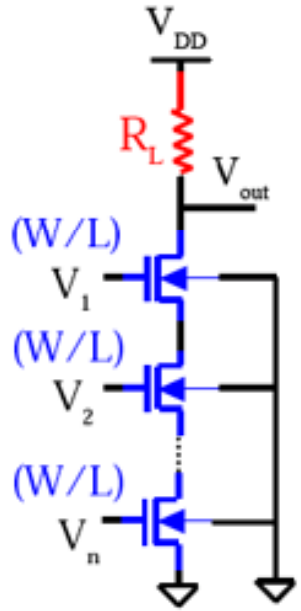
and V_{x1} = low -> high; V_{x2} = low -> high; ... ; V_{xn-1} = low -> high

$$C_{load\text{-}NDn} \approx \boxed{C_{db1} + C_{db2} + \ldots + C_{dbn} + C_{sb1} + C_{sb2} + \ldots + C_{sbn-1}} + C_{int} + C_{gb} \text{ (worst case)}$$

$$= (2n - 1)C_{db}$$

NDn DESIGN STRATEGY

$$\left(\frac{W}{L}\right)_{EQV-NDn} \approx \frac{1}{n}\left(\frac{W}{L}\right)$$



-> Find (W/L) ratio for EQV-NDn INVERTER to satisfy V_{OL} SPEC, i.e. for R_L find $(W/L)_{EQV\text{-}NDn}$.

-> Set all $(W/L) = n(W/L)_{EQV\text{-}NDn}$.

WHERE for EQV INV

$$k_{nEQV-NDn}R_L \approx \frac{2(V_{DD} - V_{T0n})}{2(V_{DD} - V_{T0n})V_{OL-NDn} + V_{OL-NDn}^2}$$

2. Design for delay for worst case $C_{load\text{-}NDn}$.

$$\tau_{PHL-NDn} \approx \frac{C_{load-NDn}}{k_{nEQV-NDn}(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL-NDn}} - 1\right)\right]$$

$$C_{load\text{-}NDn} \approx \boxed{C_{db1} + C_{db2} + \ldots + C_{dbn} + C_{sb1} + C_{sb2} + \ldots + C_{sbn-1}} + C_{int} + C_{gb} \text{ (worst case)}$$

$$= (2n - 1)C_{db}$$