Digital IC Design and Architecture

Third Edition

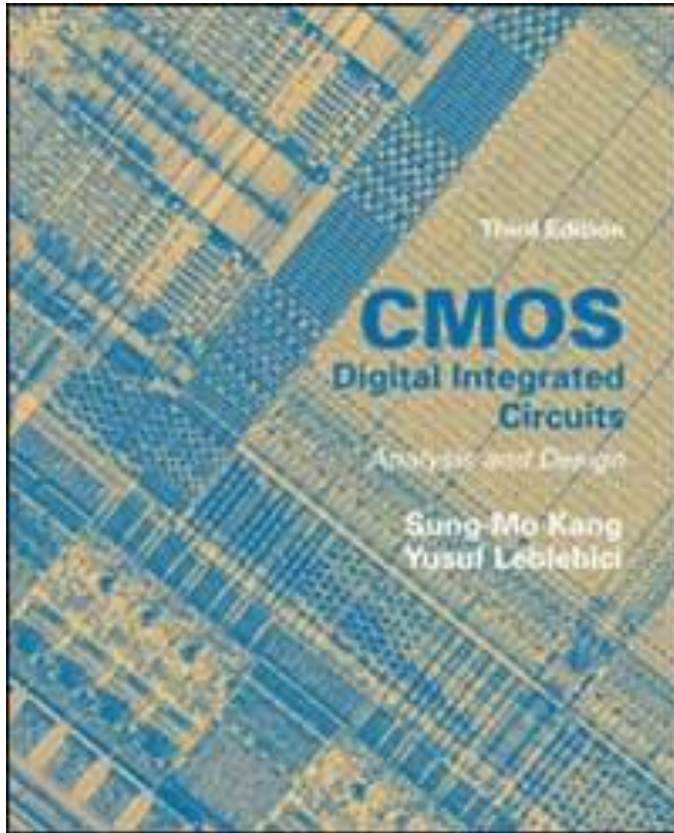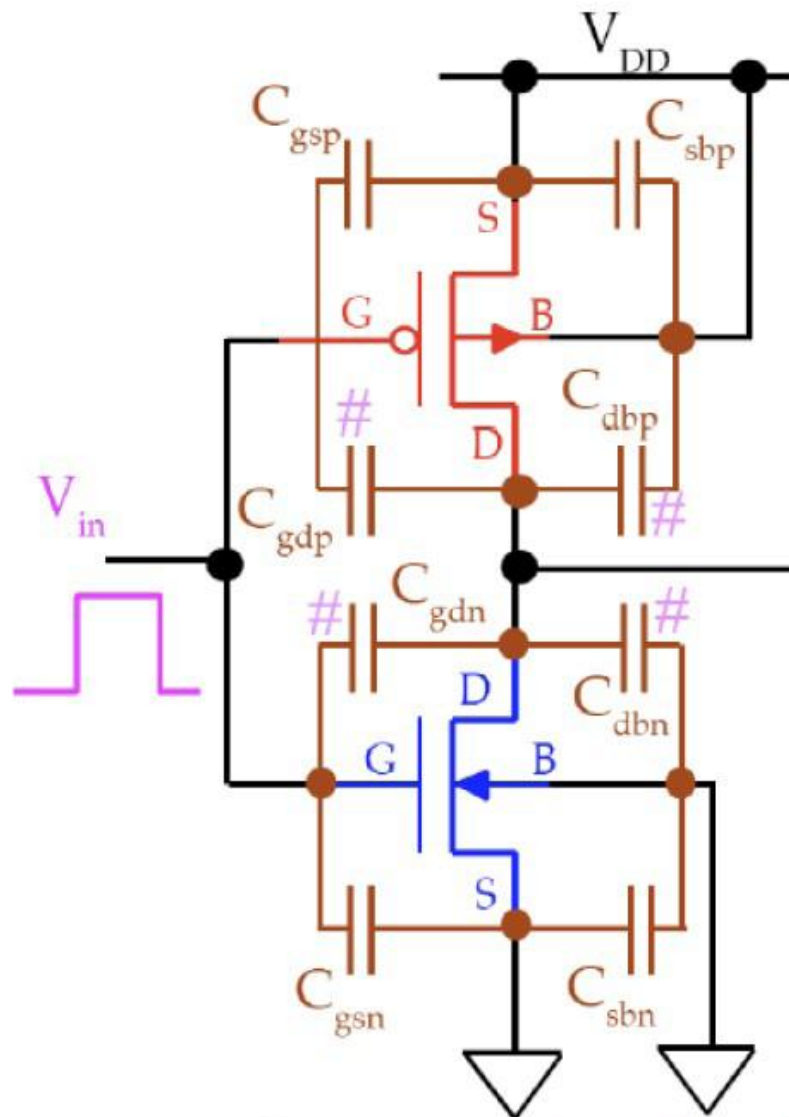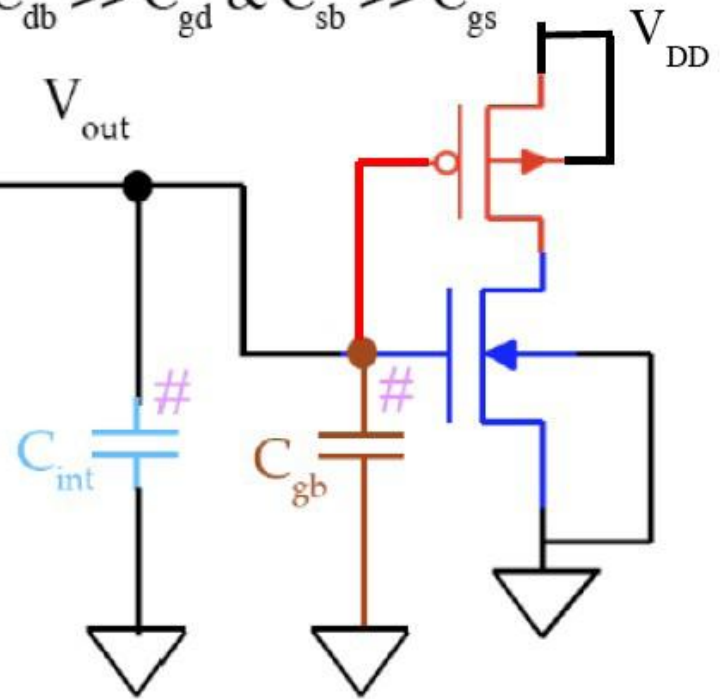**CMOS**
Digital Integrated Circuits
Analysis and Design

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MOS Inverter Dynamic Behavior

C_{gd}, C_{gs}, C_{gb} -> Oxide Caps
C_{db}, C_{sb} -> Junction Caps
C_{int} -> Inteconnect Cap
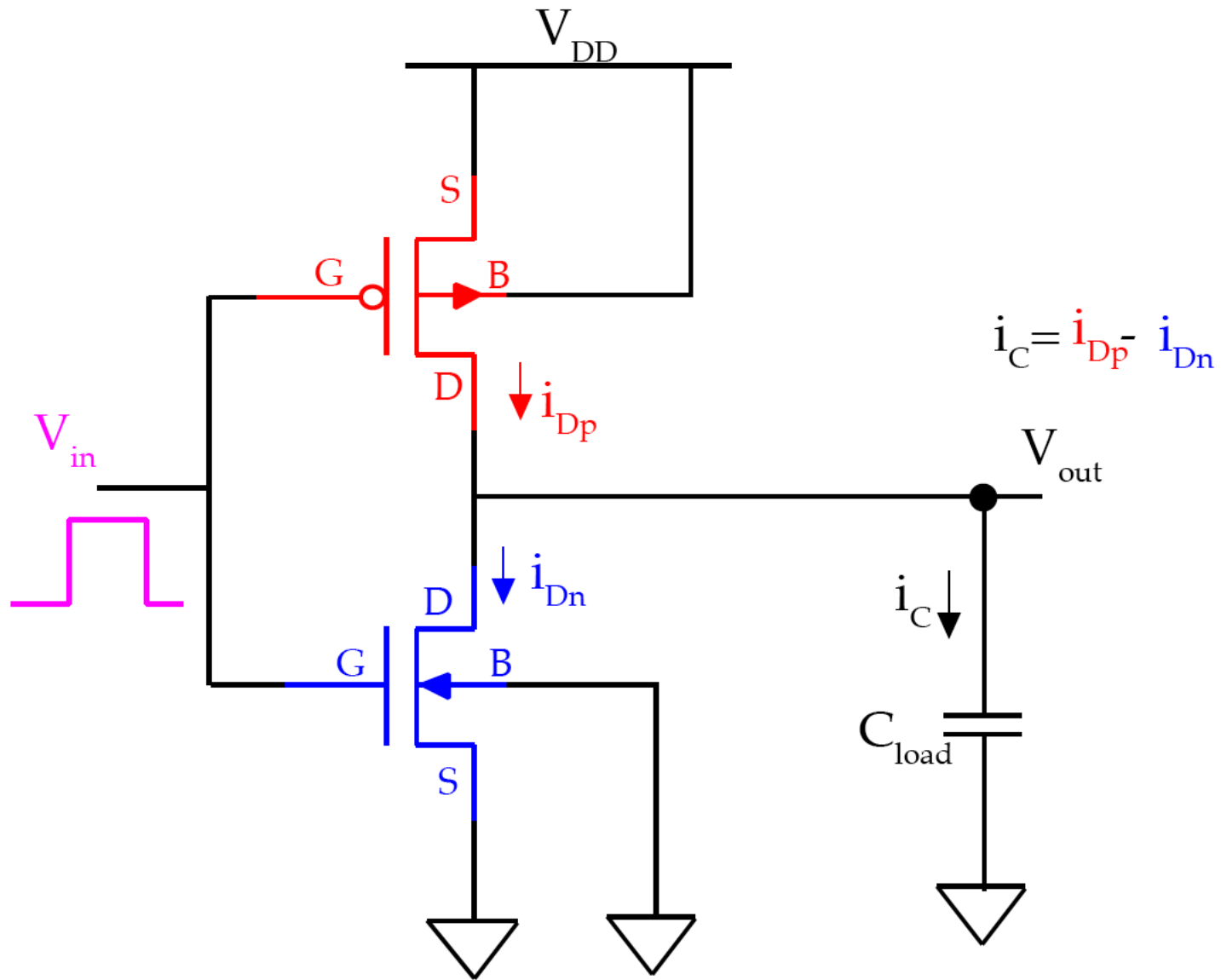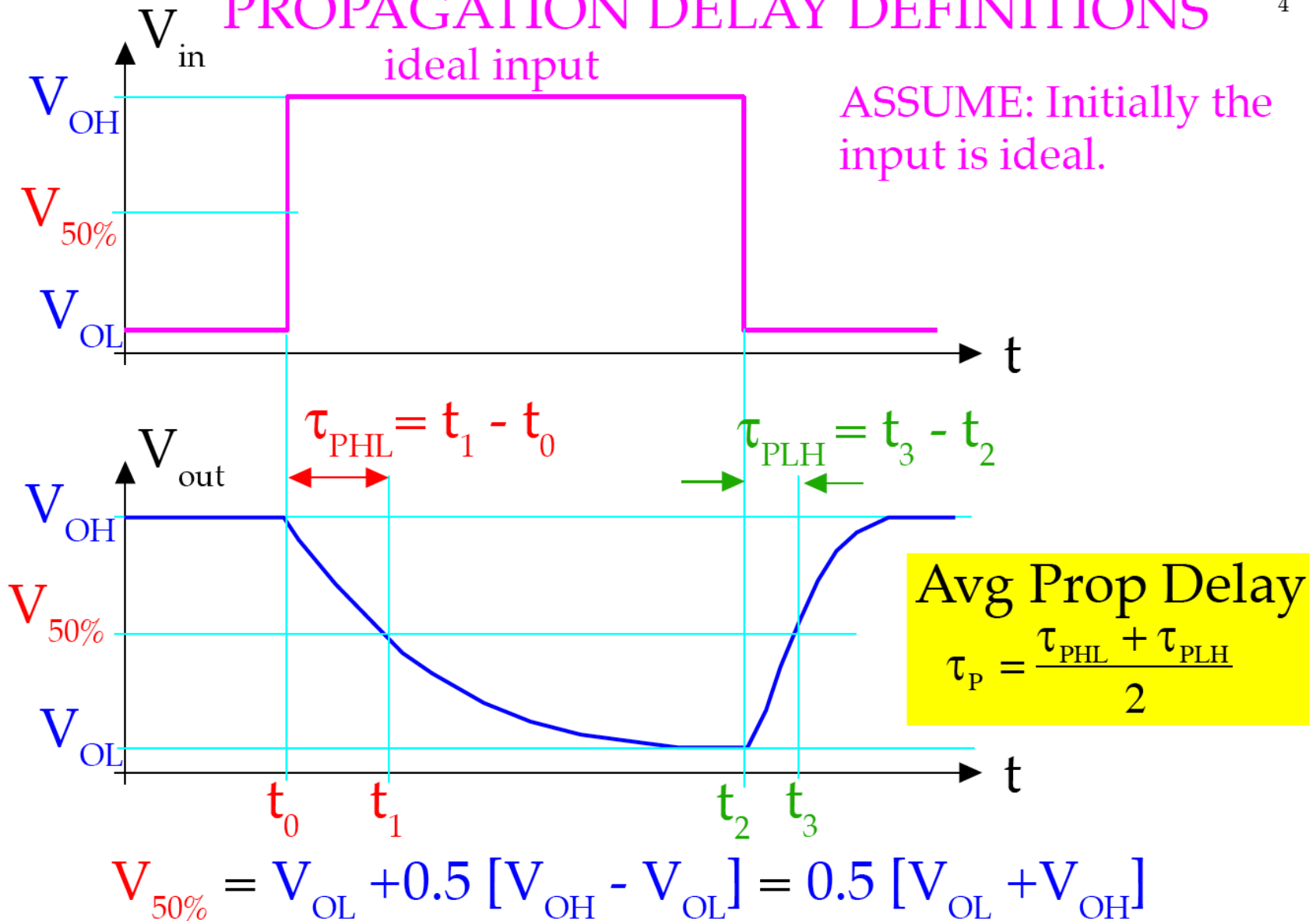
Usually
$C_{db} \gg C_{gd}$ & $C_{sb} \gg C_{gs}$

$$C_{load} = C_{dbn}^{\#} + C_{dbp}^{\#} + C_{gdn}^{\#} + C_{gdp}^{\#} + C_{int}^{\#} + C_{gb}^{\#} \approx C_{dbn} + C_{dbp} + C_{int} + \boxed{C_{gb}}$$

where $\boxed{C_{gb} = C_{gbn} + C_{gbp}}$

$$V_{DD}$$

S

G

B

$$i_C = i_{Dp} - i_{Dn}$$

D

$$\downarrow i_{Dp}$$

$$V_{in}$$

$$V_{out}$$

D

$$\downarrow i_{Dn}$$

$$i_C \downarrow$$

G

B

$$C_{load}$$

S

$$C_{load} = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{int} + C_{gb}$$

PROPAGATION DELAY DEFINITIONS

V_{in}

ideal input

V_{OH}

$V_{50\%}$

V_{OL}

t

ASSUME: Initially the input is ideal.

$\tau_{PHL} = t_1 - t_0$

$\tau_{PLH} = t_3 - t_2$

V_{out}

V_{OH}

$V_{50\%}$

V_{OL}

t

t_0 t_1 t_2 t_3

Avg Prop Delay

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

$$V_{50\%} = V_{OL} + 0.5 \left[V_{OH} - V_{OL} \right] = 0.5 \left[V_{OL} + V_{OH} \right]$$

V_{in}

non-ideal input

V_{OH}

$V_{50\%}$

V_{OL}

t

Avg Prop Delay

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

ASSUME: Initially the input is ideal.

V_{out}

$\tau_{PHL} = t_1 - t_0$

$\tau_{PLH} = t_3 - t_2$

V_{OH}

$V_{50\%}$

V_{OL}

t

t_0 t_1 t_2 t_3
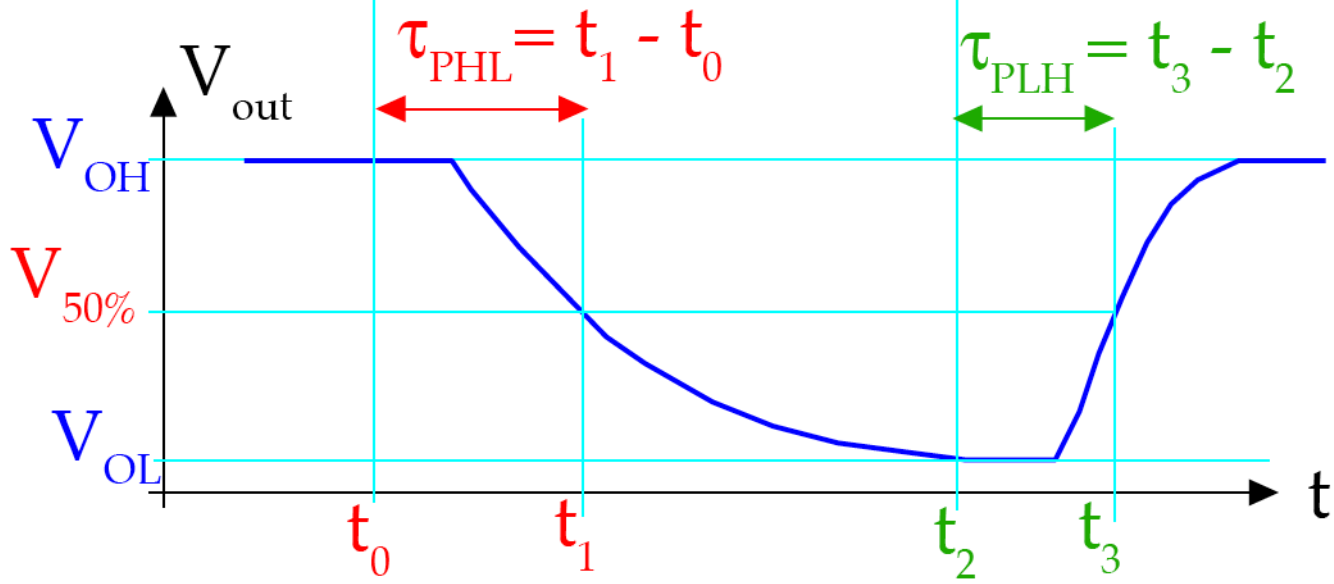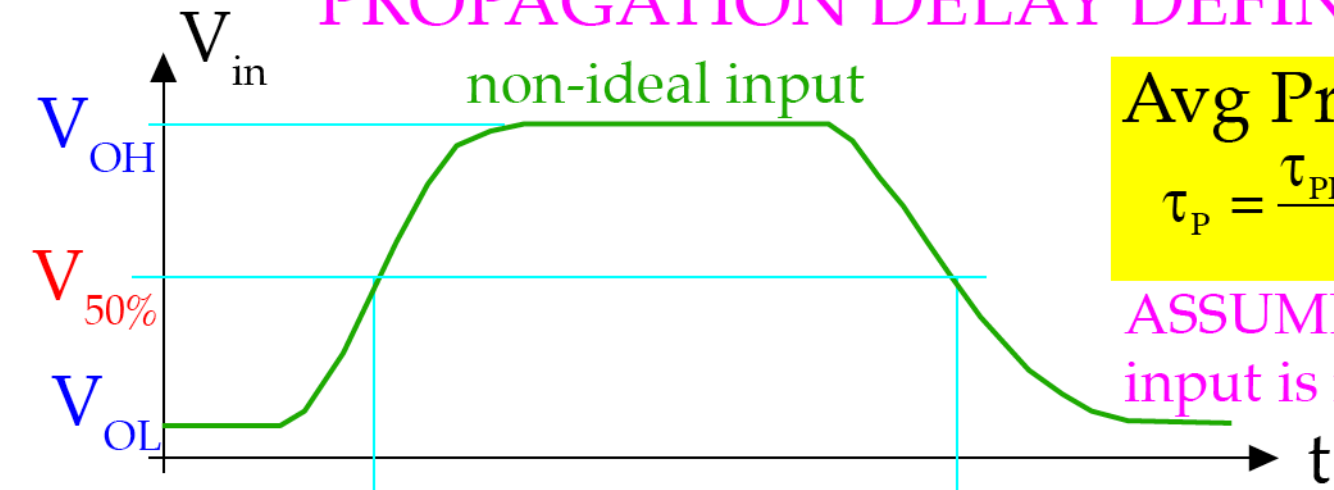
$$V_{50\%} = V_{OL} + 0.5 \, [V_{OH} - V_{OL}] = 0.5 \, [V_{OL} + V_{OH}]$$

OUTPUT VOLTAGE RISE & FALL TIMES
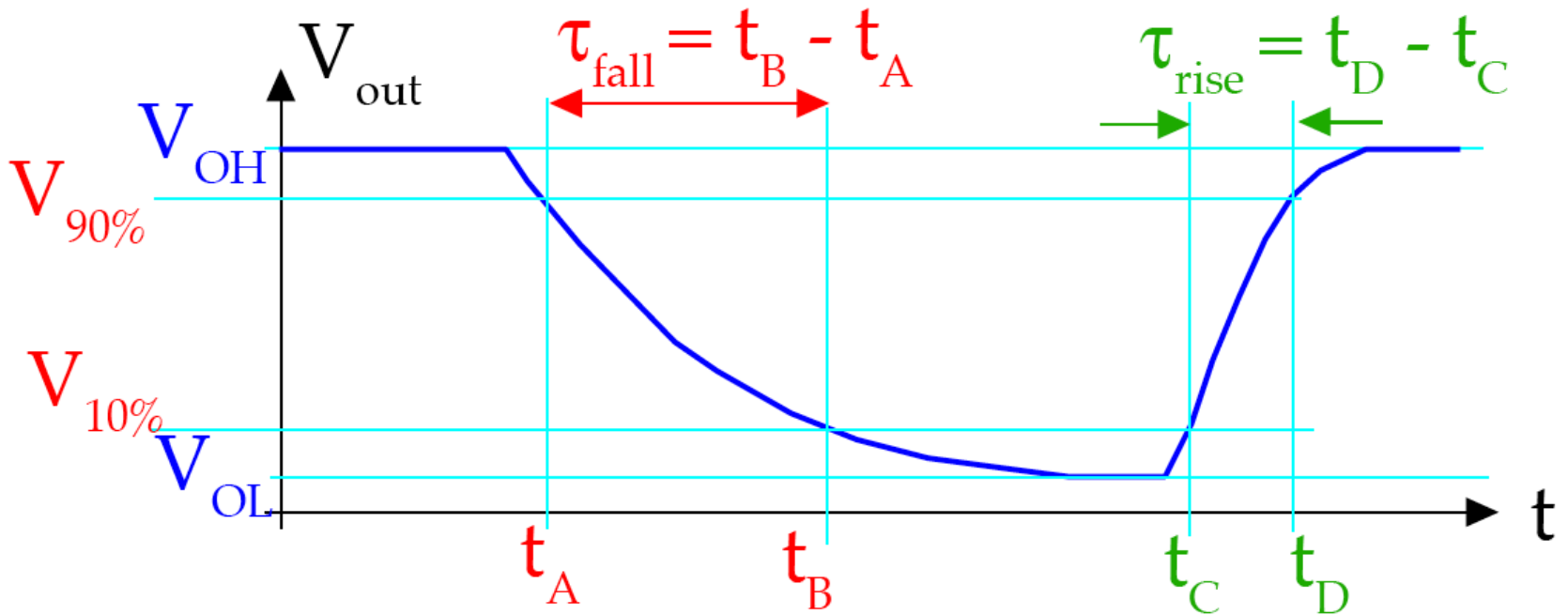
$$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$$
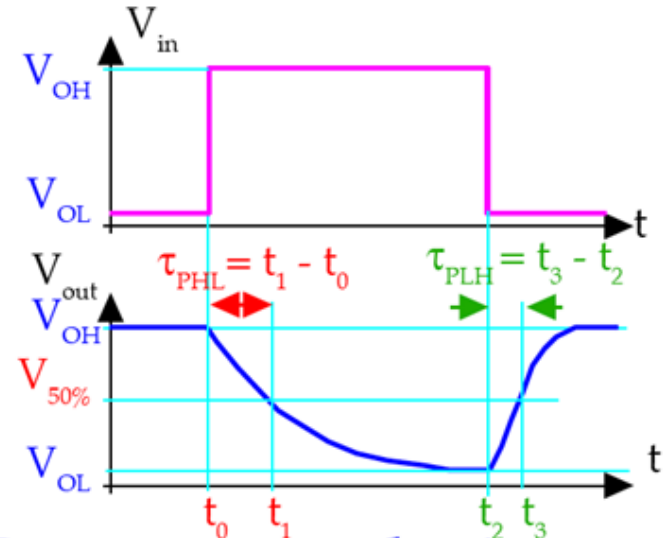
$$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$$

CALCULATION OF DELAY TIMES

$$I = C\frac{\Delta V}{\Delta t}$$

QUICK ESTIMATES:

$$\tau_{PHL} = \frac{C_{load}\,\Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load}(V_{OH} - V_{50\%})}{I_{avg,HL}}$$

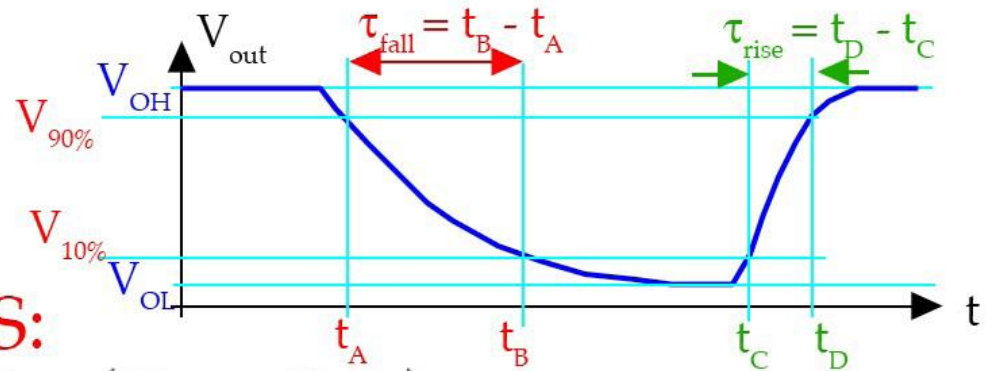$$\tau_{PLH} = \frac{C_{load}\,\Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load}(V_{50\%} - V_{OL})}{I_{avg,LH}}$$

$I_{avg,HL}$ -> approximate average C_{load} current during high-to-low V_{out} transition

$$I_{avg,HL} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{OH}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{50\%}\right)\right]$$

$I_{avg,LH}$ -> approximate average C_{load} current during low-to-high V_{out} transition

$$I_{avg,LH} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OL}, V_{out} = V_{OL}\right) + i_C\left(V_{in} = V_{OL}, V_{out} = V_{50\%}\right)\right]$$

$$i_C = i_{Dp} - i_{Dn}$$

QUICK ESTIMATES:

$$\tau_{fall} = \frac{C_{load}\Delta V_{90-to-10\%}}{I_{avg,90-to-10\%}} = \frac{C_{load}\left(V_{90\%} - V_{10\%}\right)}{I_{avg,90-to-10\%}}$$

$$\tau_{rise} = \frac{C_{load}\Delta V_{10-to-90\%}}{I_{avg,10-to-90\%}} = \frac{C_{load}\left(V_{90\%} - V_{10\%}\right)}{I_{avg,10-to-90\%}}$$

$I_{avg,90-to-10\%}$ -> approximate average C_{load} current during 90%-to-10% V_{out} transition

$$I_{avg,90-to-10\%} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{90\%}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{10\%}\right)\right]$$

$I_{avg,10-to90\%}$ -> approximate average C_{load} current during 10%-to-90% V_{out} transition

$$I_{avg,10-to-90\%} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OL}, V_{out} = V_{10\%}\right) + i_C\left(V_{in} = V_{OL}, V_{out} = V_{90\%}\right)\right]$$

Calculating Propagation Delays By Solving the Circuit Differential Equation

MORE ACCURATE CALCULATION OF τ_{PHL}, τ_{PLH}:
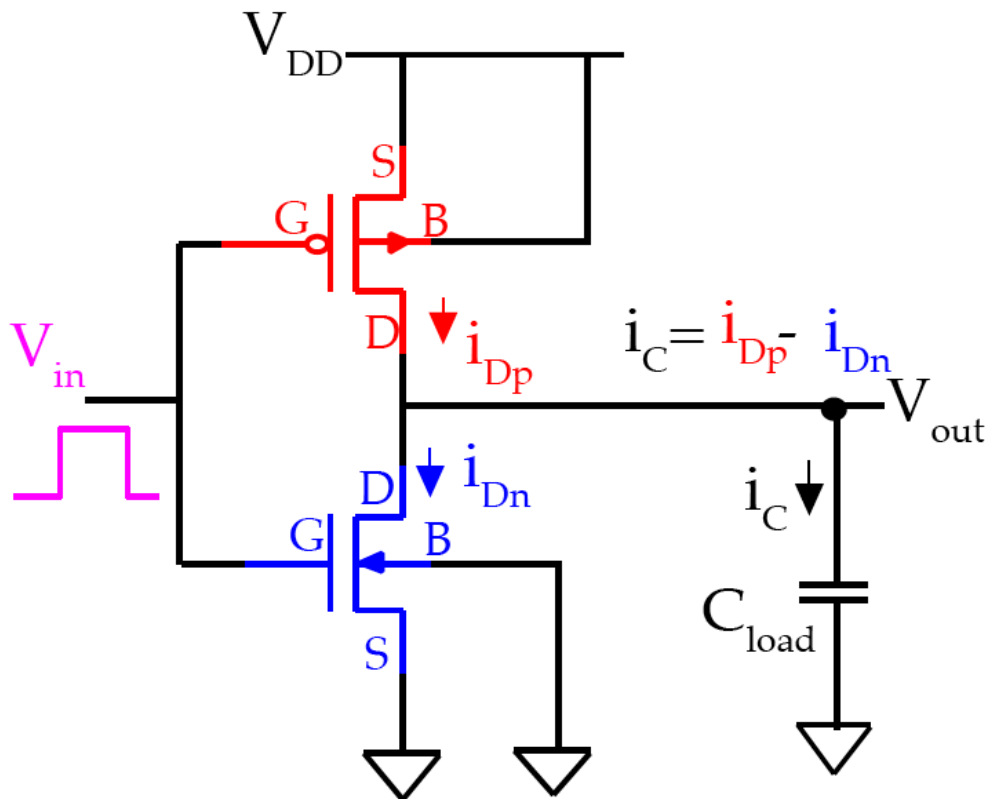
$$i_C = i_{Dp} - i_{Dn}$$

$$i_C = C_{load} \frac{dV_{out}}{dt} = i_{Dp} - i_{Dn}$$

1) V_{in} - ABRUPTLY RISES CASE:

IC: $V_{out} = V_{DD}$, $V_{in} = 0 \rightarrow V_{DD}$

nMOS - ON SAT $V_{out} \geqslant V_{DD} - V_{T0n}$

p-MOS OFF LIN $0 \leqslant V_{out} < V_{DD} - V_{T0n}$
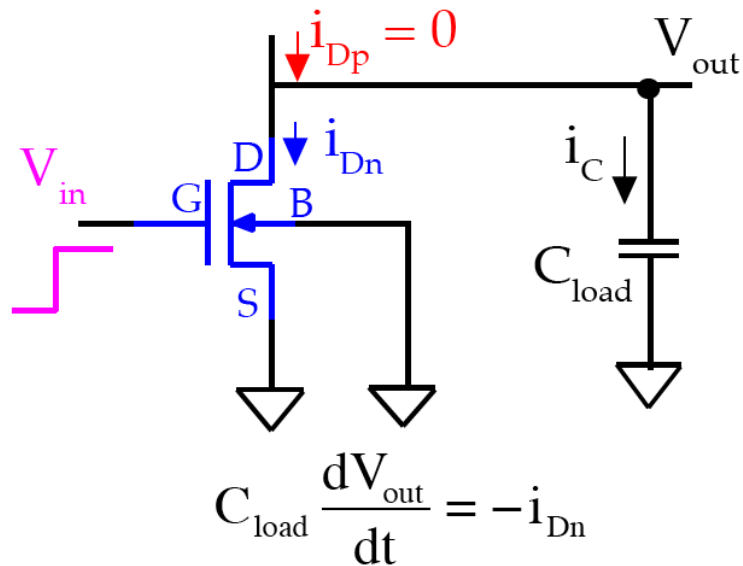
$$C_{load} \frac{dV_{out}}{dt} = -i_{Dn}$$

NOTE THAT:

$|i_{Dp}| \ll |i_{Dn}|$ for all inverter types

$V_{OH} = V_{DD}$

$V_{OL} = 0$

$\tau_{PHL} = t_{50\%} - t_0$

$V_{OH} = V_{DD}$

$V_{DD} - V_{T0n}$

$V_{50\%}$

$V_{OL} = 0$

$t_0 \quad t_1' \quad t_{50\%}$

nMOS SAT
nMOS LIN

9
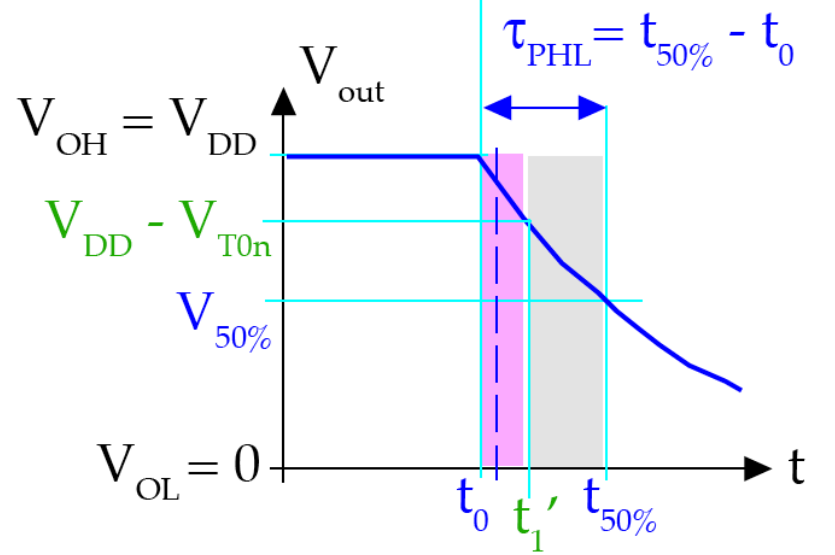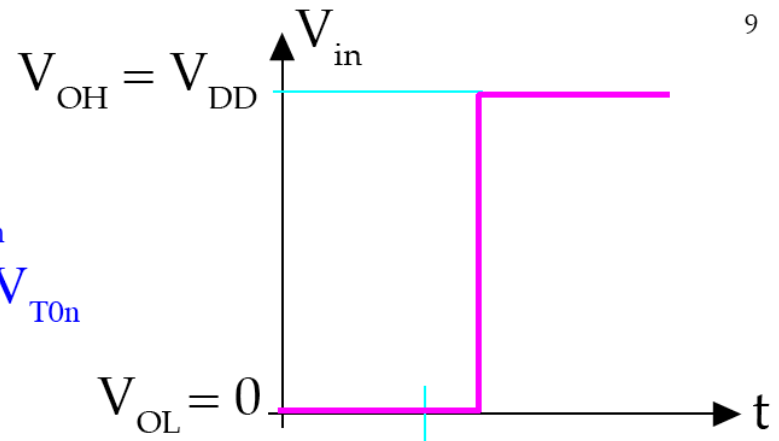
CMOS Inverter Revisited

CMOS INV

$$V_{in} = V_{GSn} = V_{GSp} + V_{DD}$$

$$V_{SBp} = 0$$

$$V_{SBn} = 0$$

$$V_{out} = V_{DSn} = V_{DSp} + V_{DD}$$

τ_{PHL}

$V_{OH} = V_{DD}$

V_{in}

$V_{OL} = 0$

t

V_{out}

V_{DD}

$V_{OH} - V_{T0n}$

$V_{50\%}$

0

t

$\tau_{PHL} = t_{50\%} - t_0$

nMOS SAT
nMOS LIN

t_0 t_1' $t_{50\%}$
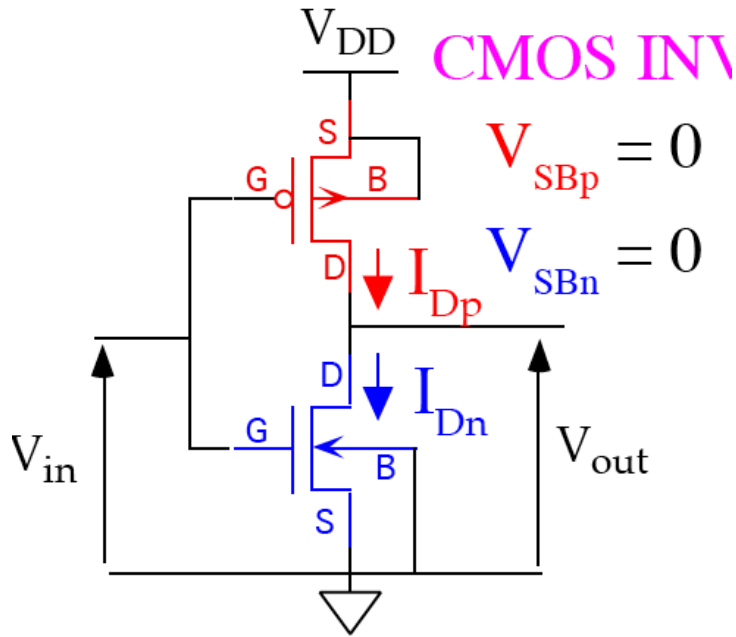
Since i_{Dn} is INDEP of V_{out}
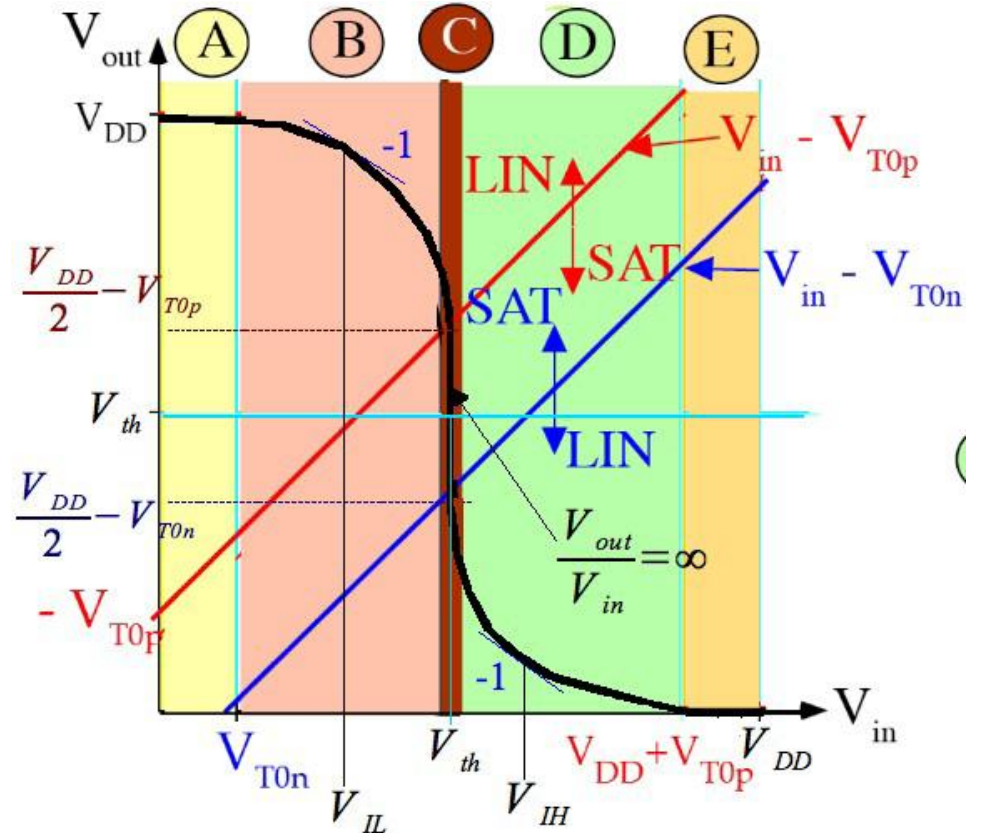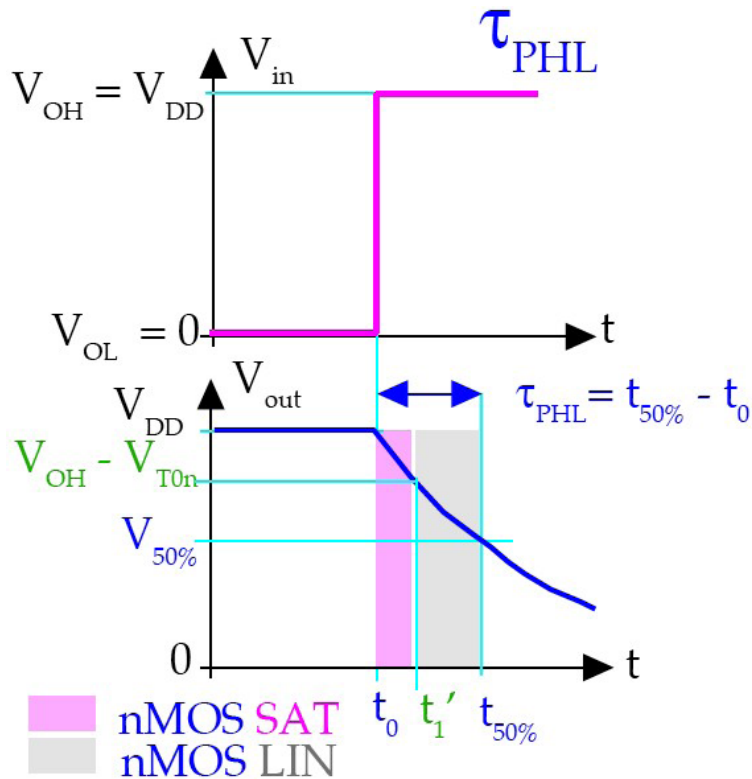
$t_0 < t < t_1'$:

$$i_{Dn} = \frac{k_n}{2}(V_{in} - V_{T0n})^2 = -i_C$$

$$\frac{k_n}{2}(V_{OH} - V_{T0n})^2 = -C_{load}\frac{dV_{out}}{dt}$$

for $V_{OH} - V_{T0n} < V_{out} \leq V_{OH}$

$$i_{Dn} = -C_{load}\frac{dV_{out}}{dt} \Rightarrow \boxed{dt = -\frac{C_{load}}{i_{Dn}}dV_{out}}$$

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}}\left(\frac{1}{i_{Dn}}\right)dV_{out}$$

$$\int_{t=t_0}^{t=t_1'} dt = -\frac{C_{load}}{\frac{k_n}{2}(V_{OH} - V_{T0n})^2}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}}dV_{out}$$

$$\boxed{t_1' - t_0 = \frac{2C_{load}V_{T0n}}{k_n(V_{OH} - V_{T0n})^2}}$$
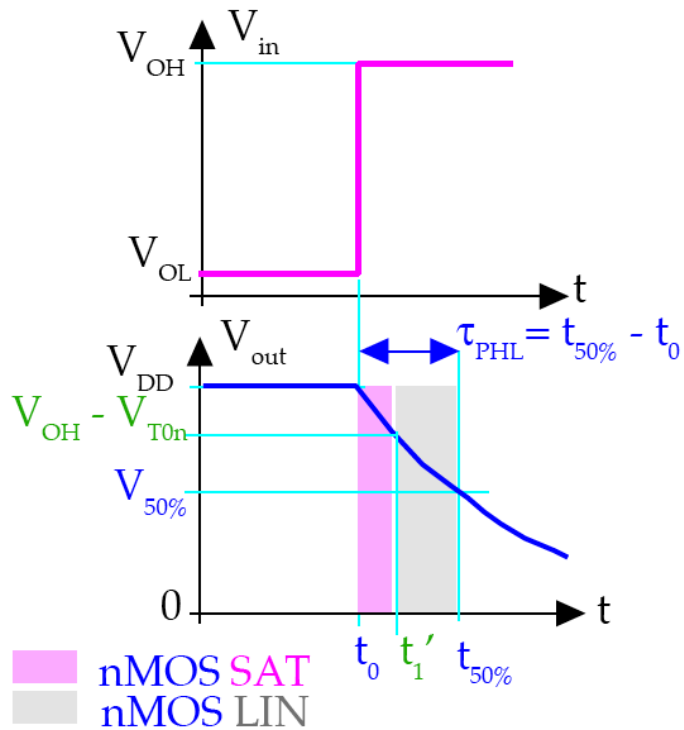
$$t_1' < t < t_{50\%}:$$

$$i_{Dn} = \frac{k_n}{2}\left[2(V_{in} - V_{T0n})V_{out} - V_{out}^2\right]$$

$$\tau_{PHL} = t_{50\%} - t_0 = \frac{k_n}{2}\left[2(V_{OH} - V_{T0n})V_{out} - V_{out}^2\right] = -C_{load}\frac{dV_{out}}{dt}$$

$$\text{for} \quad V_{out} \le V_{OH} - V_{T0n}$$

$$\int_{t=t_1'}^{t=t_{50\%}} dt = -C_{load}\int_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}}\left(\frac{1}{i_{Dn}}\right)dV_{out}$$

$$\int_{t=t_1'}^{t=t_{50\%}} dt = -\frac{2C_{load}}{k_n}\int_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}}\left(\frac{1}{2(V_{OH}-V_{T0n})V_{out} - V_{out}^2}\right)dV_{out}$$

$$t_{50\%} - t_1' = -\frac{2C_{load}}{k_n}\frac{1}{2(V_{OH}-V_{T0n})}\ln\left(\frac{V_{out}}{2(V_{OH}-V_{T0n})-V_{out}}\right)\Big|_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}}$$

nMOS SAT
nMOS LIN

$$t_{50\%} - t_1' = -\frac{2C_{load}}{k_n} \frac{1}{2(V_{OH} - V_{T0n})} \ln\left(\frac{V_{out}}{2(V_{OH} - V_{T0n}) - V_{out}}\right)\bigg|_{\substack{V_{out} = V_{50\%} \\ V_{out} = V_{OH} - V_{T0n}}}$$

$$= \frac{C_{load}}{k_n(V_{OH} - V_{T0n})} \ln\left(\frac{2(V_{OH} - V_{T0n}) - V_{50\%}}{V_{50\%}}\right)$$

$$\longrightarrow \quad t_1' - t_0 = \frac{2C_{load}V_{T0n}}{k_n(V_{OH} - V_{T0n})^2}$$

$$\tau_{PHL} = t_{50\%} - t_1' + t_1' - t_0$$

$$\tau_{PHL} = \frac{2C_{load}V_{T0n}}{k_n(V_{OH} - V_{T0n})^2} + \frac{C_{load}}{k_n(V_{OH} - V_{T0n})} \ln\left(\frac{2(V_{OH} - V_{T0n}) - V_{50\%}}{V_{50\%}}\right)$$

$$= \frac{C_{load}}{k_n(V_{OH} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{2(V_{OH} - V_{T0n})}{V_{50\%}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{OH} - V_{T0n})}\left[\frac{2\,V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{2(V_{OH} - V_{T0n})}{V_{50\%}} - 1\right)\right]$$

SUBSTITUTING $V_{50\%} = 0.5\,[V_{OL} + V_{OH}]$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{OH} - V_{T0n})}\left[\frac{2\,V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL}} - 1\right)\right]$$

WHERE for CMOS Inverters $V_{OL} = 0$, $V_{OH} = V_{DD}$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2\,V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

Fall Time: τ_{fall}
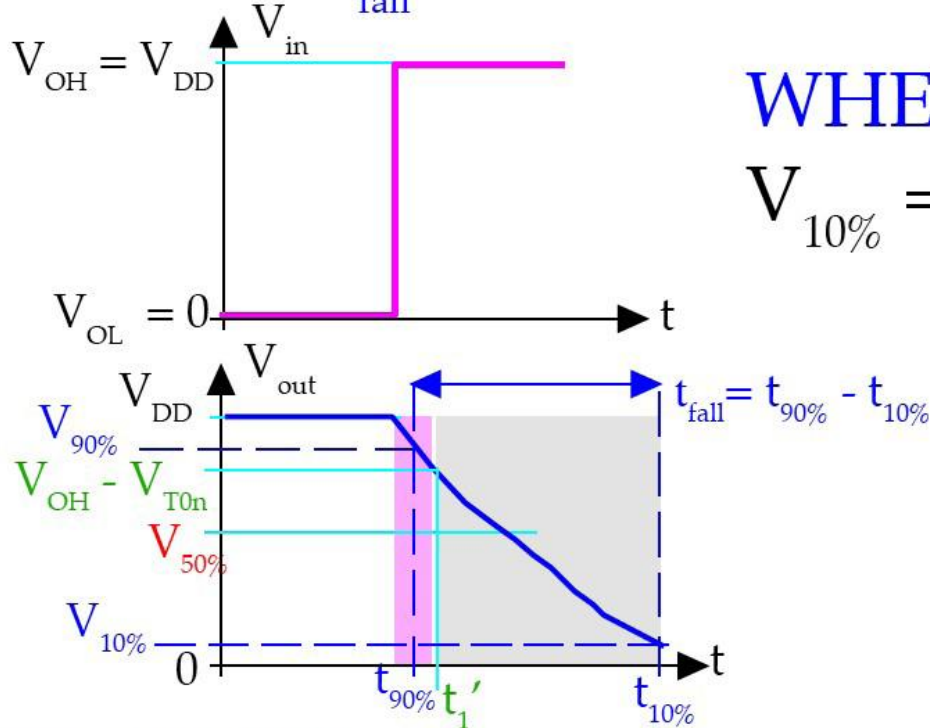
WHERE for CMOS Inverters

$$V_{10\%} = 0.1V_{DD}, \ V_{90\%} = 0.9V_{DD}$$

$t_{fall} = t_{90\%} - t_{10\%}$

nMOS SAT
nMOS LIN

$$\tau_{fall} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2(V_{T0n} - 0.1V_{DD})}{V_{DD} - V_{T0n}} + \ln\left(\frac{2(V_{DD} - V_{T0n})}{0.1V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{2(V_{DD} - V_{T0n})}{0.5V_{DD}} - 1\right)\right]$$

EXAMPLE 6.1

Consider a CMOS inverter with $C_{load} = 1.0$ pF, where the IV characteristics of the nMOS transitor driver are specified as follows:

$$V_{GSn} = 5 \text{ V and } V_{DSn} \geqslant 4V \implies i_{Dn} = i_{Dnsat} = 5 \text{ mA}$$

Assume V_{in} is a step pulse that switches instantaneously from 0 to 5 V. Calculate the delay time necessary for the inverter output to fall from its initial value of 5 V to 2.5 V.

$$V_{50\%} = 0.5 [V_{OL} + V_{OH}] = 0.5 [0 + 5 \text{ V}] = 2.5 \text{ V}$$

1. FROM IV DATA: Determine V_{T0n} and k_n

nMOS in SAT $\implies V_{DSn} = 5V - V_{T0n} = 4 \text{ V} \implies V_{T0n} = 1 \text{ V}$

Using $\quad i_{Dnsat} = \dfrac{k_n}{2} (V_{GS} - V_{T0n})^2 = 5 \text{ mA}$

$$k_n = \frac{2 i_{Dnsat}}{(V_{GS} - V_{T0n})^2} = \frac{2 \times 5 \text{ mA}}{(4 \text{ V})^2} = 0.625 \times 10^{-3} \text{ A} / \text{V}^2$$

2. $t_0 < t < t_1'$:

where $i_{Dn} = I_{Dnsat} = 5\,\text{mA}$

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

$V_{OH} - V_{T0n} = 4\,\text{V}$

$V_{OH} = 5\,\text{V}$

$$t_1' - t_0 = -\frac{C_{load}}{i_{Dnsat}} \int_{V_{out}=5V}^{V_{out}=4V} dV_{out} = -\frac{1\text{pF}}{5\,\text{mA}}(-1\,\text{V}) = 0.2\,\text{nS}$$

UNITS $\boxed{\dfrac{C_{Load}}{i_{Dnsat}}\Delta V = \dfrac{F}{A}V = \dfrac{C/V}{C/s}V = s}$

3. $t_1' < t < t_1$:

$$t_1 - t_1' = \frac{C_{load}}{k_n(V_{OH} - V_{T0n})} \ln\left(\frac{2(V_{OH} - V_{T0n}) - V_{50\%}}{V_{50\%}}\right)$$

$$= \frac{1\text{pF}}{(0.625 \times 10^3\,\text{A/V}^2)(5-1)\,\text{V}} \ln\left(\frac{2(5-1)\,\text{V} - 2.5\,\text{V}}{2.5\,\text{V}}\right)$$

$$= \frac{1 \times 10^{-12}\,\text{F}}{(0.625 \times 10^3\,\text{A/V}^2)\,4\,\text{V}} \ln\left(\frac{5.5}{2.5}\right) = 1.26\,\text{ns}$$

$$\tau_{PHL} = 0.2\,\text{ns} + 1.26\,\text{ns} = 1.46\,\text{ns}$$

2) V_{in} - ABRUPTLY FALLS CASE:

IC: $V_{out} = V_{OL}, V_{in} = V_{OH} \rightarrow V_{OL} = 0$

nMOS - OFF   SAT $V_{out} \leqslant V_{in} - V_{T0p} = -V_{T0p}$

p-MOS ON   LIN $V_{out} > -V_{T0p}$

$V_{GS} = V_{in} - V_{DD}$ $V_{DS} = V_{out} - V_{DD}$

$$C_{load} \frac{dV_{out}}{dt} = i_{Dp}$$

$i_C = i_{Dp}$

$i_{Dn} = 0$

$\tau_{PLH} = t_{50\%} - t_0$
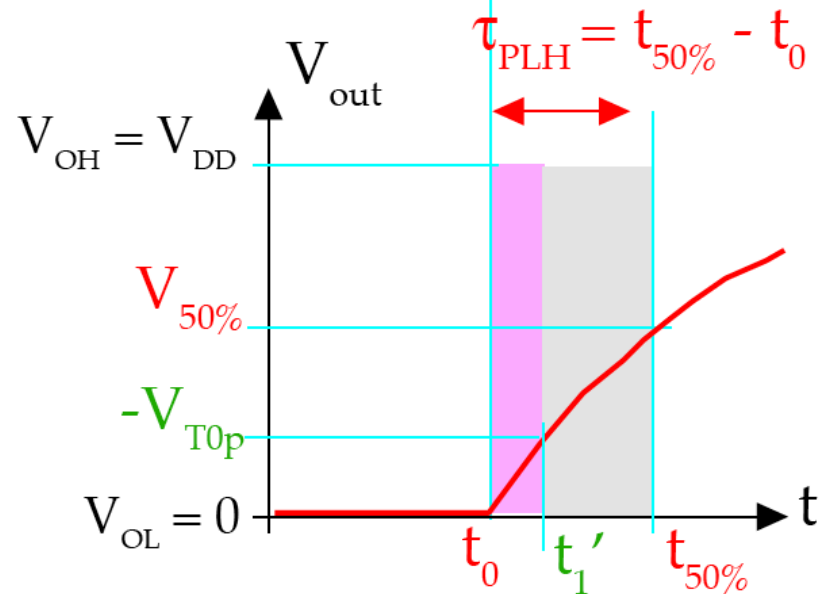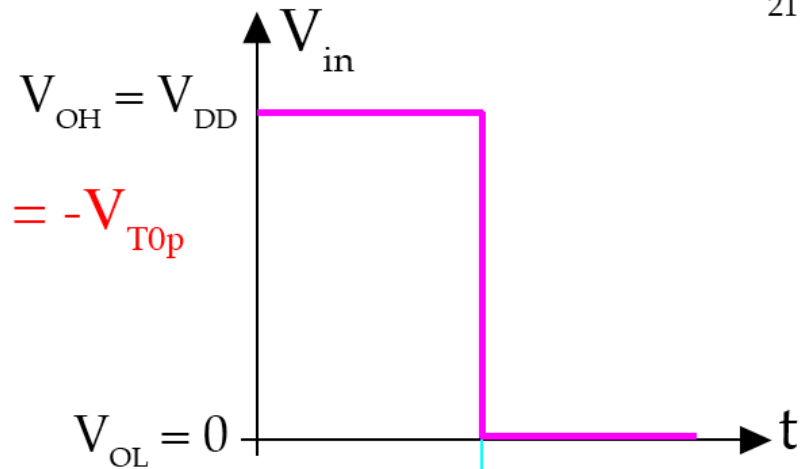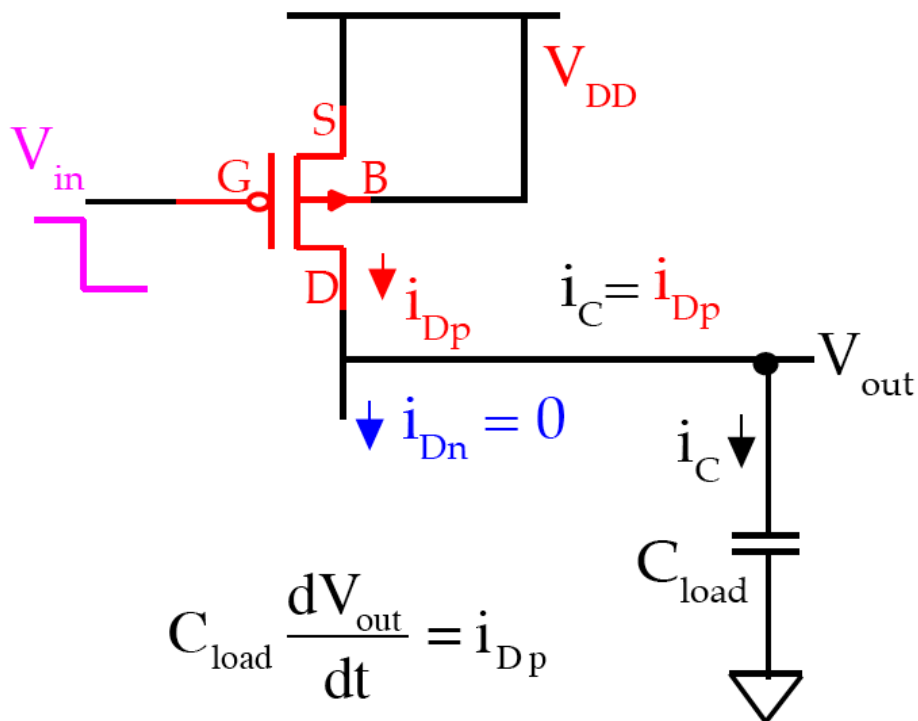
pMOS SAT

pMOS LIN

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{OH} - V_{OL} - |V_{T0p}|)} \left[\frac{2|V_{T0p}|}{V_{OH} - |V_{T0p}|} \right.$$

$$\left. + \ln\left(\frac{2(V_{OH} - V_{OL} - |V_{T0p}|)}{V_{OH} - V_{50\%}} - 1 \right) \right]$$

$V_{50\%} = 0.5\,[V_{OL} + V_{OH}],$ FOR CMOS INV: $V_{OL} = 0,\ V_{OH} = V_{DD}$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)} \left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1 \right) \right]$$

$$\tau_{rise} = \frac{C_{load}}{k_p\left(V_{DD} - |V_{T0p}|\right)} \left[\frac{2\left(|V_{T0p}| - 0.1V_{DD}\right)}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{2\left(V_{DD} - |V_{T0p}|\right)}{0.1V_{DD}} - 1 \right) \right]$$

FOR CMOS INV: $V_{OL} = 0,\ V_{OH} = V_{DD}$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1 \right) \right]$$

CONDITIONS FOR Balanced CMOS Inverter Propagation
Delays, i.e. $\tau_{PHL} = \tau_{PLH}$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

where $\quad k_n = \mu_n C_{ox} \frac{W_n}{L_n} \quad$ & $\quad k_p = \mu_p C_{ox} \frac{W_p}{L_p}$

FOR $\tau_{PHL} = \tau_{PLH}$

$$V_{T0n} = |V_{T0p}|$$

$$k_n = k_p \qquad \text{or} \qquad \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n}$$

OBSERVATIONS

$$\tau_{PHL} = \frac{C_{load}L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{1}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}L_p}{\mu_n C_{ox}(V_{DD} - |V_{T0p}|)}\left(\frac{1}{W_p}\right)\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

- Calculation of τ_{PHL}, depends largely on NMOS driver, i.e. nearly same for all INV types.
- Calculation of τ_{PLH}, depends largely on the load device and its operation, i.e. different for all INV types.
- Options to reduce τ_{PHL}, τ_{PLH}:
  - Decrease C_{load}
  - Increase V_{DD}
  - Increase W/L ratio (which usually means increasing W)
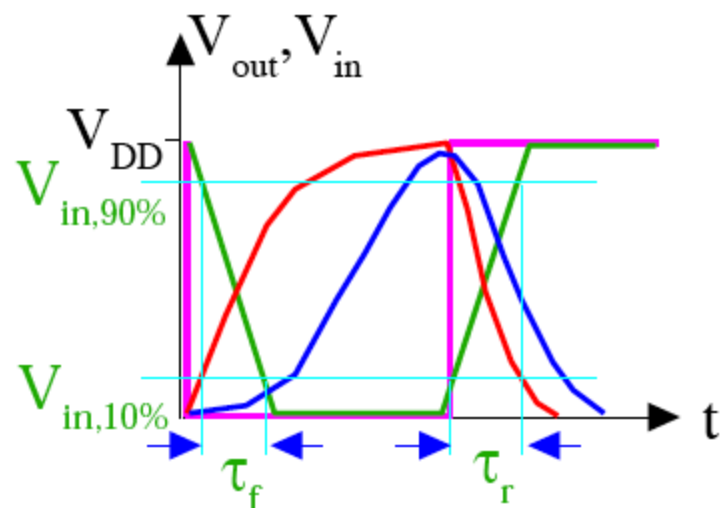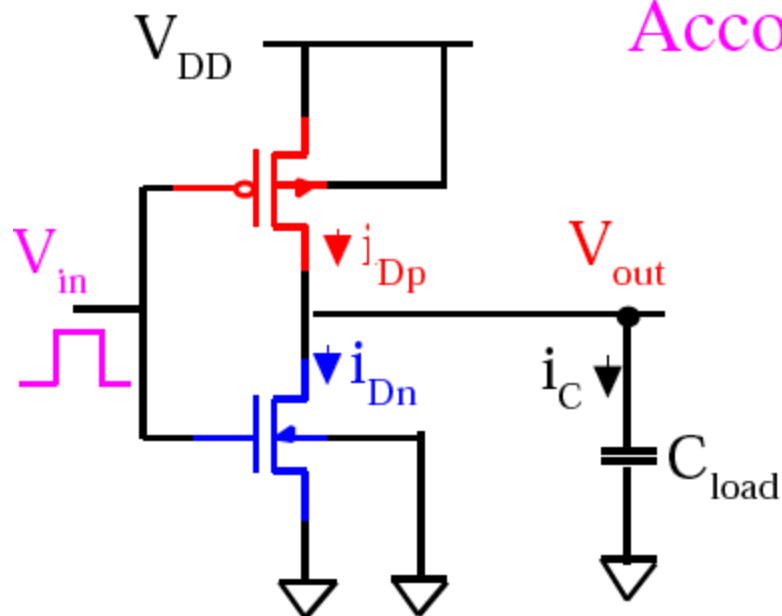
EMPERICAL DELAY
CORRECTIONS FOR INPUT τ_r, τ_f:

$$\tau_{PHL}(\text{actual}) = \sqrt{\tau_{PHL}^2(\text{step}-\text{input}) + \left(\frac{\tau_r}{2}\right)^2}$$

$$\tau_{PLH}(\text{actual}) = \sqrt{\tau_{PLH}^2(\text{step}-\text{input}) + \left(\frac{\tau_f}{2}\right)^2}$$
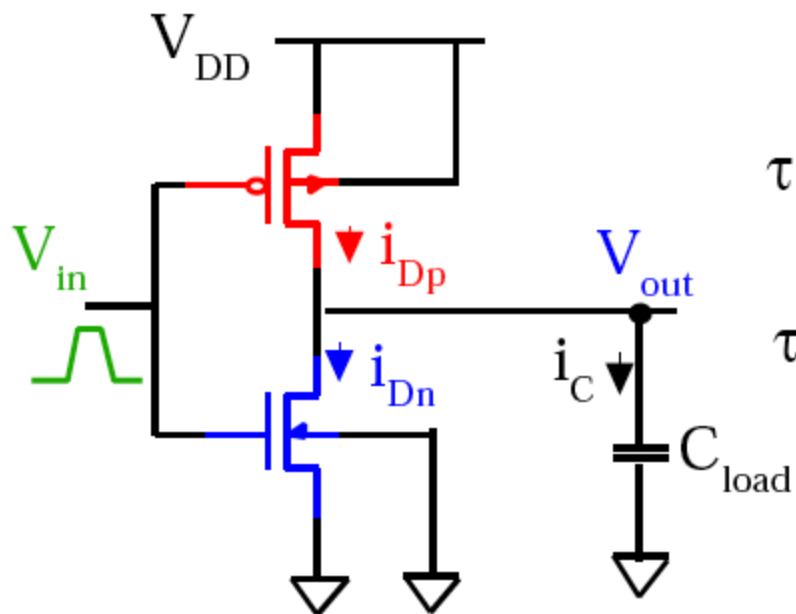
CMOS INVERTER DELAY DESIGN FORMULAS

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

where $k_n = \mu_n C_{ox}\frac{W_n}{L_n}$

$$\frac{W_n}{L_n} = \frac{C_{load}}{\tau_{PHL}\mu_n C_{ox}(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

where $k_p = \mu_p C_{ox}\frac{W_p}{L_p}$

$$\frac{W_p}{L_p} = \frac{C_{load}}{\tau_{PLH}\mu_p C_{ox}(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

EXAMPLE 6.3

Design a CMOS inverter by determining the W_n and W_p of the nMOS and PMOS transistors to meet the following specs:

> -> V_{th} = 2 V for V_{DD} = 5 V
> -> Delay time of 2 ns for a V_{out} transition from 4 V to 1 V, with C_{load} = 1.0 pF.

The process and device parameters are specified as follows:

> $k_n' = \mu_n C_{ox}$ = 30 $\mu A/V^2$,
> $k_p' = \mu_p C_{ox}$ = 10 $\mu A/V^2$
> $L_n = L_p$ = 1.0 μm
> V_{T0n} = 1.0 V
> V_{T0p} = -1.5 V
> W_{min} = 2 μm (limited by design rules)

STEP #1: Satisfy the Delay Constraint: τ_{PHL} from 4 V to 1 V

HL => PULL-DOWN => τ_{PHL} determined by nMOS driver

NOTE $V_{in} = V_{OH}$ and $1 \le V_{out} \le 4$ V => nMOS LIN

$$C_{load} \frac{dV_{out}}{dt} = -\frac{\mu_n C_{ox}}{2} \frac{W_n}{L_n} \left[2(V_{OH} - V_{T0\,n}) V_{out} - V_{out}^2 \right]$$

$$\tau_{delay} = 2.0 \times 10^{-9}\,s = -2\,C_{load} \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n}} \int_{V_{out}=4}^{V_{out}=1} \frac{dV_{out}}{\left[2(V_{OH} - V_{T0\,n}) V_{out} - V_{out}^2 \right]}$$

$$= -2\,C_{load} \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n}} \frac{1}{2(V_{OH} - V_{T0\,n})} \ln\left| \frac{V_{out}}{2(V_{OH} - V_{T0\,n}) - V_{out}} \right|_{V_{out}=4}^{V_{out}=1}$$

$$= \frac{-C_{load}}{\mu_n C_{ox} \frac{W_n}{L_n}(V_{DD} - V_{T0n})} \left\{ \ln\left[\frac{1V}{2(5-1)V - 1V} \right] - \ln\left[\frac{4V}{2(5-1)V - 4V} \right] \right\}$$

$$2.0 \times 10^{-9}\,s = \frac{-1 \times 10^{-12}\,F}{\left(30 \times 10^{-6}\,A/V^2\right) \frac{W_n}{L_n}(5-1)V} \left\{ \ln\left[\frac{1}{7} \right] - \ln\left[\frac{4}{4} \right] \right\}$$

$$\frac{W_n}{L_n} = \frac{1 \times 10^{-12}\,F}{(2.0 \times 10^{-9}\,s)(30 \times 10^{-6}\,A/V^2)(4)} \ln(7) = \frac{1}{(2.0)(0.03)(4)} \ln(7) = 8.108$$

$$\frac{W_n}{L_n} = 8.108, \ L_n = 1\mu m \quad \Rightarrow \quad W_n = 8.108 \ (1 \ \mu m) = 8.1 \ \mu m$$

From τ_{delay} spec.

STEP #2: Satisfy the V_{th} constraint, where:

$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} = \frac{1.0\,V + \sqrt{\frac{1}{k_R}}(5 + (-1.5))\,V}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

$$= \frac{1.0\,V + \sqrt{\frac{1}{k_R}}(3.5)\,V}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} = 2\,V \quad \Rightarrow \quad k_R = (1.5)^2 = \frac{9}{4}$$

$$k_R = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{30\,W_n}{10\,W_p} = 3\frac{W_n}{W_p} = \frac{9}{4} \quad \Rightarrow \quad W_p = \frac{4}{9}(3)W_n$$

with $L_p = 1 \ \mu m$ $\qquad W_p = \frac{4}{9}(3)8.1\mu\,m = 10.8\mu\,m$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

$$k_n = \mu_n C_{ox} \frac{W_n}{L_n} \qquad k_p = \mu_p C_{ox} \frac{W_p}{L_p}$$

If C_{load} = independent of L_n, W_n and L_p, W_p

$$\tau_{PHL} = \frac{C_{load} L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{1}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right] = \boxed{\frac{k_{PHL}}{W_n}}$$

$$\tau_{PLH} = \frac{C_{load} L_p}{\mu_n C_{ox}(V_{DD} - |V_{T0p}|)}\left(\frac{1}{W_p}\right)\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right] = \boxed{\frac{k_{PLH}}{W_p}}$$

Also

$$\boxed{\tau_{fall} = \frac{k_{fall}}{W_n}} \qquad \boxed{\tau_{rise} = \frac{k_{rise}}{W_p}}$$

Cload $i \approx i$ Cdbn + Cdbp + Cint + Cgb

For C_{load} = constant $\quad \tau_{PHL} = \dfrac{k_{PHL}}{W_n} \qquad \lim\limits_{W_n \to \infty} \tau_{PHL} = \lim\limits_{W_n \to \infty} \dfrac{k_{PHL}}{W_n} \to 0s$

$$\tau_{PLH} = \dfrac{k_{PLH}}{W_p} \qquad \lim\limits_{W_p \to \infty} \tau_{PLH} = \lim\limits_{W_p \to \infty} \dfrac{k_{PLH}}{W_p} \to 0s$$

Only when C_{load} is dominated by C_{int} is C_{load} a constant design parameter that is independent of the device dimensions.

In practice, to minimize area, L_n, L_p are set to the minimum dimension , i.e. $L_n = L_p = L_{min}$.
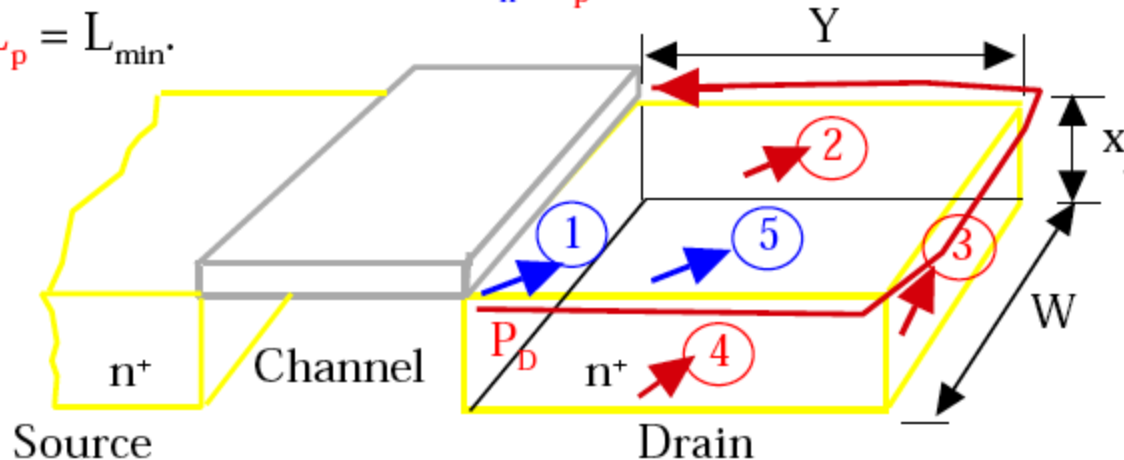
Cload $i \approx i$ Cdbn(Wn) + Cdbp(Wp) + Cint + Cgb

Y

x_j

② ① ⑤ ③

P_b

④

W

n⁺ Channel n⁺

Source Drain

due to gate capacitance of next stage

$$C_{load} \approx \underbrace{C_{dbn}(W_n) + C_{dbp}(W_p)}_{intrinsic} + \underbrace{C_{int} + \boxed{C_{gb}}}_{extrinsic}$$
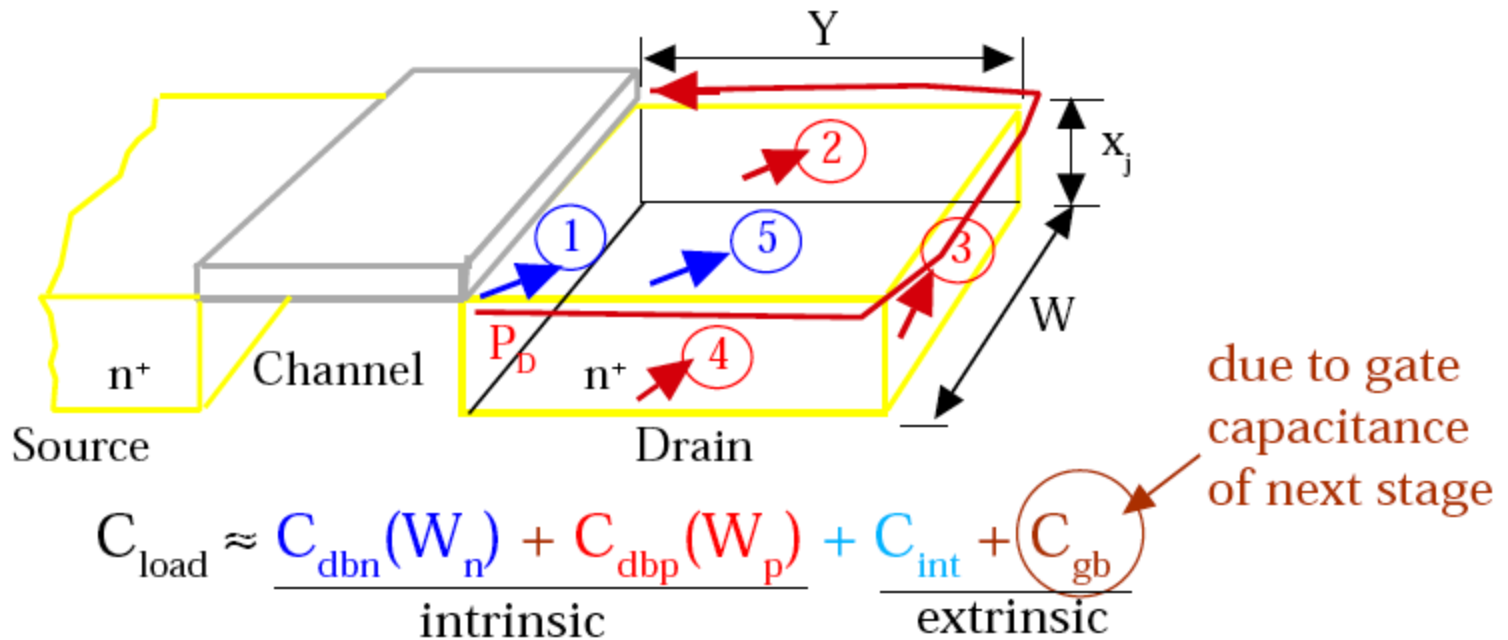
where

$$C_{dbn}(W_n) = W_n(Y + x_j)C_{j0n}K_{eqn} + (W_n + 2Y)\, C_{jswn}K_{eqn}$$

$$C_{dbp}(W_p) = W_p(Y + x_j)C_{j0p}K_{eqp} + (W_p + 2Y)\, C_{jswp}K_{eqp}$$

$$C_{load} = \alpha_n W_n + \alpha_p W_p + \alpha_0$$

$$\alpha_0 = 2Y(C_{jswn}K_{eqn} + C_{jswp}K_{eqp}) + C_{int} + C_{gb}$$

$$\alpha_n = K_{eqn}\left((Y + x_j)C_{j0n} + C_{jswn}\right)$$

$$\alpha_p = K_{eqp}\left((Y + x_j)C_{j0p} + C_{jswp}\right)$$

$$\tau_{PHL} = \frac{C_{load}L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{1}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}L_p}{\mu_n C_{ox}\left(V_{DD} - |V_{T0p}|\right)}\left(\frac{1}{W_p}\right)\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T0p}|\right)}{V_{DD}} - 1\right)\right]$$

Let $C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$

$$\frac{C_{load}}{W_n}$$

$$\frac{C_{load}}{W_p}$$

$$\tau_{PHL} = \Gamma_n\left(\frac{\alpha_0 + \left(\alpha_n + R\alpha_p\right)W_n}{W_n}\right) \qquad \tau_{PLH} = \Gamma_p\left(\frac{\alpha_0 + \left(\frac{\alpha_n}{R} + \alpha_p\right)W_p}{W_p}\right)$$

where $\quad R = \dfrac{W_p}{W_n}$ (set to static parameters, V_{th} in CMOS)

$$\Gamma_n = \left(\frac{L_n}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\Gamma_p = \left(\frac{L_p}{\mu_p C_{ox}\left(V_{DD} - |V_{T0p}|\right)}\right)\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T0p}|\right)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \Gamma_n \left(\frac{\alpha_0 + (\alpha_n + R\alpha_p)W_n}{W_n} \right) \qquad \tau_{PLH} = \Gamma_p \left(\frac{\alpha_0 + \left(\frac{\alpha_n}{R} + \alpha_p \right)W_p}{W_p} \right)$$

Hence, increasing W_p and W_n will have diminishing influence on τ_{PHL} and τ_{PLH} as they become large, i.e.

$$\tau_{PHL}^{Limit} = \lim_{W_n \to \infty} \tau_{PHL} = \Gamma_n (\alpha_n + R\alpha_p)$$

$$\tau_{PLH}^{Limit} = \lim_{W_p \to \infty} \tau_{PHL} = \Gamma_p \left(\frac{\alpha_n}{R} + \alpha_p \right)$$

absolute minimum delays

NOTE:

1. τ_{PHL}^{Limit}, τ_{PLH}^{Limit} are independent of $\alpha_0 = f(C_{int}, C_{gb})$.

2. Achievement of ABSOLUTE MINIUMUM DELAYS comes with maximum cost, i.e.

   DIE AREA -> Maximized
   POWER DISIPATION -> Maximized

CMOS RING OSCILLATOR
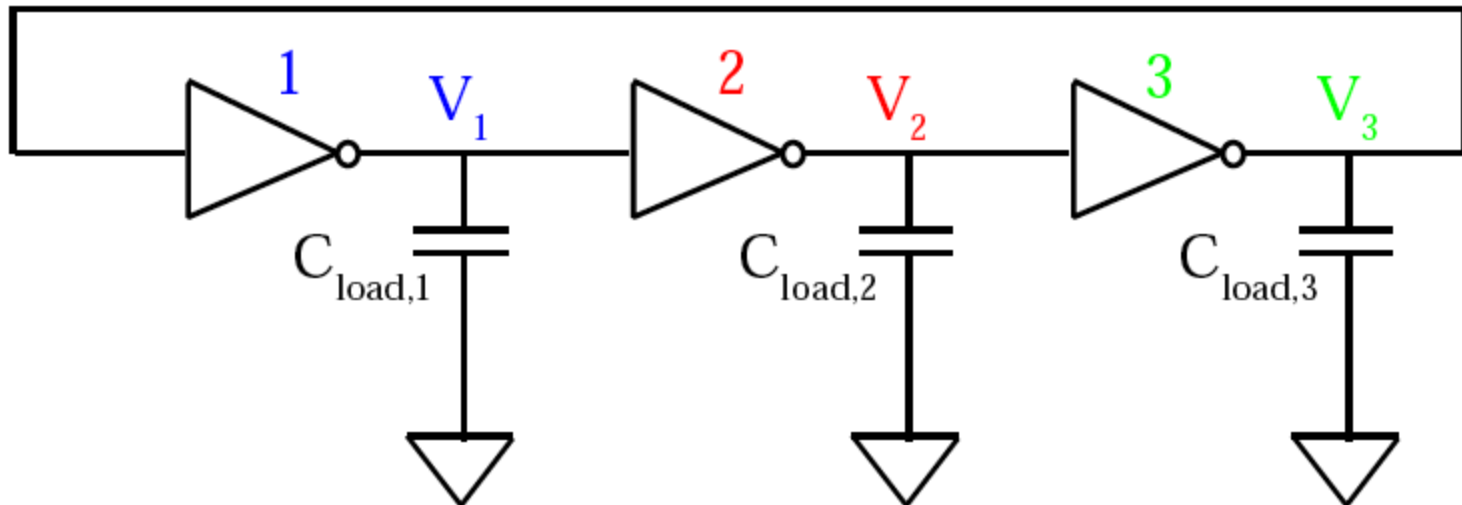
$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3
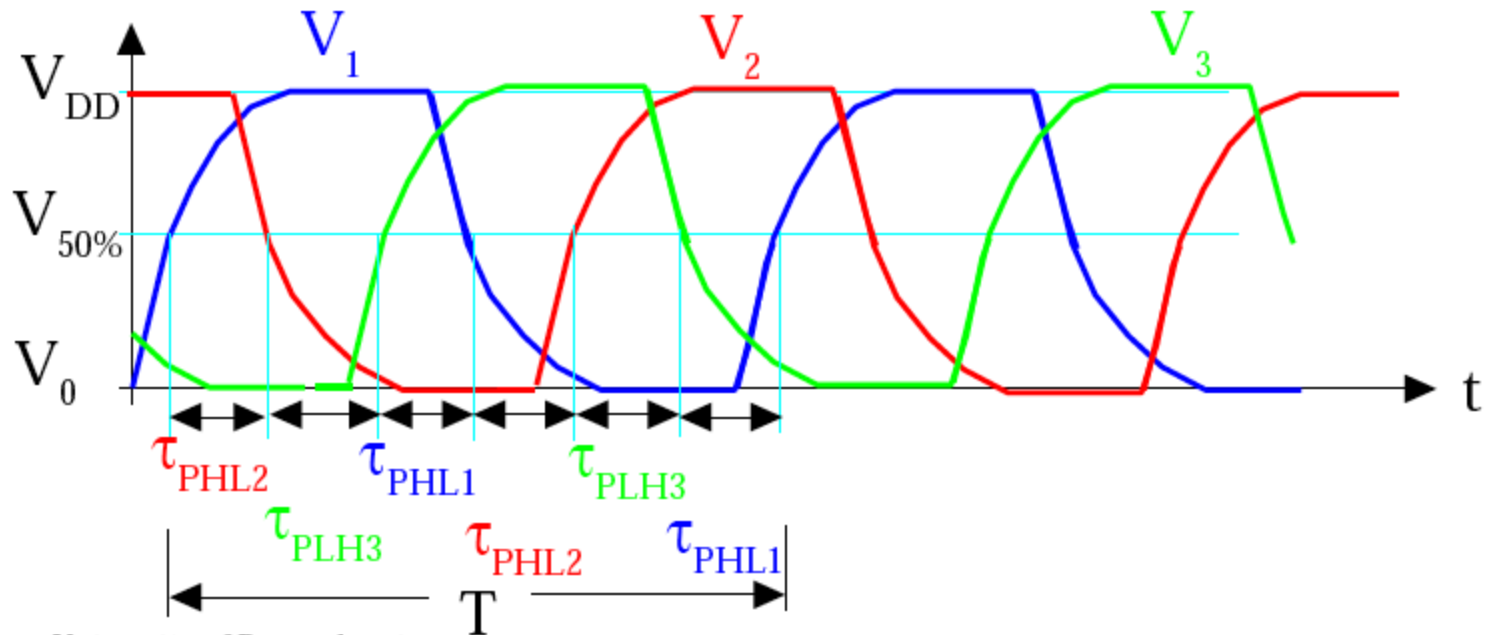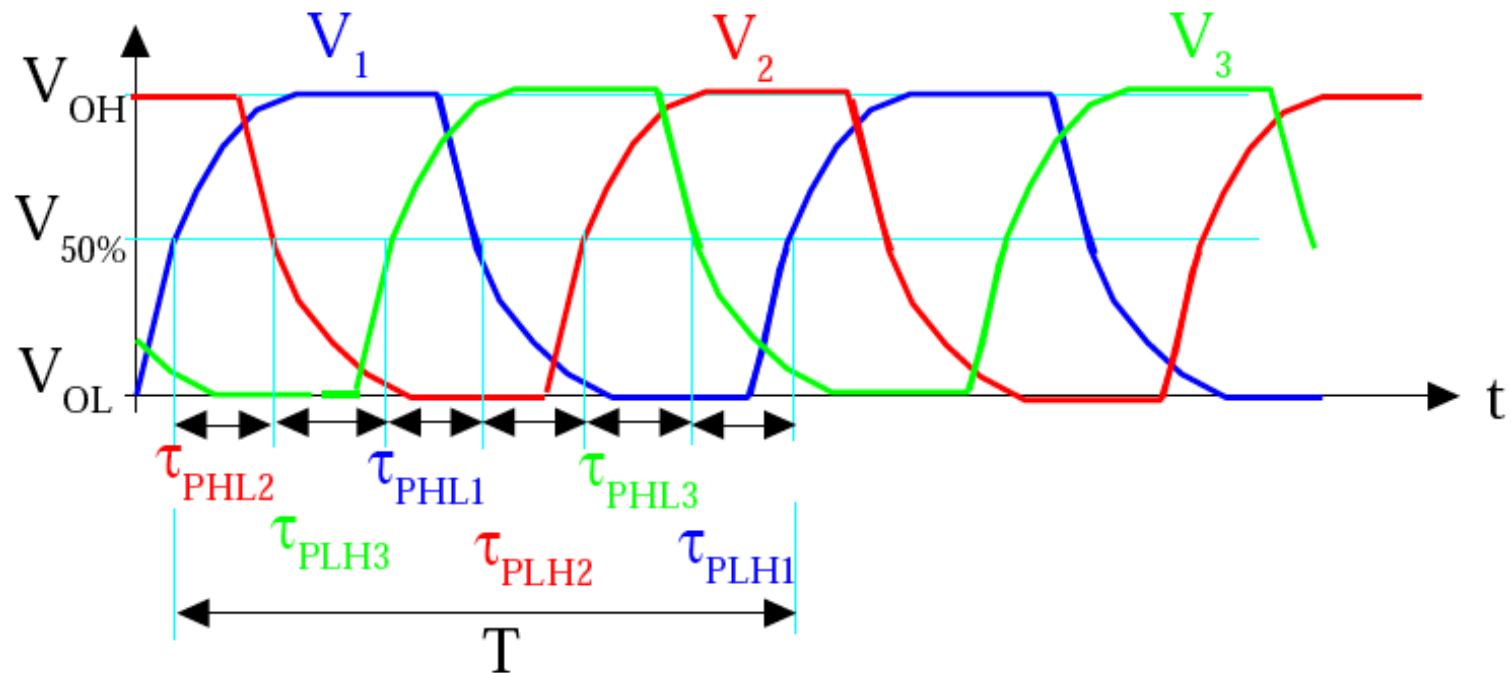
$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3

$T = \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH1} = 6\tau_P$

where $2\tau_p = \tau_{PHLi} + \tau_{PLHi}$ for i = 1, 2, 3

$f = \dfrac{1}{T} = \dfrac{1}{3 \times 2\tau_p} = \dfrac{1}{6\tau_p}$ Oscillation FREQ for 3 INVERTERS

For n INVERTERS:
where n = odd

$$f = \frac{1}{T} = \frac{1}{2n\tau_p} \quad \text{or} \quad \tau_P = \frac{1}{2nf}$$

Interconnection Capacitance
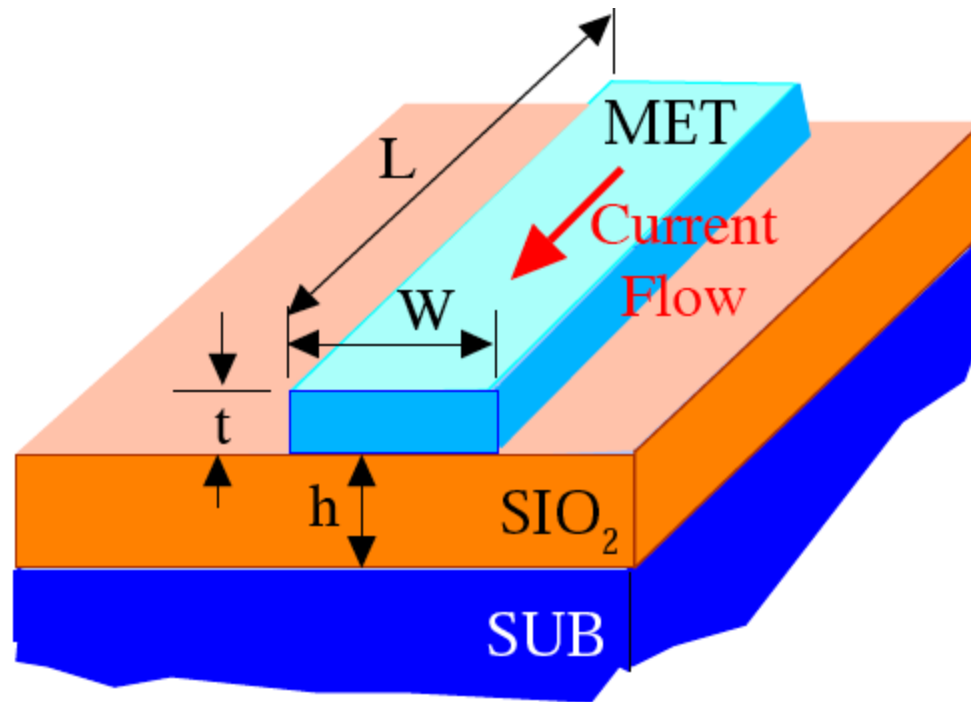
PARASITIC RESISTANCE:

$$R_{metal} = \rho \frac{L}{Wt} = R_{sheet} \frac{L}{W}$$

Interconnection Delays in Sub-micron process
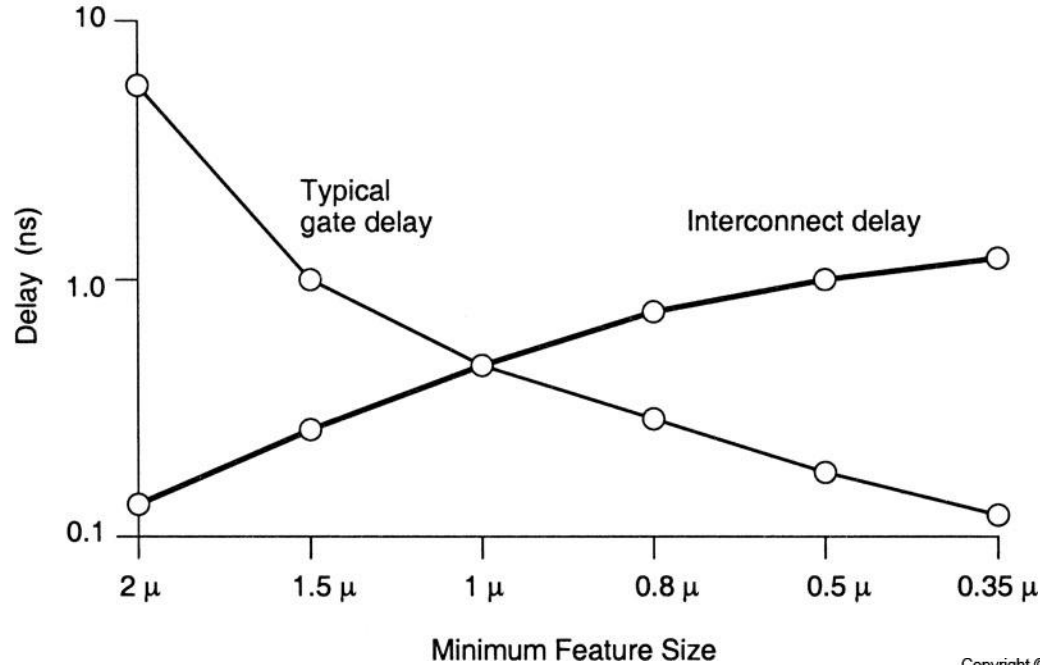
fringing fields W t h
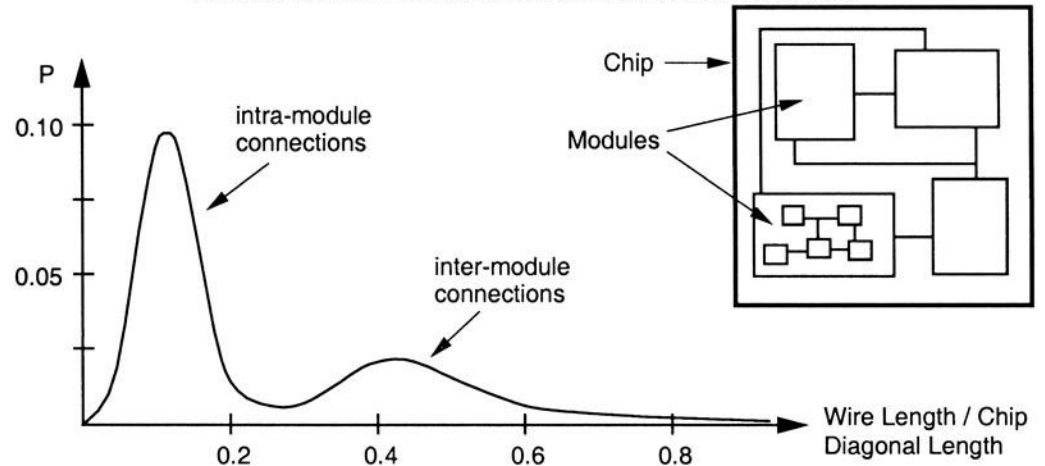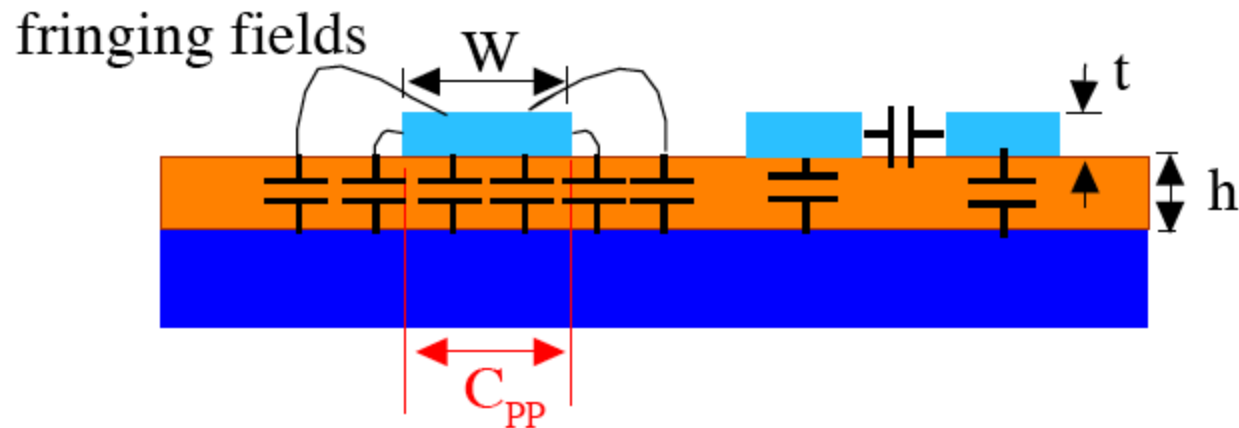
$FF = C_{total}/C_{PP}$ -> FRINGING-FIELD FACTOR

FF -> INC as t/h -> INC, W/h <- DEC, and W/L -> INC

(SEE PLOT FF in FIG. 6.18 of TEXT)

$$C_{total} = \varepsilon \left[\frac{W - \frac{t}{2}}{h} + \frac{2\pi}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} \right] \text{pF/}\mu\text{m L} \quad \text{for } W \geq t/2$$

$$C_{total} = \varepsilon \left[\frac{W}{h} + \frac{\pi\left(1 - 0.0543\frac{t}{2h}\right)}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} + 1.47 \right] \text{pF/}\mu\text{m L} \quad \text{for } W < t/2$$
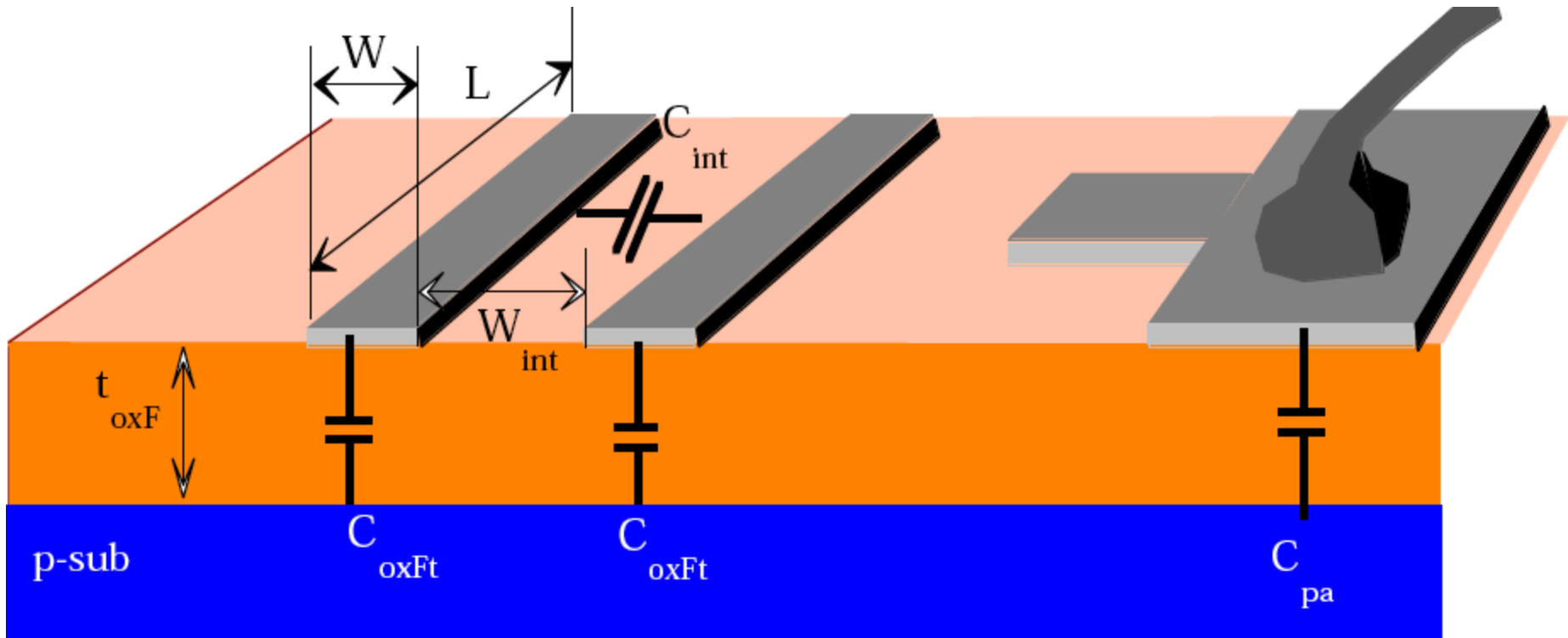
Double-metal double-poly n-well CMOS process

C_{mm}	$C_{\text{metal-to-metal}}$	$=$	$2.5\ \text{nF/cm}^2$
C_{oxm}	$C_{\text{metal-to-substrate}}$	$=$	$5.2\ \text{nF/cm}^2$
C_{oxp}	$C_{\text{poly-to-substrate}}$	$=$	$6.5\ \text{nF/cm}^2$
C_{mp}	$C_{\text{metal-to-poly}}$	$=$	$12.0\ \text{nF/cm}^2$

Diagram labels: A, B, C, D, E, F, G, passivation, m2, m1, poly, field ox, substrate
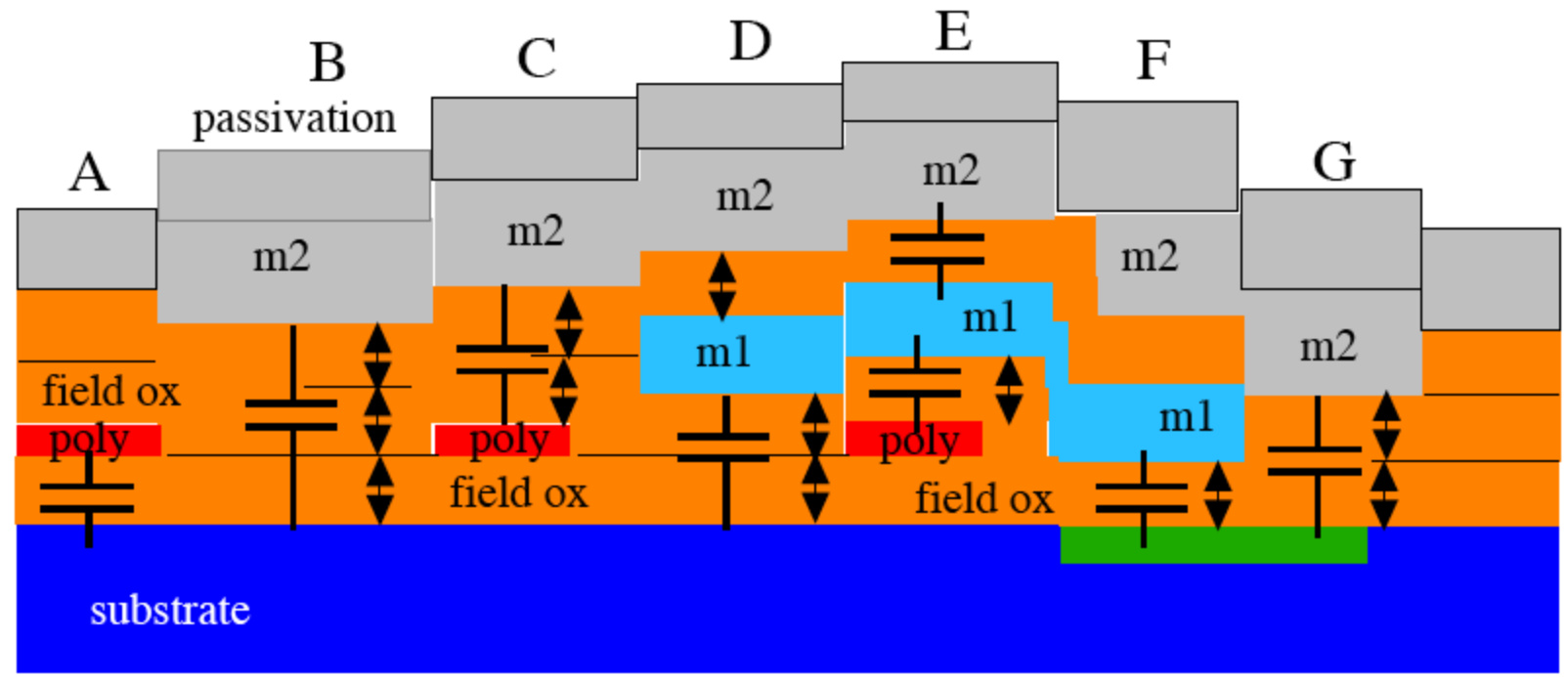
	Layer	Cap	Ox Thickness	Typ Value
A	Poly-substrate	C_p	3000 Å	50 aF/μm^2
B	Metal2-sub	C_{m2}	9000 Å	20 aF/μm^2
C	Poly-metal2	C_{m2p}	6000 Å	30 aF/μm^2
D	Metal1-sub	C_{m1}	6000 Å	30 aF/μm^2
E	Metal1-poly	C_{m1p}	3000 Å	60 aF/μm^2
E	Metal1-metal2	C_{m2m1}	6000 Å	50 aF/μm^2
F	Metal1-diffusion	C_{m1d}	3000 Å	60 aF/μm^2
G	Metal2-diffusion	Passivation	6000 Å	30 aF/μm^2

1 μm CMOS
Capacitances
$$t_{ox} = 200 \text{Å}$$
$$C_g = 1800 \text{ aF/}\mu\text{m}^2$$
aF = 10^{-18} F

AMI 0.5 micron process

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		463	-248	uA/um
Vth		0.67	-0.91	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.8	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.49	0.57	V^0.5
K' (Uo*Cox/2)		57.8	-19.1	uA/V^2
Low-field Mobility		475.38	157.09	cm^2/V*s

AMI 0.5 micron process

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	426	724	85		30	15	9	37	aF/um^2
Area (N+active)			2434		34	17	12		aF/um^2
Area (P+active)			2351						aF/um^2
Area (poly)				899	56	16	9		aF/um^2
Area (poly2)					46				aF/um^2
Area (metal1)						33	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	361	241			71	49	33		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						46	34		aF/um
Fringe (metal2)							54		aF/um
Overlap (N+active)			292						aF/um
Overlap (P+active)			387						aF/um

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	84.4	109.2	22.9	1102	41.9	0.09	0.09	ohms/sq
Contact Resistance	60.9	150.6	15.8		26.8		0.81	ohms
Gate Oxide Thickness	142							angstrom

AMI 0.5 micron process

```
CIRCUIT PARAMETERS                              UNITS
 Inverters                     K
  Vinv                        1.0      2.04   volts
  Vinv                        1.5      2.29   volts
  Vol (100 uA)                2.0      0.12   volts
  Voh (100 uA)                2.0      4.86   volts
  Vinv                        2.0      2.47   volts
  Gain                        2.0    -18.26
 Ring Oscillator Freq.
  DIV256 (31-stg,5.0V)                98.75   MHz
  D256_WIDE (31-stg,5.0V)            153.47   MHz
 Ring Oscillator Power
  DIV256 (31-stg,5.0V)                 0.49   uW/MHz/gate
  D256_WIDE (31-stg,5.0V)              1.00   uW/MHz/gate
```

ROUTE-LENGTH DESIGN GUIDE

To ignore the RC delay of interconnect, $\tau_W \ll \tau_{Pgate}$ (intrinsic)

$\tau_W \approx 0.69 \dfrac{rcL_W^2}{2}$ emperical formula

for simple lumped RC ckt

L_W = length of route
$r = \Omega$ per unit lenght
$c = F$ per unit length (W at minimum dimension)

$$\tau_W \approx 0.69 \frac{rcL_W^2}{2} \ll \tau_{Pgate} = 0.01\tau_{Pgate} \Rightarrow L_{Wlim} = \frac{1}{10}\sqrt{\frac{2\tau_{Pgate}}{0.69rc}}$$

EXAMPLE: Consider a minimum width metal1 route to a node with an associated gate delay of 200 ps.

$$L_{Wlim} = \frac{1}{10}\sqrt{\frac{\tau_{Pgate}}{0.69rc}} = \frac{1}{10}\sqrt{\frac{2 \times \left(0.2 \times 10^{-9}\,s\right)}{\left(\dfrac{0.05\,\Omega}{\lambda}\right)\left(\dfrac{30 \times 10^{-18}\,F}{\lambda}\right)}}$$
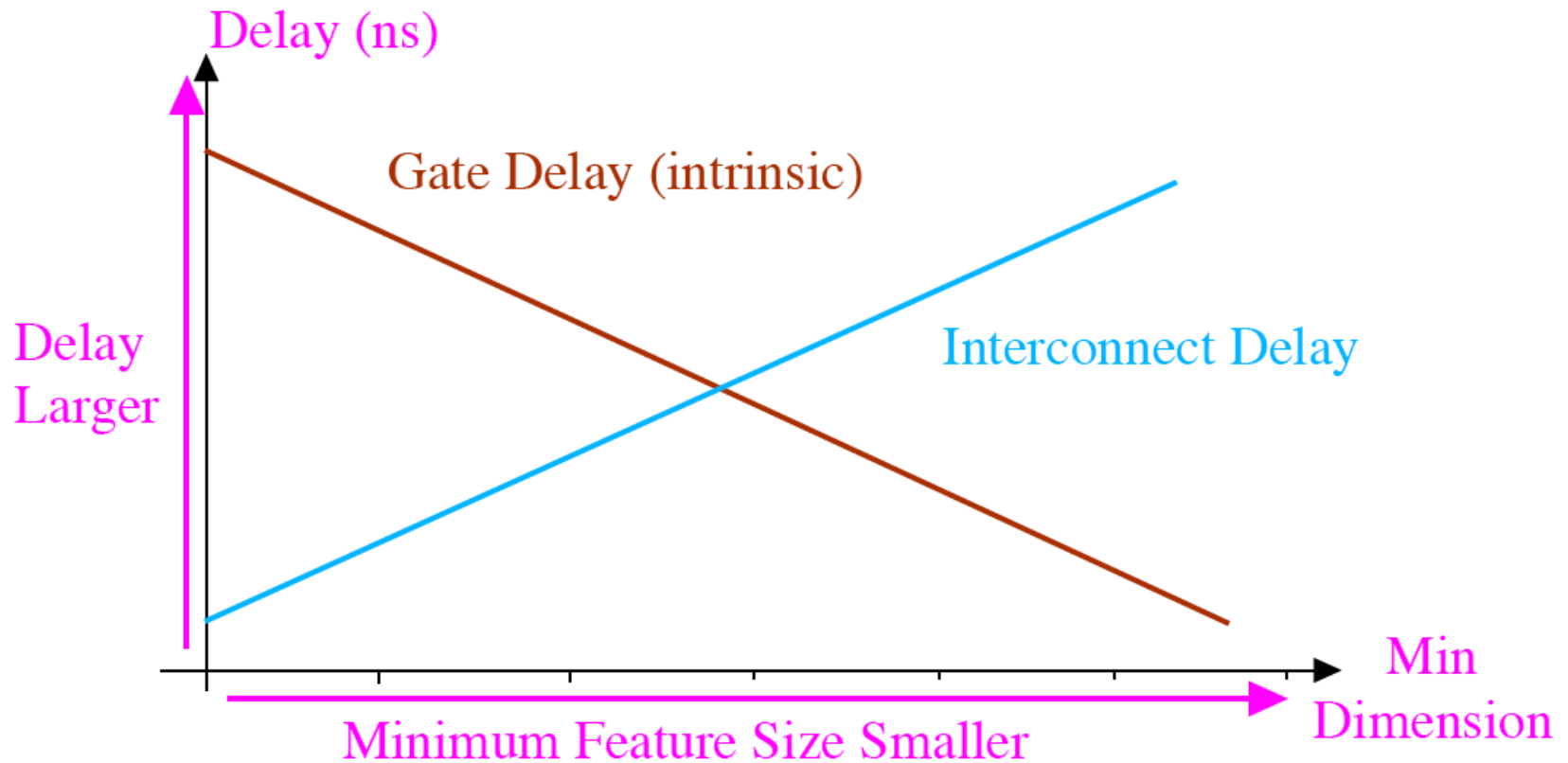
$= 1633\,\lambda$

λ = design rule parameter

GUIDELINES FOR IGNORING RC DELAYS in a wire route

Layer	Max Length (L_{Wlim})
metal3	1000 λ
metal2	800 λ
metal1	500 λ
silicide	60 λ
poly	20 λ
diffusion	6 λ

DELAY TREND IN VLSI WITH DIMINISHING FEATURE SIZE

$$\tau_W \approx 0.69 \frac{rcL_W^2}{2} \ll \tau_{Pgate} = 0.01\tau_{Pgate} \Rightarrow L_{Wlim} = \frac{1}{10}\sqrt{\frac{2\tau_{Pgate}}{0.69rc}}$$

BECOMING MORE DIFFICULT TO ACHIEVE

Examples of Propagation Delay

Product	CMOS technology generation	Clock frequency, f	Fan-out=4 inverter delay
Pentium II	0.25 μm	600 MHz	~100 ps
Pentium III	0.18 μm	1.8 GHz	~40 ps
Pentium IV	0.13 μm	3.2 GHz	~20 ps

Typical clock periods:
• high-performance μP: ~15 FO4 delays
• PlayStation 2: 60 FO4 delays

POWER DISSIPATION

P_s = Static power dissipation due to leakage current or other current drawn continuously from the power supply.

P_d = dynamic power dissipation due to charging and discharging load capacitances (v_{in} assumed to be square-like)

P_{sc} = short circuit power dissipation due to charging and discharging load capacitances during the finite rise and fall times of v_{in}.
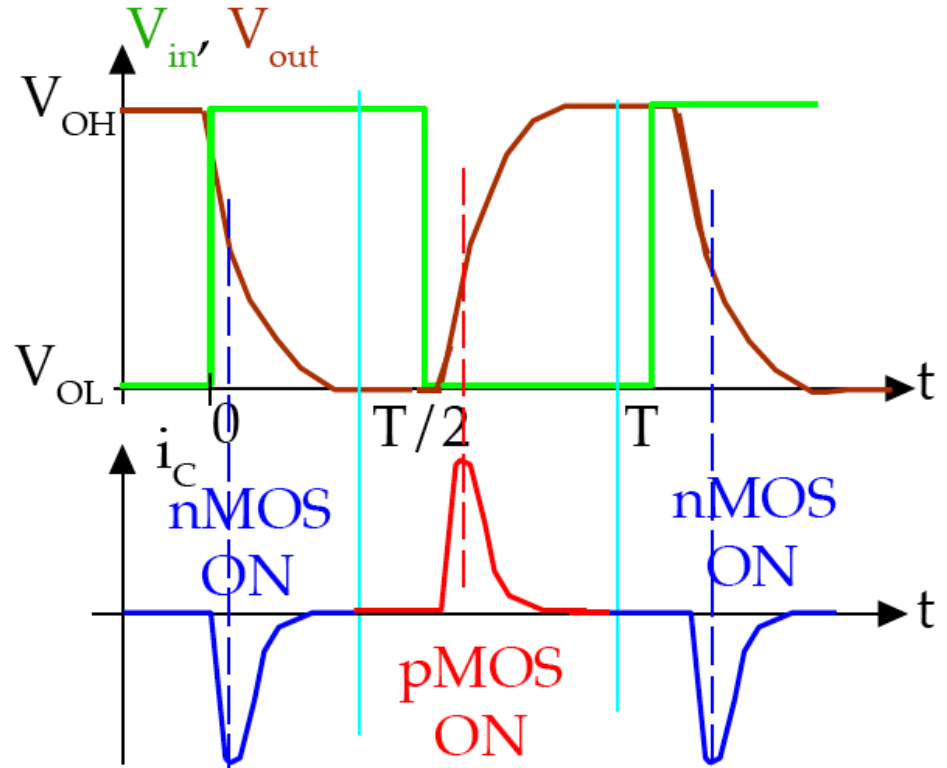
DYNAMIC POWER DISSAPATION

$$i_C = i_{Dp} - i_{Dn}$$
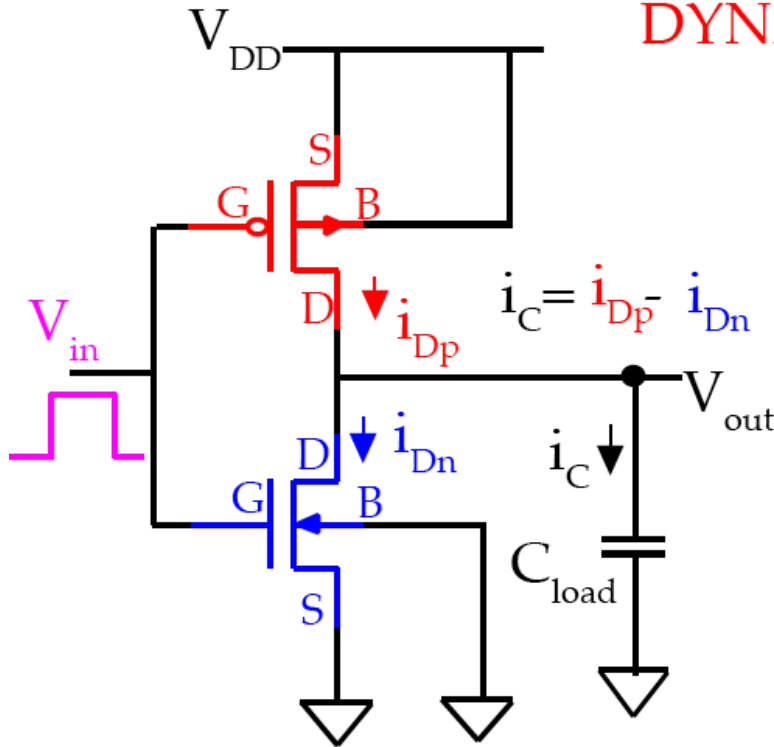
$$P_{avg} = \frac{1}{T} \int_0^T v(t)i(t)dt$$

$$P_{avg} = \frac{1}{T} \int_0^{T/2} V_{out}(t)i_{Dn}(t)dt + \frac{1}{T} \int_{T/2}^T \left(V_{DD} - V_{out}(t)\right)i_{Dp}(t)dt$$

where $\quad i_{Dn}(t) = -C_{load}\dfrac{dV_{out}}{dt} \qquad i_{Dp}(t) = C_{load}\dfrac{dV_{out}}{dt}$

$$P_{avg} = \frac{1}{T} \int_0^{T/2} V_{out}(t)\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \frac{1}{T} \int_{T/2}^{T} \left(V_{DD} - V_{out}(t)\right)\left(C_{load}\frac{dV_{out}}{dt}\right)dt$$
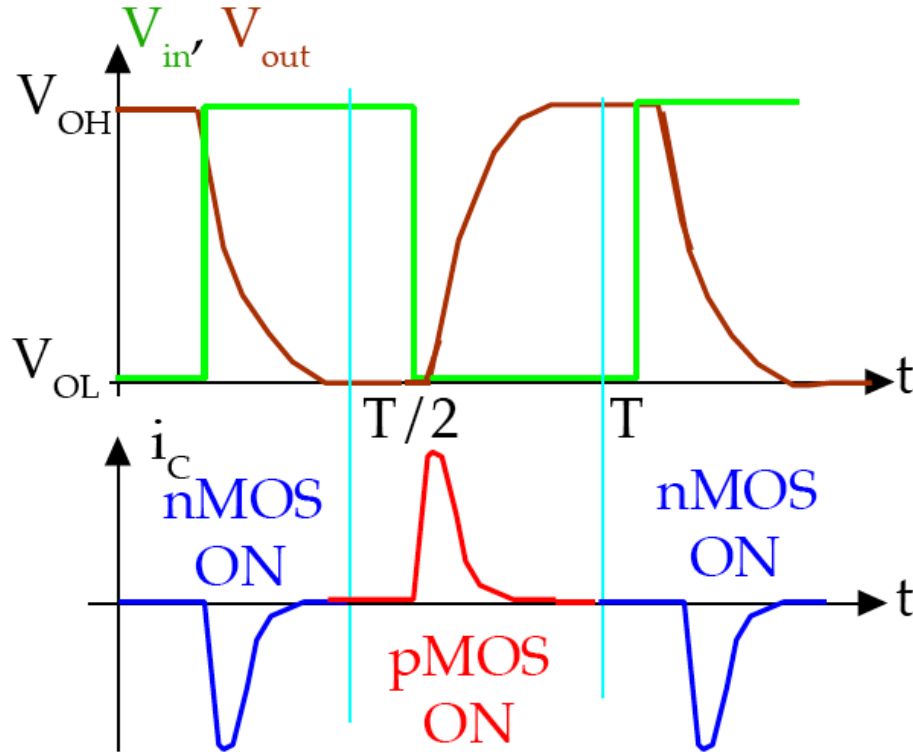
$$P_{avg} = \frac{1}{T} \int_{V_{DD}}^{0} -C_{load}V_{out}(t)dV_{out} + \frac{1}{T} \int_0^{V_{DD}} C_{load}\left(V_{DD} - V_{out}(t)\right)dV_{out}$$

$$= \frac{1}{T}\left[-C_{load}\frac{V_{out}^2}{2}\Big|_{V_{out}=V_{DD}}^{V_{out}=0} + C_{load}\left(V_{DD}V_{out} - \frac{V_{out}^2}{2}\right)\Big|_{V_{out}=0}^{V_{out}=V_{DD}}\right]$$

$$P_{avg} = \frac{1}{T}\left[-C_{load} \frac{V_{out}^2}{2}\bigg|_{\substack{V_{out}=0 \\ V_{out}=V_{DD}}} + C_{load}\left(V_{DD}V_{out} - \frac{V_{out}^2}{2}\right)\bigg|_{\substack{V_{out}=V_{DD} \\ V_{out}=0}} \right]$$

$$= \frac{1}{T}C_{load}V_{DD}^2$$
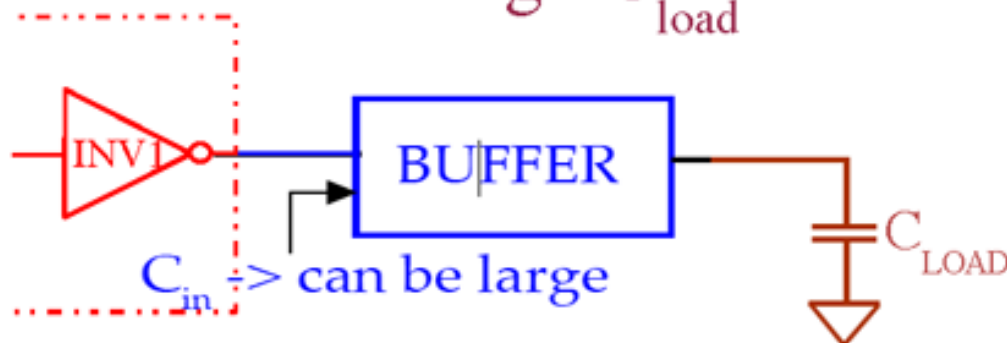
$$P_{avg} = C_{load}V_{DD}^2 f$$

APPLIES TO GENERAL CMOS LOGIC CIRCUITS
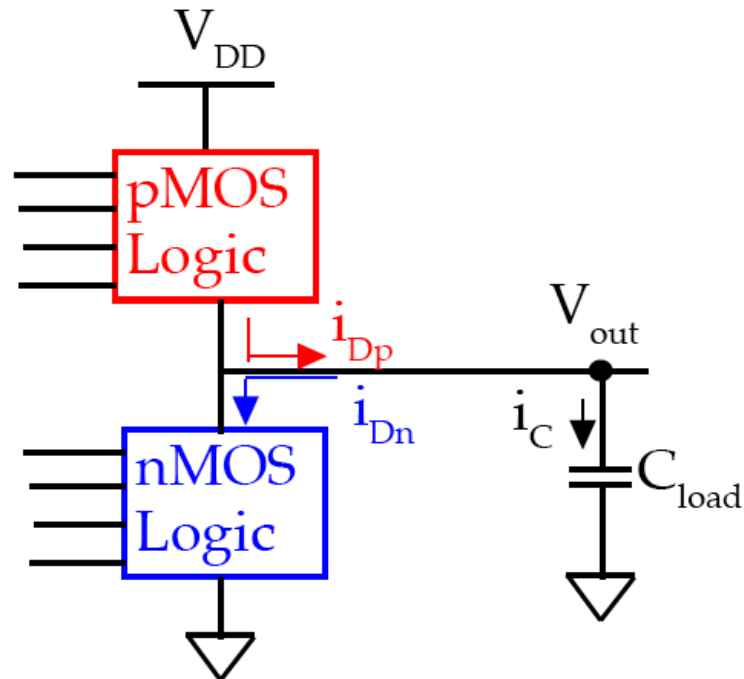
Cascade of N Inverters or Super-Buffer to Drive Large C_{load}

standard
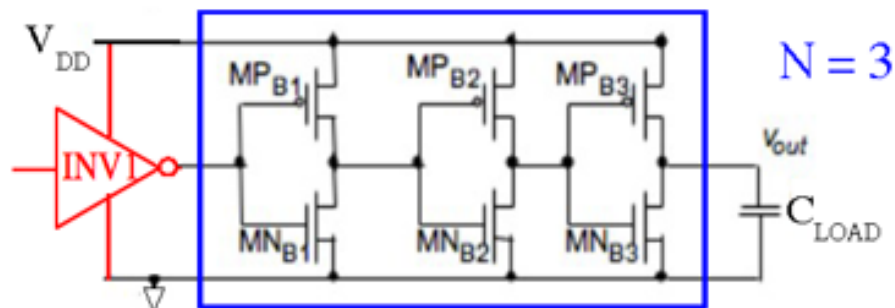CMOS
logic on
die

INV

C_{in} => can be large

BUFFER

C_{LOAD}

V_{DD}

INV

MP_B

v_{out}

MN_B

C_{LOAD}

PROBLEM: A minimum sized inverter drives a large load C_{LOAD}, leading to excessive delay, even with a large buffer (large W/L).
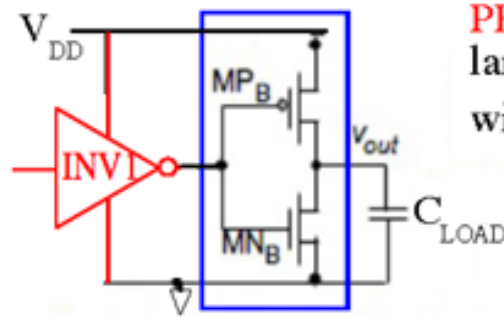
SOLUTION: Insert N inverter stages in cascade with increasing W/L between INV1 and load C_{LOAD}. The total delay through N stages will be less than the delay through a singe stage driving C_{LOAD}.

V_{DD}

INV

MP_{B1} MP_{B2} MP_{B3}

v_{out}

MN_{B1} MN_{B2} MN_{B3}

C_{LOAD}

$N = 3$

Cascade of N Inverters or Super-Buffer to Drive Large C_{load} cont.

Super Buffer - chain of scaled cascaded inverters

INV1

Stage-0 Stage-1 Stage-2 Stage-3

V_{o0} V_{o1} V_{o2} V_{o3}

C_g C_d aC_g aC_d a^2C_g a^2C_d a^3C_g a^3C_d C_{LOAD}

C_{load0}

N = 3
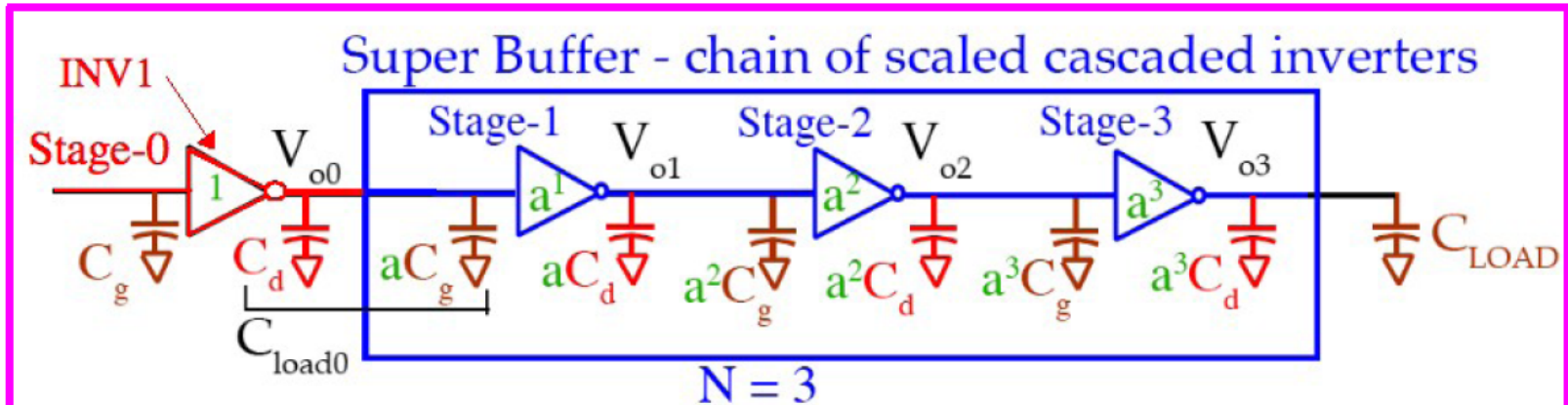
CONSIDER N stages, where N is a variable, and $a^{N+1} = C_{LOAD}/C_g$

$W_{ni} = a^i W_{n0}$ and $W_{pi} = a^i W_{p0}$ for $i = 0, 1, ..., N$

$C_{loadi} = a^i(C_d + aC_g)$ for $i = 0, 1, ..., N$ and $a^{N+1} = C_{LOAD}/C_g$

NOTE: ALL inverters have the same delay

$$t_d = \frac{\tau_0}{a^i} \frac{a^i(C_d + aC_g)}{C_d + C_g} = \tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

where $i = 1, ..., N$; τ_0 is the gate delay for INV1 in a ring oscillator with load $C_d + C_g$

$$t_{total} = (N+1) \cdot t_d = (N+1) \cdot \tau_0 \cdot \frac{C_d + aC_g}{C_d + C_g}$$

Choose N and a to minimize t_{total}

where $a^{N+1} = C_{LOAD}/C_g$ & $N+1 = \frac{\ln(C_{LOAD}/C_g)}{\ln(a)}$

Cascade of N Inverters or Super-Buffer to Drive Large C_{load} cont.

$$t_{total} = (N+1)\tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

$$N+1 = \frac{\ln(C_{LOAD}/C_g)}{\ln(a)}$$

$$\Rightarrow \quad t_{total} = \frac{\ln(C_{LOAD}/C_g)}{\ln(a)} \tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

$$W_{ni} = a^i W_{n0} \text{ and } W_{pi} = a^i W_{p0}$$

TO MINIMIZE t_{total}:

$$\frac{dt_{total}}{da} = \tau_0 \ln\left(\frac{C_{LOAD}}{C_g}\right)\left[-\frac{1/a}{(\ln(a))^2}\left(\frac{C_d + aC_g}{C_d + C_g}\right) + \frac{1}{\ln(a)}\left(\frac{C_g}{C_d + C_g}\right)\right] = 0$$

$$= 0$$

$$a_{opt}\left[\ln(a_{opt}) - 1\right] = \frac{C_d}{C_g} \qquad a_{opt} \geq e = 2.718$$

For the SPECIAL CASE $C_d = 0 \Rightarrow \ln(a_{opt}) = 1$ or $a_{opt} = e^1 = 2.718$

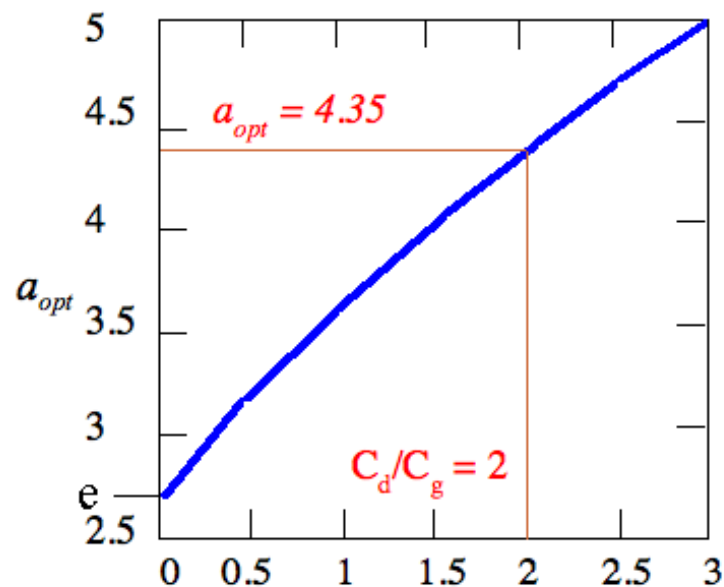Since $C_d > C_g$, $C_d = 0$ is only an academic special case.

EXAMPLE: Design a Buffer using a scaled cascade of inverters to achieve minimum total delay t_{total} when $C_{LOAD} = 100\ C_g$. Consider the case where $C_d = 2C_g$.

$C_d = 2C_g \Rightarrow$ plot a_{opt} as function of C_d/C_g: $\boxed{a_{opt} = 4.35} \Rightarrow \ln(a_{opt}) = 1.47$

Plot using Excel, MathCad, MatLab.

$$N + 1 = \frac{\ln(C_{LOAD}/C_g)}{\ln(a_{opt})}$$

$$\Rightarrow N = \frac{\overset{4.61}{\boxed{\ln(C_{LOAD}/C_g)}}}{1.47} - 1 = 2.13 \rightarrow \boxed{N = 3}$$

$$e^{3.13 \ast 1.47} = 100 \le \frac{C_{LOAD}}{C_g} \le e^{4 \ast 1.47} = 365$$

$$\frac{C_d}{C_g} = a_{opt} \cdot (\ln a_{opt} - 1)$$

$a_{opt} = 4.35$

$C_d/C_g = 2$

i	W_{ni}/W_{n0}	W_{pi}/W_{p0}
1	$(a_{opt})^1 = 4.35$	$(a_{opt})^1 = 4.35$
2	$(a_{opt})^2 = 18.92$	$(a_{opt})^2 = 18.92$
3	$(a_{opt})^3 = 82.31$	$(a_{opt})^3 = 82.31$

3rd stage can be eliminated with little impact.