Alexandria University
Faculty of Engineering
Electrical Engineering Department

CC401: Digital Integrated Circuits
Lab 3: CMOS Combinational Logic Gates

Introduction:

The experiment is to design a 2-input CMOS NAND gate based on the CMOS inverter and study its characteristics. Using the properties of the inverter we are able to create a network of NMOS and PMOS transistors to create logic [Figure 1]. This allows the creation of any of the logic gates, to illustrate we build a NAND gate. This gate is an important one because this is a universal gate, meaning we can create any logic function using only this gate. Its logic function is $\overline{A.B}$, which is what the design must satisfy [Table 1].

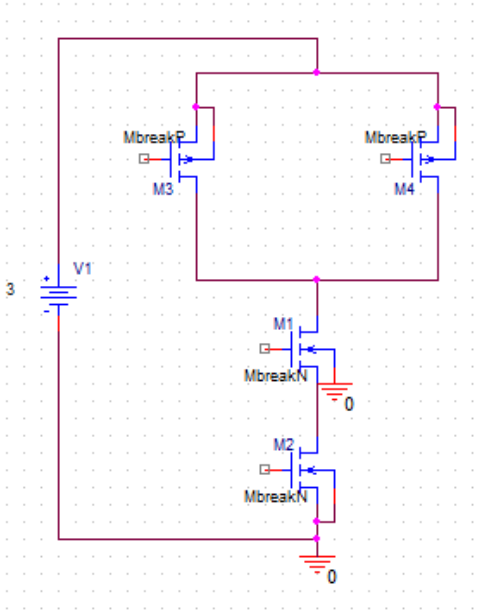

Figure 1

Table 1

A	B	NAND
1	0	1
1	1	1
0	0	1
0	1	0

The experiment will also analyze the "worst case" scenario in which the propagation delay is extended because of the conditions the PMOS and NMOS are interacting.

Procedure:

The NAND gates is composed of a pull up and pull down network, composed of PMOS and NMOS transistors respectively. When designed in the NAND manner the width of the PMOS channel is larger than that of the NMOS, causing the gate to not have a desired VDD/2 threshold. This led to the sizing of the NMOS network to match the PMOS and have an equal voltage drop across the two networks.

The NAND gate accepts two inputs and with their combinations the NAND gate turns on or off the NMOS and PMOS, creating paths to VDD or ground hence creating the logic. Because these are networks that interact with each other, there is cases where the networks in parallel and its components are not all on or off at the same time causing the "worst case" scenario. This is when the path of the current through a network is giving the correct logic, but because of the input combinations not all the transistors are operating, causing smaller channels or longer paths. When such case occurs it is identified as the "worst case" because the propagation delay is increased, which is not desirable. For this design the worst case condition is when one of the PMOS transistors is on and the other off lowering the width of the channel.

The procedure involved

- Design a static 2 input CMOS NAND gate based on the CMOS inverter.
- Then it had to be tested for the logic functionality of the design so it satisfies the NAND gate properties. (We have two inputs use two input pulse waves see figure 1 and the following paragraph will illustrate more).
- Size each gate such that NMOS and PMOS pull strength for both networks match for the "worst case" delay. (See lecture notes).
- Then, simulate the Voltage Transfer Characteristic (VTC) of the design to verify the functionality of the switching. (By connecting all the inputs together, acts as an inverter).
- Finally, draw the layout for the NAND gate using L-Edit and test its functionality using T-spice.
- Repeat the previous steps for NOR gate.

The simulation set up was to design the desired gates; their simulation was first evaluated to analyze the gate's functionality. Figure 2 are the NAND gate simulations when analyzed on ORCAD PSPICE. These verify the proper functionality of the design at the various frequency at which it was tested with accompanying results. Simulate the gate with three frequencies: 0.1, 0.5 and 1 MHz in conjunction with half the test frequency to produce all the logic scenarios, inputs A and B respectively. Figure 3 shows how the results should be.

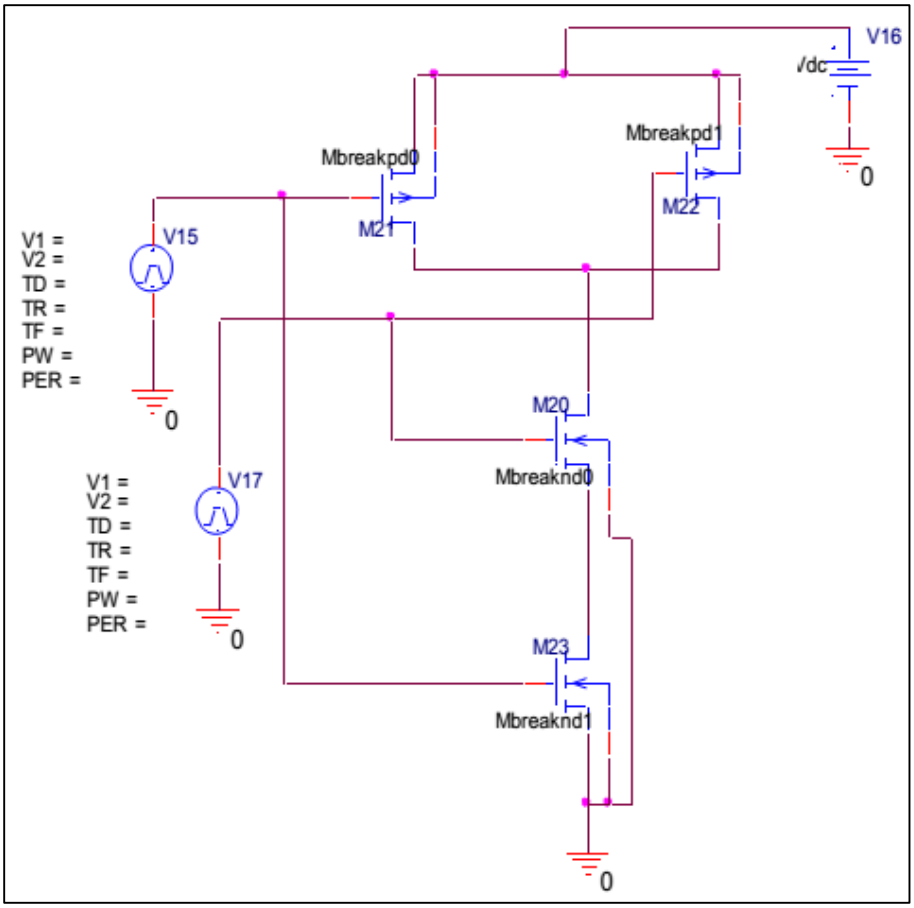

Figure 2

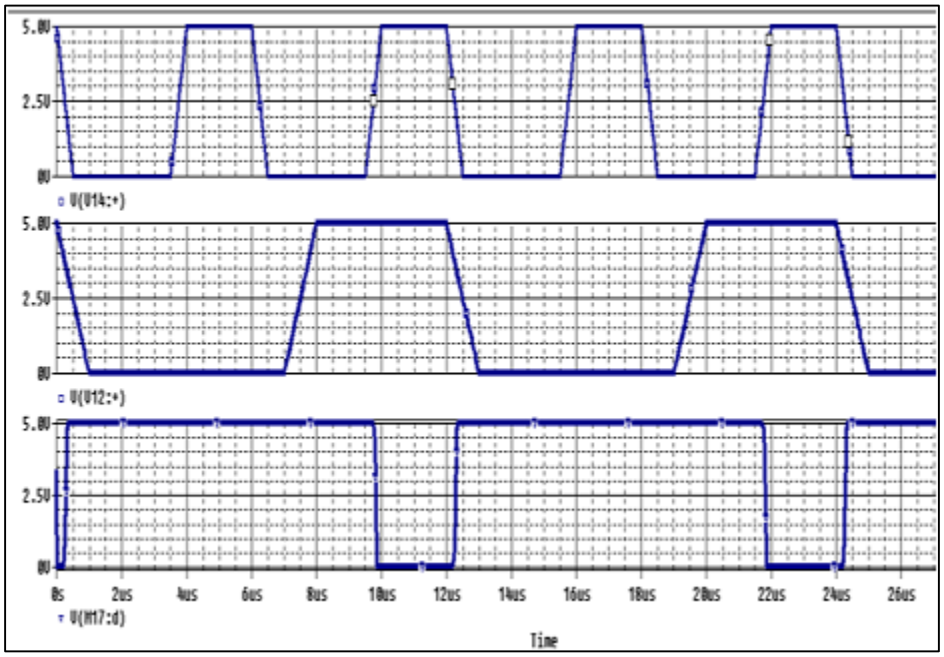

Figure 3

Appendix:

PMOS Model

.model Mbreakp PMOS LEVEL = 3
+ TOX = 200E-10 NSUB = 1E17 GAMMA = 0.6
+ PHI = 0.7 VTO = -0.9 DELTA = 0.1
+ UO = 250 ETA = 0 THETA = 0.1
+ KP = 40E-6 VMAX = 5E4 KAPPA = 1
+ RSH = 0 NFS = 1E12 TPG = -1
+ XJ = 500E-9 LD = 100E-9
12
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
+ CJSW = 300E-12 MJSW = 0.5

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NMOS Model

.model Mbreakn NMOS LEVEL = 3
+ TOX = 200E-10 NSUB = 1E17 GAMMA = 0.5
+ PHI = 0.7 VTO = 0.8 DELTA = 3.0
+ UO = 650 ETA = 3.0E-6 THETA = 0.1
+ KP = 120E-6 VMAX = 1E5 KAPPA = 0.3
+ RSH = 0 NFS = 1E12 TPG = 1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
0
+ CJSW = 300E-12 MJSW = 0.5

Reference:

Christian Gil, Edgar Siles, “CMOS Digital Electronics Laboratory Notes”, California State University, Northridge.