Alexandria University
Faculty of Engineering
Communications and Computers Department
Mid-term Exam, April 2016

جامعة الإسكندرية
كلية الهندسة
قسم هندسة الإتصالات والحاسبات
امتحان نصف الفصل الدراسي الثاني (إبريل ٢٠١٦)

Course Title and Code Number:
Digital Integrated Circuits Design (CC401)
Time Allowed: 1 Hours

اسم المقرر والرقم الكودي له: تصنيع و تصميم
تصميم الدوائر المتكاملة الرقمية (CC401)
الزمن: ساعة واحدة

Answer all questions: **(20 marks)**

Question 1: **(10 marks)**

Consider a CMOS inverter, with the following device parameters:

NMOS $V_{T0n} = 0.6\ V$ $\mu n\ Cox = 50\ \mu A/V^2$
PMOS $V_{T0p} = -0.6\ V$ $\mu p\ Cox = 20\ \mu A/V^2$
and $V_{DD} = 3.3\ V$

a) Determine the (W/L) ratios of the nMOS and pMOS transistors for a symmetric inverter.
b) Plot the VTC of the CMOS inverter and indicate the values of V_{OH}, V_{OL}, V_{th}, V_{IL}, and VIH.
c) Plot the VTC of two cascaded inverters, and calculate the output voltage for an input voltage V_i of 1 V. What is this circuit called?

Question 2: **(10 marks)**

For the symmetric CMOS inverter described in Question 1:

a) Calculate the propagation time τ_{PHL} and τ_{PLH} of the inverter for an output load capacitance of 1.5 pF.
b) Determine the maximum frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0 V to 3.3 V in each cycle. Calculate the dynamic power dissipation at this frequency.
c) How do the inverter switching threshold V_{th} and the delay times change if the power supply voltage is increased from 3.3 V to 5 V.
d) Calculate the frequency of a ring oscillator designed using three instances of the above inverter and plot the output of each inverter as a function of time.

Good Luck

*Examiner**: Dr. Mohammed Morsy***