Alexandria University
Faculty of Engineering
Communications and Computers Department
Mid-term Exam, March 2015

جامعة الإسكندرية
كلية الهندسة
قسم هندسة الإتصالات والحاسبات
امتحان نصف الفصل الدراسي الثاني (مارس ٢٠١٥)

Course Title and Code Number:
Digital Integrated Circuits Design (CC401)
Time Allowed: 1 Hours

اسم المقرر والرقم الكودي له: تصنيع و تصميم
تصميم الدوائر المتكاملة الرقميةً (CC401)
الزمن: ساعة واحدة

Answer all questions: **(20 marks)**

Question 1: **(10 marks)**

Consider a CMOS inverter, with the following device parameters:

NMOS VT0n = 0.6 V μn Cox = 60 μA/V2
PMOS VT0p = - 0.8 V μp Cox = 20 μA/V2
and VDD = 3

a) Determine the (W/L) ratios of the nMOS and pMOS transistors for a symmetric inverter.
b) Plot the VTC of the CMOS inverter and indicate the values of V_{OH}, V_{OL}, V_{IL}, and V_{IH}.
c) Calculate the inverter voltage output of two cascaded inverters for an input voltage V_i of 1V.

Question 2: **(10 marks)**

For the symmetric CMOS inverter described in Question 1:

a) Calculate the rise time and the fall time of the output signal using the average current method. The output load capacitance is 1.5 pF.
b) Determine the maximum frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0V to 3V in each cycle.
c) Calculate the dynamic power dissipation at this frequency.

Good Luck

*Examiner**: Dr. Mohammed Morsy***