Alexandria University
Faculty of Engineering
Communications and Computers Department
Final Exam, Spring 2016

جامعة الإسكندرية
كلية الهندسة
قسم هندسة الإتصالات والحاسبات
امتحان نهاية الفصل الدراسي الثاني (ربيع ٢٠١٦)

Course Title and Code Number: Digital Integrated Circuits Design (CC401)
Time Allowed: 2 Hours

اسم المقرر والرقم الكودي له: تصنيع و تصميم تصميم الدوائر المتكاملة الرقمية (CC401)
الزمن: ساعتين

Attempt all questions: **(40 marks)**

Question 1: **(10 marks)**

Consider the AOI logic function:

$$a)\quad f = \overline{a.(b + c.(d + e))}$$

a) Design a CMOS circuit realizing this function using the fewest number of transistors.
b) Determine the transistor sizes relative to a basic symmetric inverter of $(W/L)_n$ and $(W/L)_p$ size such that the logic circuit has approximately the same propagation delays as the inverter.
c) Is it possible to find an equivalent nFET and pFET Euler paths for the circuit? If so, construct a colored stick diagram layout. If not, find a layout strategy and construct the corresponding stick diagram.
d) Draw the voltage transfer characteristics of the gate and indicate all important values on it.
e) Calculate the worst fall and rise time of the gate, and indicate when they occurs?

V_{DD}=5 V, $|V_{T0}|$=1 V, C_L=5pF, $\gamma = 0.4V^{\frac{1}{2}}$, $|2\emptyset_F| = 0.6V$
$\mu p\ Cox$ = 20 μA/V2, $\mu n\ Cox$ = 50 μA/V2, $(W/L)_n$ = 0.5μm/0.25μm,

Question 2: **(9 marks)**

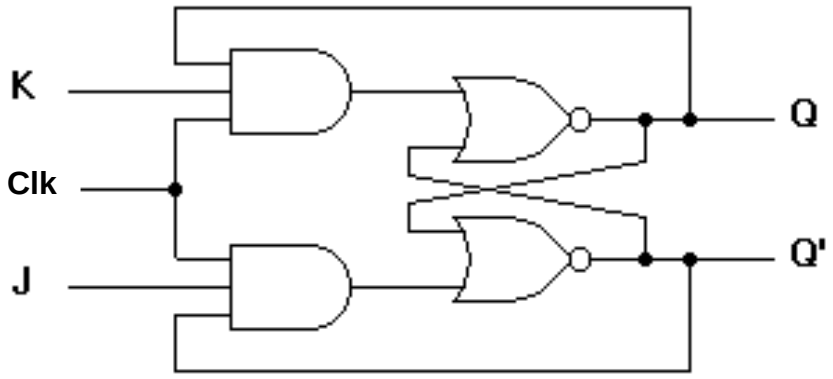
a) Design a circuit realizing this function using nMOS PTL with the fewest number of transistors.

$$y = \bar{a}c + \bar{b}\bar{c}\bar{d} + abd$$

b) Calculate the output voltage (not the logic level) for the following inputs: $a, b, c = 0$, $d = 1$ and $a, b, c, d = 0$, and calculate the propagation delay to switch between the two input combinations. Use the same V_{DD} and transistor and load capacitance parameters from Question 1.
c) Design an 8-to-1 multiplexer using transmission gates.
d) Show how the multiplexer you developed in (c) can be used to realize the function of (a).

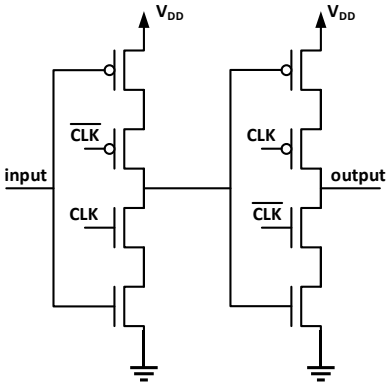
Question 3: **(9 marks)**

a) Design a CMOS circuit realizing the following JK Latch using the fewest number of transistors.



b) Establish the truth table of the JK latch of part (a) indicating each mode of operation.

c) Identify the type of the following gate and establish its truth table. Draw the transmission gate realization of the same gate and compare between the transistor count of both circuits.



Question 4: **(12 marks)**

Address	d_3	d_2	d_1	d_0
0	1	0	1	0
1	0	1	0	0
2	1	0	0	1
3	0	0	1	1

a) Design an active-low 4x4 ROM having the following truth table.

b) Design the column and row address decoders of the ROM circuit of part (a).

c) Calculate the total number of transistors used by the ROM circuit of part (a) and its decoders of part (b).

d) Consider the CMOS SRAM cell shown in the Figure below. Transistors Ml and M2 have (W/L) values of 4/4. Transistors M3 and M4 have (W/L) values of 2/4. M5 and M6 are to be sized such that the state of the cell can be changed for Vc < 0.5 V. Assuming that M5 and M6 are the same size, calculate the required (W/L). Use the following parameters:

$V_{T0,n}$ = 0.7 V, $V_{T0,p}$ = -0.7 V, K_n = 20 µA/V^2, K_p = 10 µA/V^2 , γ = 0.4 V$^{1/2}$, $|2\emptyset_F|$=0.6 V